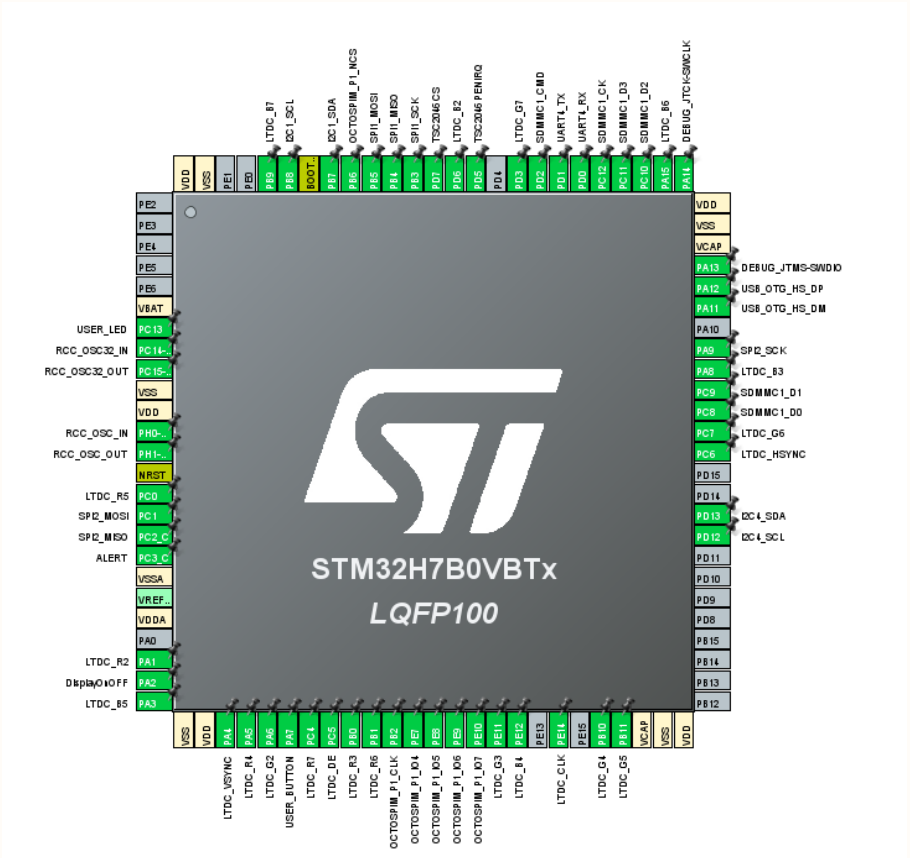
STM32 Integrated Microcontroller Demo Board

"SiMi Demo Board" Core Board

STM32H7VB0



Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

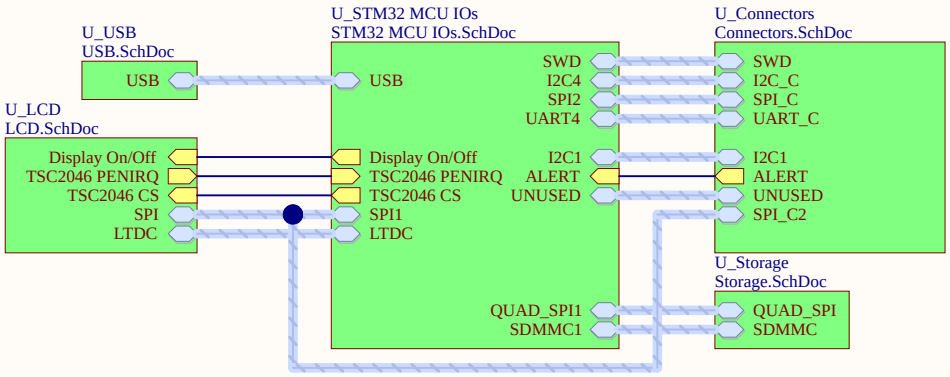
ACHTUNG!!!!!
ALTIUM EXPORTIERT BU MULTILAYER BOARDS >>PLANES<< ALS NEGATIVER GERBER. HEM MUAS MEN AUF SIGNAL STELLEN UND SELBER A PLANE ZEICHNEN

Figure 21. Six layer PCB stack-up example

	Solder Mask
Layer_1 (Top)	High Speed Signals+GND
	Prepeg
Layer_2 (Inner1)	GND Plane
	Core
Layer_3 (Inner2)	Power Plane
	Prepeg
Layer_4 (Inner3)	Low Speed Signals
	Core
Layer_5 (Inner4)	GND Plane
	Prepeg
Layer_6 (Bottom)	High Speed Signals+GND
	Solder Mask

U_Top
Top.SchDoc

Title	**Project Overview**	
Size: A4	Number	Revision: V10
Date: 5.14.2025		Sheet of
File: C:\Users\..\Project_Overview.SchDoc		Drawn By: Simon Mayr



U_STM32 MCU Power
STM32 MCU Power.SchDoc

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Date: 5.14.2025		Sheet of
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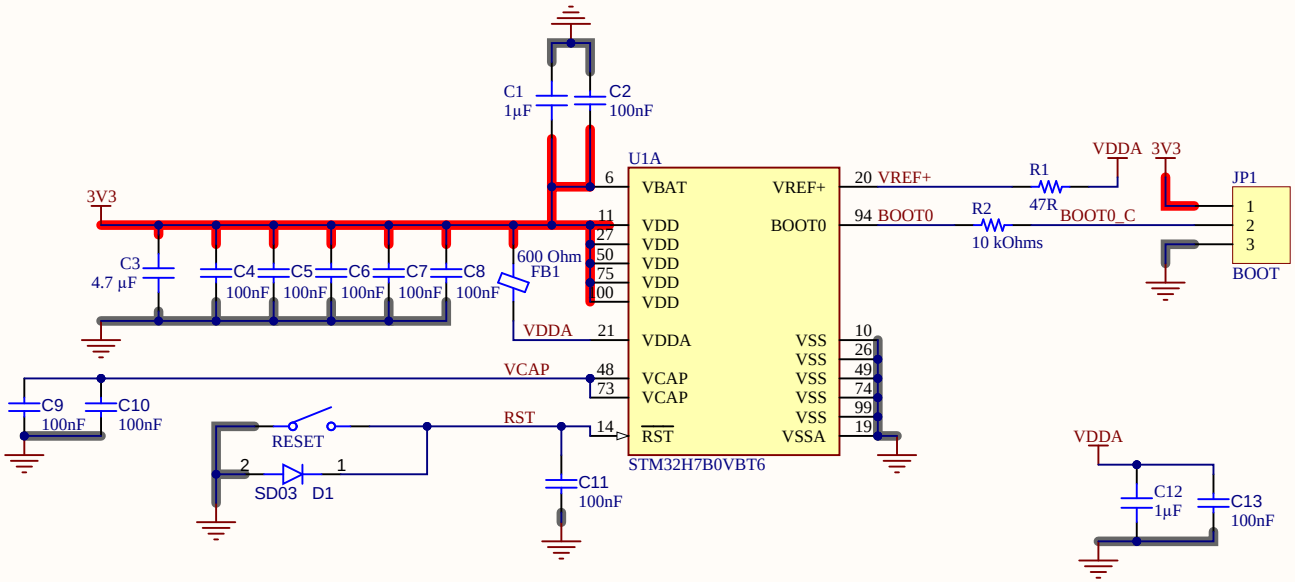

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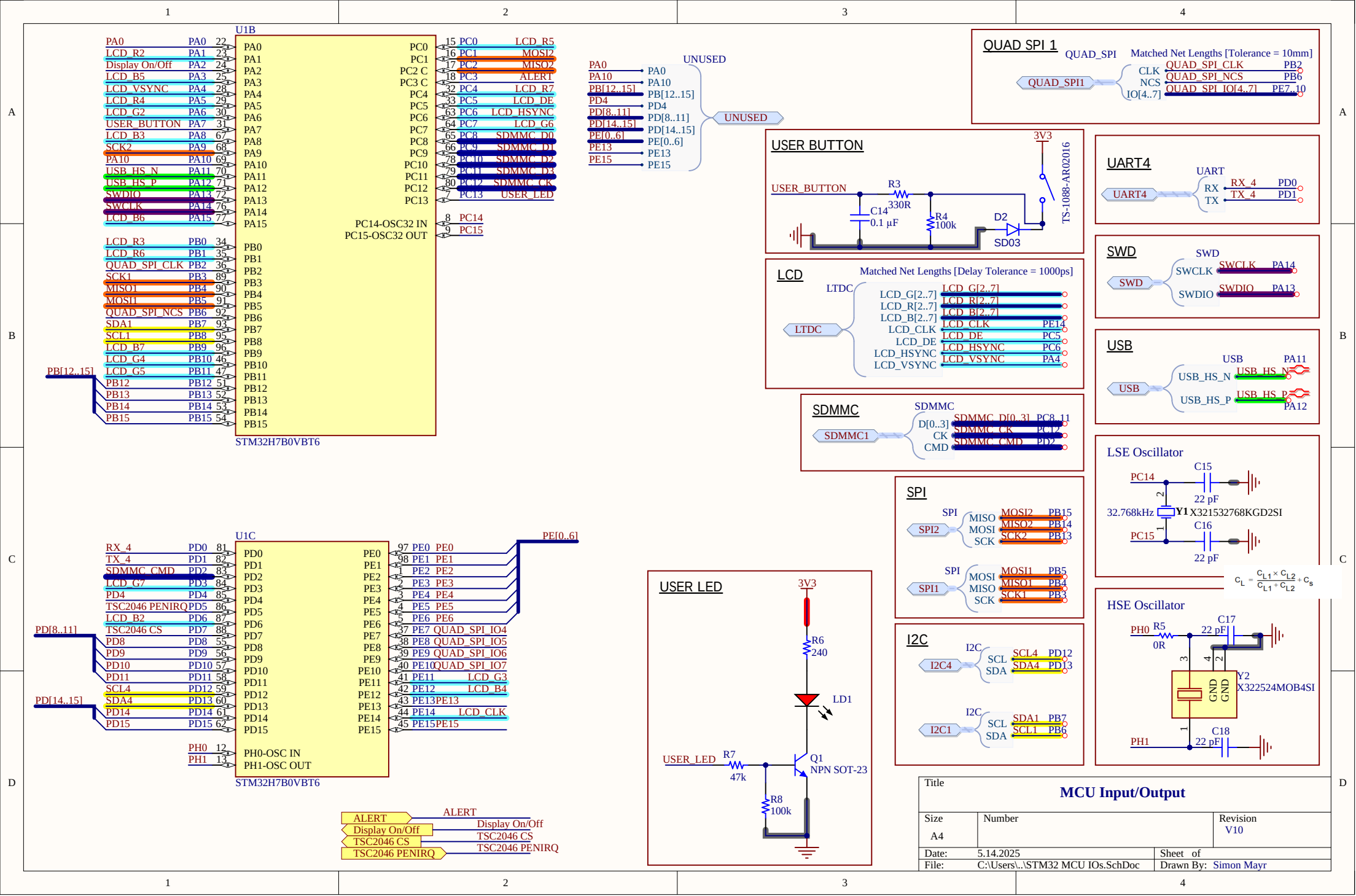
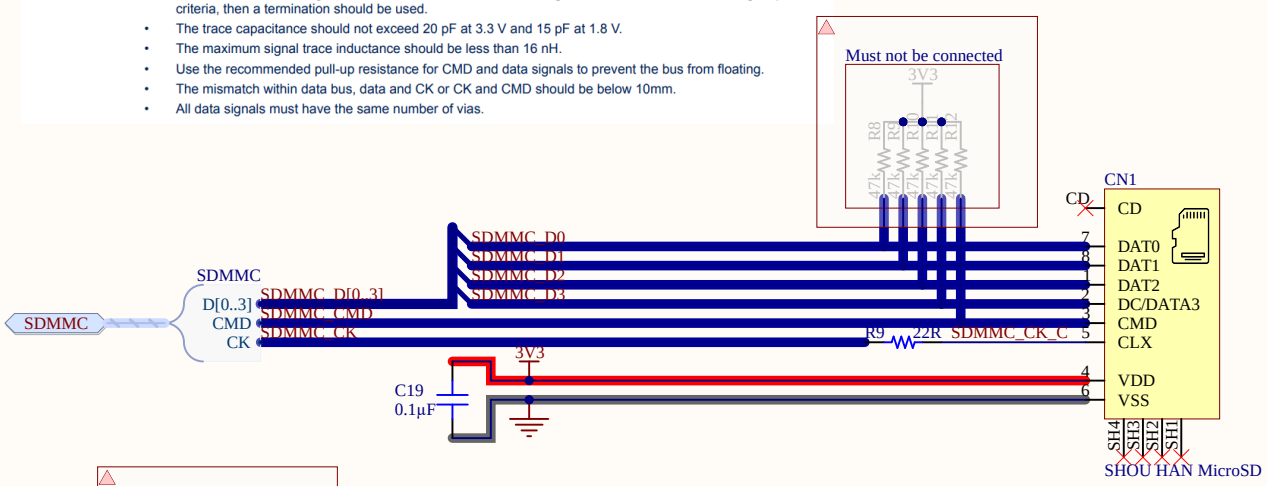
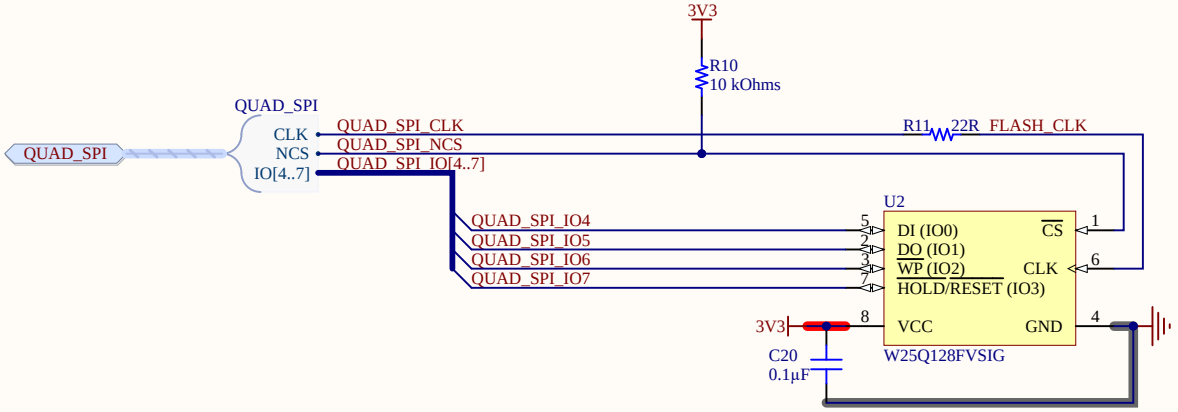

U1B
STM32H7B0VBT6
U1C
STM32H7B0VBT6
UNUSED
QUAD SPI 1
QUAD_SPI
Matched Net Lengths [Tolerance = 10mm]
USER BUTTON
3V3
TS-1088-AR02016
R3
330R
C14
0.1 µF
R4
100k
D2
SD03
UART4
SWD
USB
LCD
Matched Net Lengths [Delay Tolerance = 1000ps]
SDMMC
SPI
I2C
LSE Oscillator
32.768kHz
Y1 X321532768KGD2SI
C15
C16
22 pF
HSE Oscillator
R5
0R
C17
C18
Y2
X322524MOB4SI
USER LED
R6
240
LD1
R7
47k
Q1
NPN SOT-23
R8
100k
ALERT
Display On/Off
TSC2046 CS
TSC2046 PENIRQ
Title
MCU Input/Output
Size
A4
Number
Revision
V10
Date: 5.14.2025
Sheet of
File: C:\Users\..\STM32 MCU IOs.SchDoc
Drawn By: Simon Mayr

Interface signal layout guidelines

- Reference the plane using GND or PWR (if PWR, add 10 nF switching cap between PWR and GND).
- Trace impedance: 50 Ω ± 10%.
- All clock and data lines should have equal lengths to minimize any skew.
- The maximum skew between data and clock should be less than 250 ps at 10 mm.
- The maximum trace length should be less than 120 mm. If the signal trace exceeds this trace-length/speed criteria, then a termination should be used.
- The trace capacitance should not exceed 20 pF at 3.3 V and 15 pF at 1.8 V.
- The maximum signal trace inductance should be less than 16 nH.
- Use the recommended pull-up resistance for CMD and data signals to prevent the bus from floating.
- The mismatch within data bus, data and CK or CK and CMD should be below 10mm.
- All data signals must have the same number of vias.





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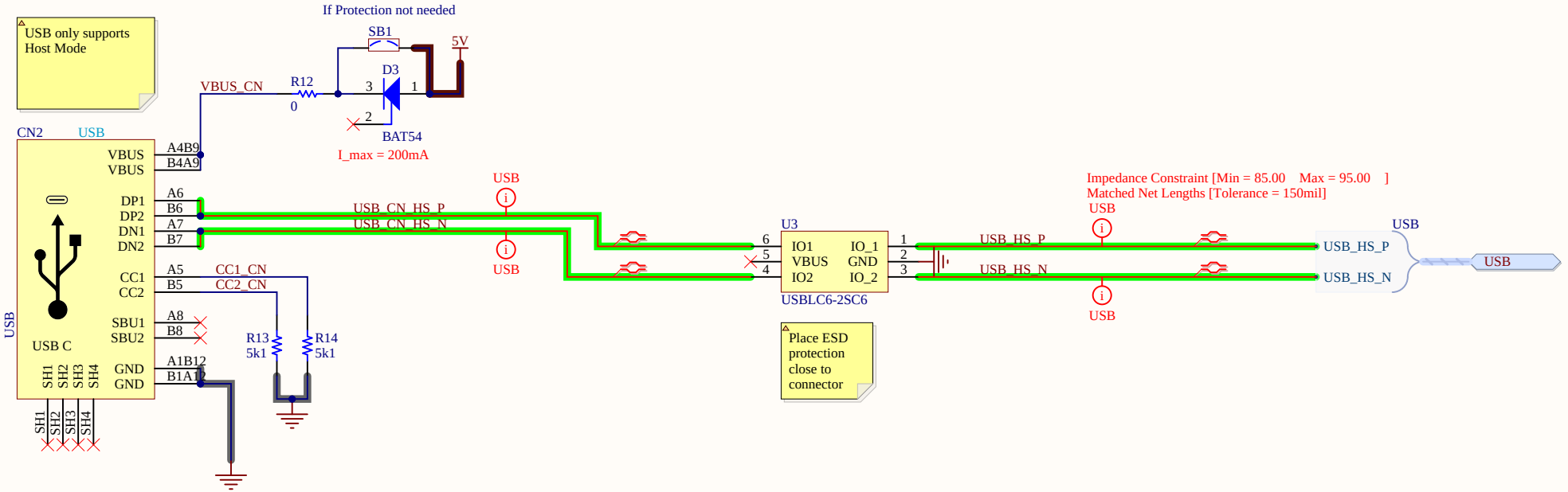

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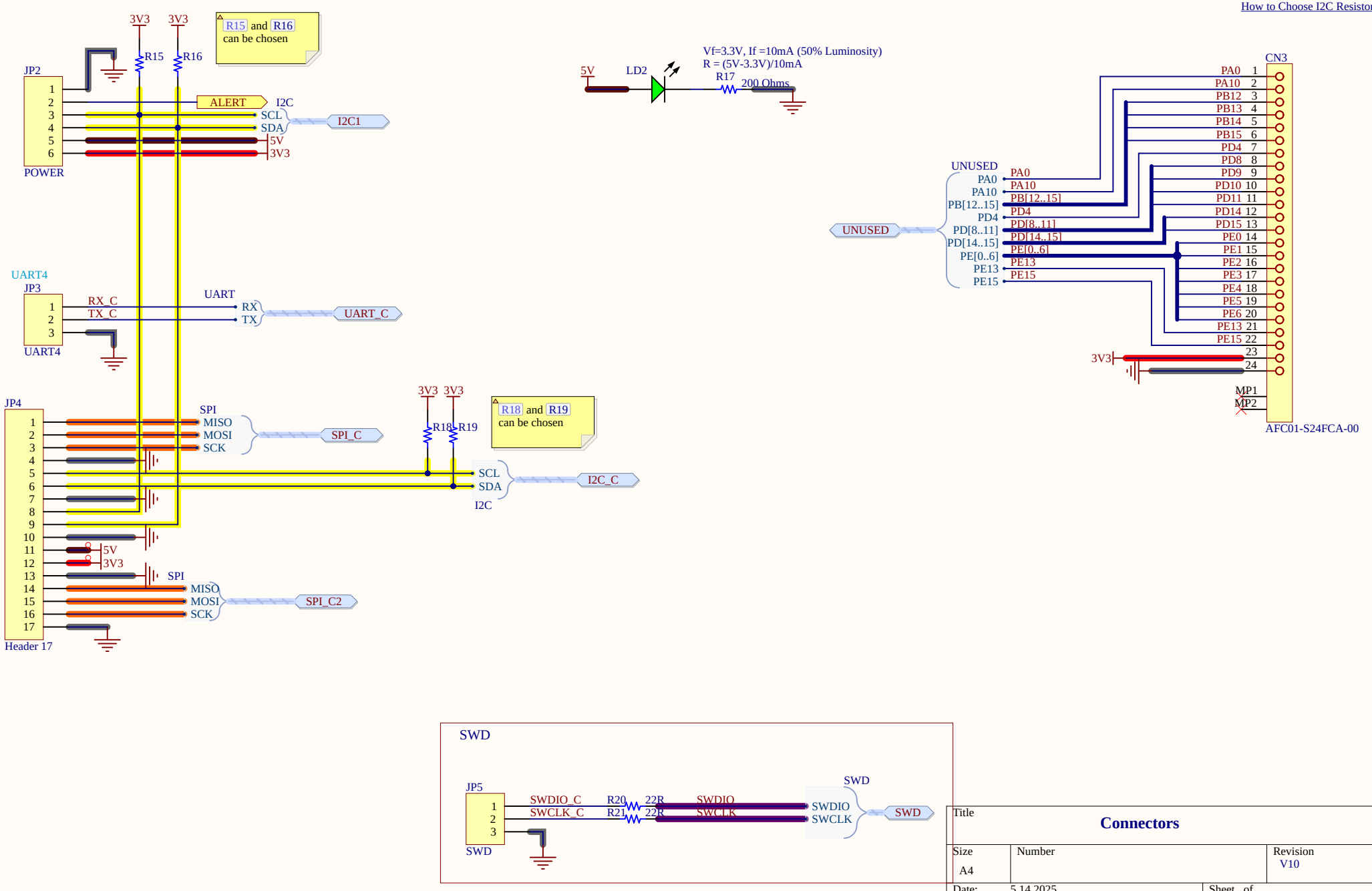
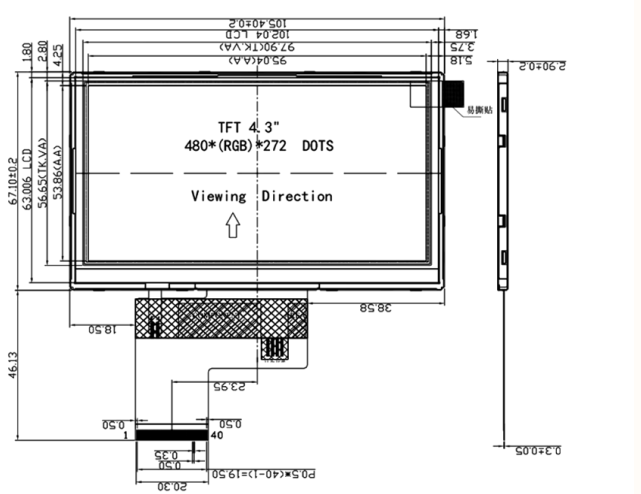


Title	**Connectors**	
Size: A4	Number:	Revision: V10
Date: 5.14.2025		Sheet of
File: C:\Users\..\Connectors.SchDoc		Drawn By: Simon Mayr

Flipped so screen can be used properly

Pin.No	Symbol	Function
1	LEDK	back light power supply negative
2	LEDA	back light power supply positive
3	GND	Ground
4	VCC	Power supply
5-12	R0-R7	Red Data
13-20	G0-G7	Green Data
21-28	B0-B7	Blue Data
29	GND	Ground
30	CLK	Colock signal
31	DISP	Display on/off
32	HSYNC	Horizontal sync input in RGB mode(short to GND if not used)
33	VSYNC	Vertical sync input in RGB mode(short to GND if not used)
34	DE	Data enable
35	NC	No Connection
36	GND	Ground
37	XR	touch panel X-right
38	YD	touch panel Y-bottom
39	XL	touch panel X-left
40	YU	touch panel Y-upl



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