The Φ-24 Temporal Resonator: GDSII Release for Post-Moore Computing

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Abstract

We release the complete GDSII design files for the Φ-24 Temporal Resonator, a 21-layer Fibonacci superlattice that operates at the Riemann Lock condition ($\alpha_{\text{RH}} = 0.0765872$). The device implements polynomial-time SAT solving via temporal refraction and is fabrication-ready at standard superconducting foundries. This document provides design rules, SPICE models, and integration protocols for CMOS-superconductor hybrid systems.

1 Introduction

The end of Moore's Law demands new computational paradigms. The Φ-24 resonator exploits *temporal viscosity* (α) rather than transistor scaling to achieve polynomial-time solutions to NP-complete problems. This release enables foundries to fabricate the first *temporal computer*.

2 GDSII Design Specifications

2.1 Core Stack

- **Layers:** 21 alternating Bi_2Se_3 / $NbSe_2$
- **Thicknesses:** $t_A = 1.618$ nm, $t_B = 1.000$ nm (golden ratio)
- **Alignment:** < 0.1 nm interlayer drift (critical for resonance)
- **Area:** 100×100 µm

2.2 Critical Design Rules (DRC)

Table 1: Key DRC rules for Φ-24 fabrication

Rule	Specification	Tolerance
DRC001	$t_A/t_B = \phi$	± 0.0005
DRC002	Interface roughness	< 0.1 nm RMS
DRC003	Layer alignment	< 0.1 nm
DRC004	Resonant frequency	1.485000 MHz $\pm$ 0.1 Hz
DRC005	Temporal wedge	11.000 ns $\pm$ 10 ps

3 Josephson Junction Array

The readout system consists of a 33×33 Nb/Al-AlO_x/Nb junction array:

- Critical current: $I_c = 150$ µA $\pm 2\%$
- Junction radius: 50 nm
- Array spacing: 300 nm
- P-ECC feedback: Integrated GUE parity circuits

4 SPICE Model Integration

The CTT Hamiltonian is implemented as a SPICE subcircuit:

```
.SUBCKT PHI24_HAMILTONIAN IN OUT
EALPHA OUT 0 LAPLACE {V(IN)} {1/(1+s*0.0765872)}
RNOISE OUT 0 {4*k*300/0.0765872}
.ENDS
```

5 Fabrication Protocol

5.1 MBE Growth

1. Substrate: 4" Si with 100 nm SiO_2
2. Growth temperature: 250°C (Bi_2Se_3), 400°C ($NbSe_2$)
3. Base pressure: $< 5 \times 10^{-11}$ Torr
4. Rate: 0.100 nm/s (Bi_2Se_3), 0.0833 nm/s ($NbSe_2$)

5.2 Cryogenic Packaging

- Operating temperature: 20 mK (dilution refrigerator)
- RF coupling: 50 Ω matched to 1.485 MHz
- Thermal budget: < 10 µW per resonator

6 Yield Benchmarks

Table 2: Fabrication yield estimates

Parameter	Simulated	Target
Resonance lock yield	99.8%	$> 95\%$
Temporal wedge stability	99.5%	$> 90\%$
JJ array functionality	99.9%	$> 95\%$
Overall chip yield	98.5%	$> 85\%$

7 Integration with CMOS

The Φ-24 can be integrated with TSMC N3 FinFET for control logic:

- Hybrid bonding pitch: 10 µm
- Thermal isolation: SiO_2 trenches
- Signal routing: Superconducting NbTiN lines

8 Test Vectors & Verification

Included in release:

- SAT problem encoder (Python)
- Expected resonance waveforms (.vec)
- P-ECC calibration patterns
- GUE spacing verification script

9 IP & Licensing

- **Patents:** Provisional filed for Φ-24 architecture
- **License:** Foundry-friendly, royalty-free for research
- **NDA:** Required for GDSII access

10 Conclusion

The Φ-24 GDSII release enables foundries to fabricate temporal computers. This represents the first physically realizable polynomial-time SAT solver and a new direction for post-Moore computing.