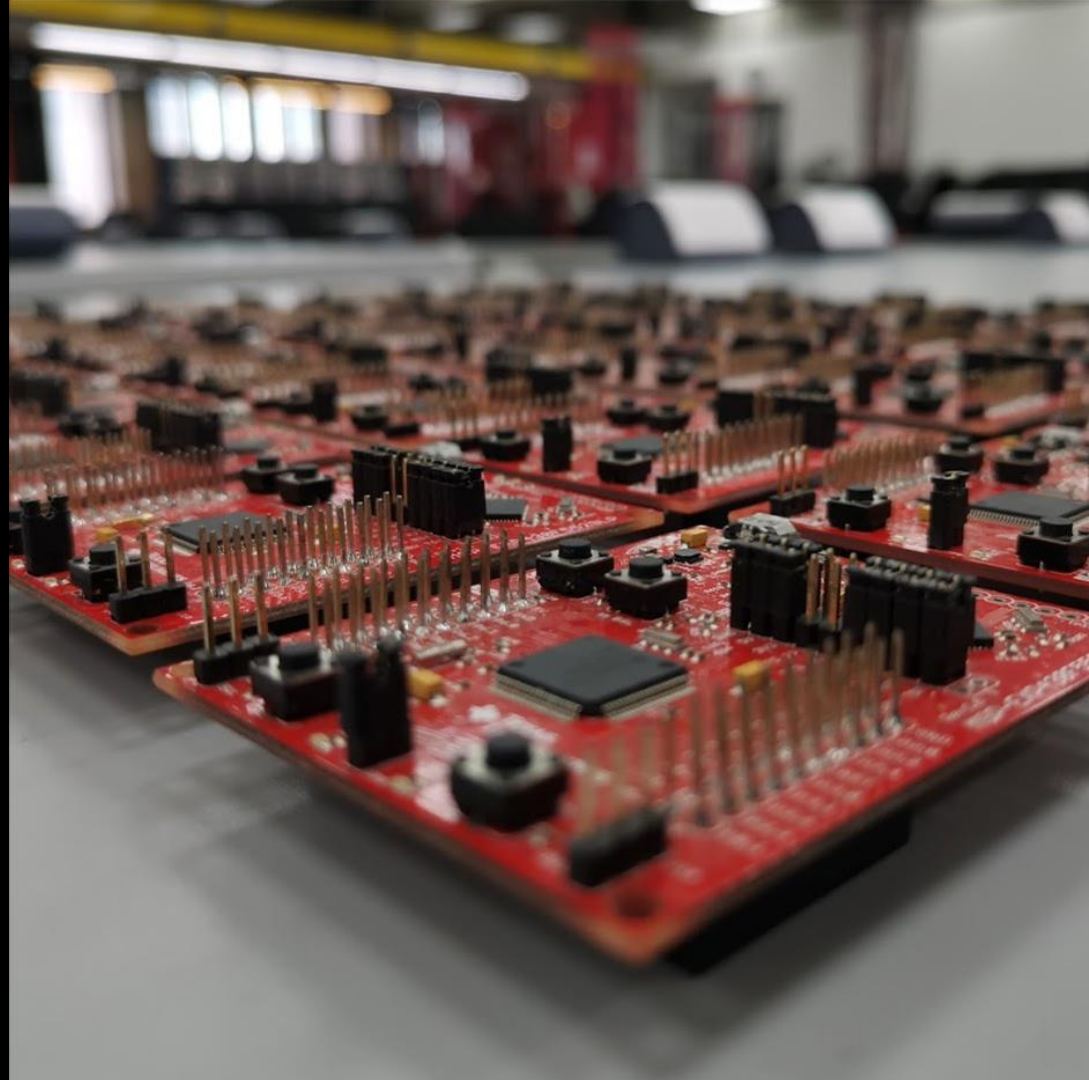
IEE2463 Sistemas Electrónicos Programables

Javier Silva Orellana
jisilva8@uc.cl
GitHub: slothzilla328p

2do semestre 2020

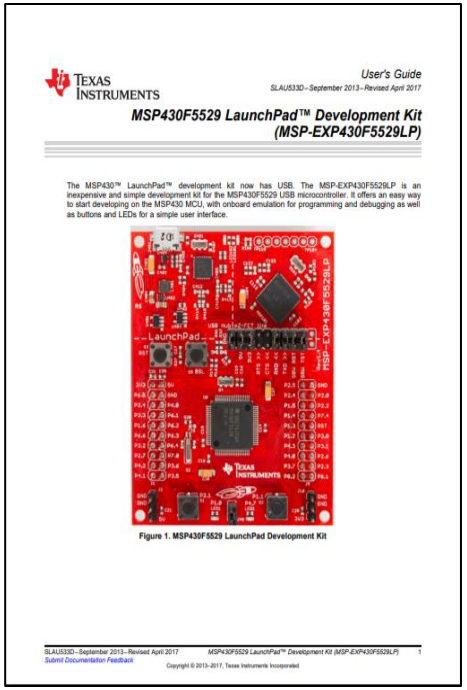


UART

UART

Universal Asynchronous Receiver-Transmitter

The four horsemen of apocalypse



TEXAS INSTRUMENTS

User's Guide

SLAU533D–September 2013–Revised April 2017

MSP430F5529 LaunchPad™ Development Kit (MSP-EXP430F5529LP)

The MSP430™ LaunchPad™ development kit now has USB. The MSP-EXP430F5529LP is an inexpensive and simple development kit for the MSP430F5529 USB microcontroller. It offers an easy way to start developing on the MSP430 MCU, with onboard emulation for programming and debugging as well as buttons and LEDs for a simple user interface.

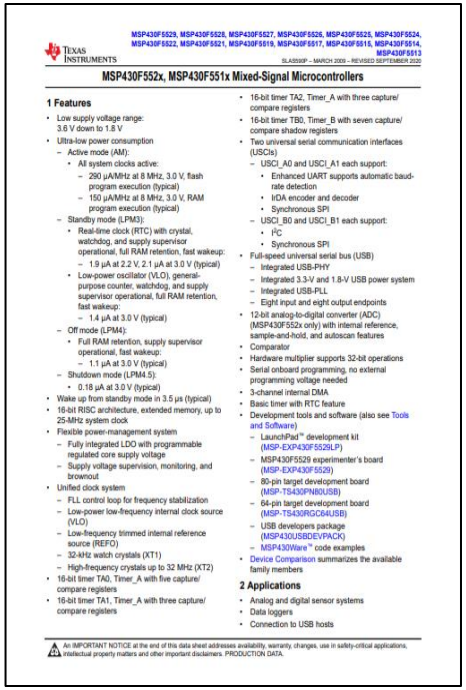
Figure 1. MSP430F5529 LaunchPad Development Kit

SLAU533D–September 2013–Revised April 2017 MSP430F5529 LaunchPad™ Development Kit (MSP-EXP430F5529LP) 1

Submit Documentation Feedback

Copyright © 2013–2017, Texas Instruments Incorporated

Launchpad



MSP430F5529, MSP430F5528, MSP430F5527, MSP430F5526, MSP430F5525, MSP430F5524, MSP430F5522, MSP430F5521, MSP430F5519, MSP430F5517, MSP430F5515, MSP430F5514, MSP430F5513

TEXAS INSTRUMENTS

SLAS590P – MARCH 2009 – REVISED SEPTEMBER 2020

MSP430F552x, MSP430F551x Mixed-Signal Microcontrollers

1 Features

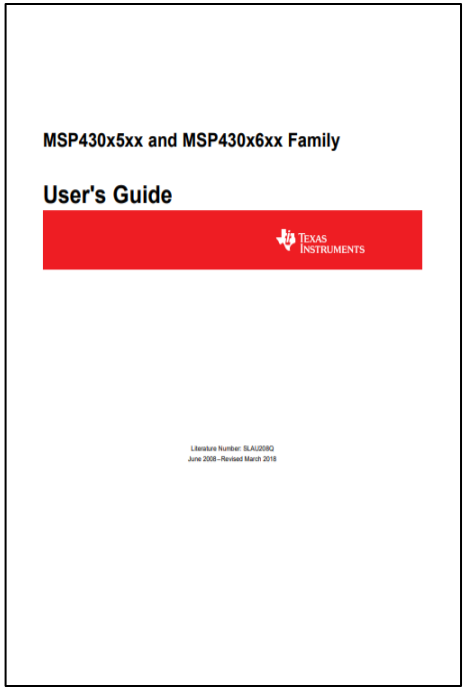
- Low supply voltage range: 3.6 V down to 1.8 V
- Ultra-low power consumption
  - Active mode (AM):
    - All system clocks active:
      - 290 µA/MHz at 8 MHz, 3.0 V, flash program execution (typical)
      - 150 µA/MHz at 8 MHz, 3.0 V, RAM program execution (typical)
  - Standby mode (LPM3):
    - Real-time clock (RTC) with crystal, watchdog, and supply supervisor operational, full RAM retention, fast wakeup:
      - 1.9 µA at 2.2 V, 2.1 µA at 3.0 V (typical)
    - Low-power oscillator (VLO), general-purpose counter, watchdog, and supply supervisor operational, full RAM retention, fast wakeup:
      - 1.4 µA at 3.0 V (typical)
  - Off mode (LPM4):
    - Full RAM retention, supply supervisor operational, fast wakeup:
      - 1.1 µA at 3.0 V (typical)
  - Shutdown mode (LPM4.5):
    - 0.18 µA at 3.0 V (typical)
- Wake up from standby mode in 3.5 µs (typical)
- 16-bit RISC architecture, extended memory, up to 25-MHz system clock
- Flexible power-management system
  - Fully integrated LDO with programmable regulated core supply voltage
  - Supply voltage supervision, monitoring, and brownout
- Unified clock system
  - FLL control loop for frequency stabilization
  - Low-power low-frequency internal clock source (VLO)
  - Low-frequency trimmed internal reference source (REFO)
  - 32-kHz watch crystals (XT1)
  - High-frequency crystals up to 32 MHz (XT2)
- 16-bit timer TA0, Timer_A with five capture/compare registers
- 16-bit timer TA1, Timer_A with three capture/compare registers
- 16-bit timer TA2, Timer_A with three capture/compare registers
- 16-bit timer TB0, Timer_B with seven capture/compare shadow registers
- Two universal serial communication interfaces (USCIs)
  - USCI_A0 and USCI_A1 each support:
    - Enhanced UART supports automatic baud-rate detection
    - IrDA encoder and decoder
    - Synchronous SPI
  - USCI_B0 and USCI_B1 each support:
    - I²C
    - Synchronous SPI
- Full-speed universal serial bus (USB)
  - Integrated USB-PHY
  - Integrated 3.3-V and 1.8-V USB power system
  - Integrated USB-PLL
  - Eight input and eight output endpoints
- 12-bit analog-to-digital converter (ADC) (MSP430F552x only) with internal reference, sample-and-hold, and autoscan features
- Comparator
- Hardware multiplier supports 32-bit operations
- Serial onboard programming, no external programming voltage needed
- 3-channel internal DMA
- Basic timer with RTC feature
- Development tools and software (also see Tools and Software)
  - LaunchPad™ development kit (MSP-EXP430F5529LP)
  - MSP430F5529 experimenter's board (MSP-EXP430F5529)
  - 80-pin target development board (MSP-TS430PN80USB)
  - 64-pin target development board (MSP-TS430RGC64USB)
  - USB developers package (MSP430USBDEVPACK)
  - MSP430Ware™ code examples
- Device Comparison summarizes the available family members

2 Applications

- Analog and digital sensor systems
- Data loggers
- Connection to USB hosts

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Especificaciones Técnicas



MSP430x5xx and MSP430x6xx Family

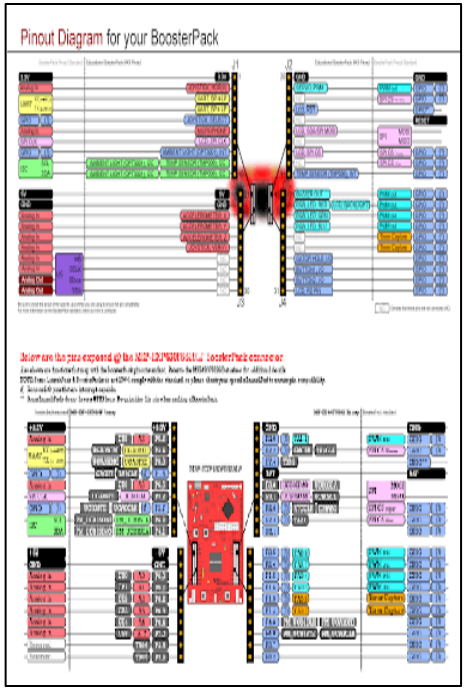
User's Guide

TEXAS INSTRUMENTS

Literature Number: SLAU208Q

June 2008–Revised March 2018

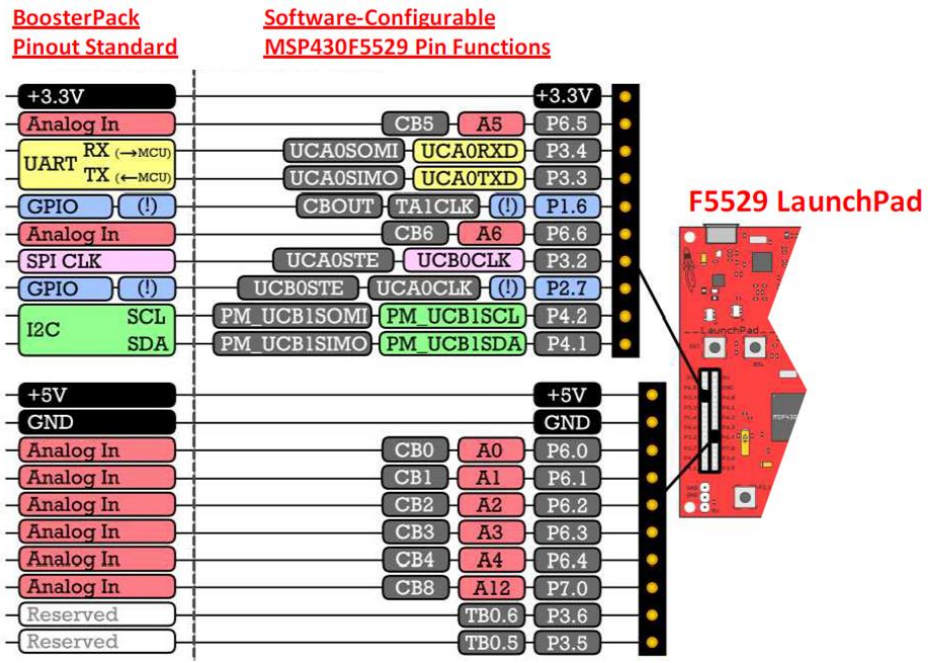
Manual de uso



Pinout

¿Dónde?

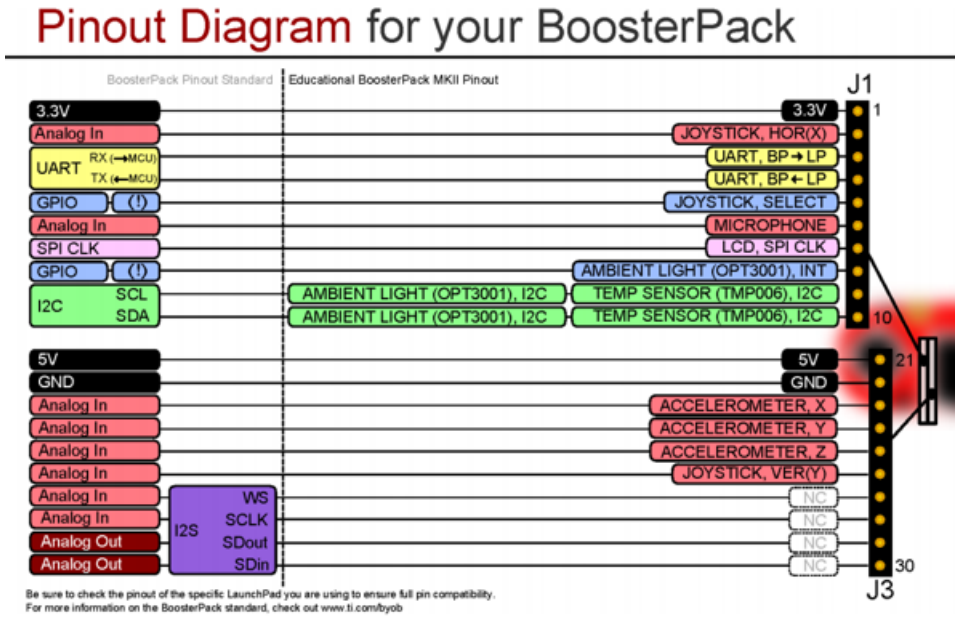
- La MSP430F5529 presenta un par de pines para comunicación serial. Estos corresponden a **P3.4** (UCA0RXD) y **P3.3** (UCA0TXD).



¿Dónde?

- La MSP430F5529 presenta un par de pines para comunicación serial. Estos corresponden a **P3.4** (UCA0RXD) y **P3.3** (UCA0TXD).

- Estos mismos pines también se encuentran directamente conectados al BoosterPack.

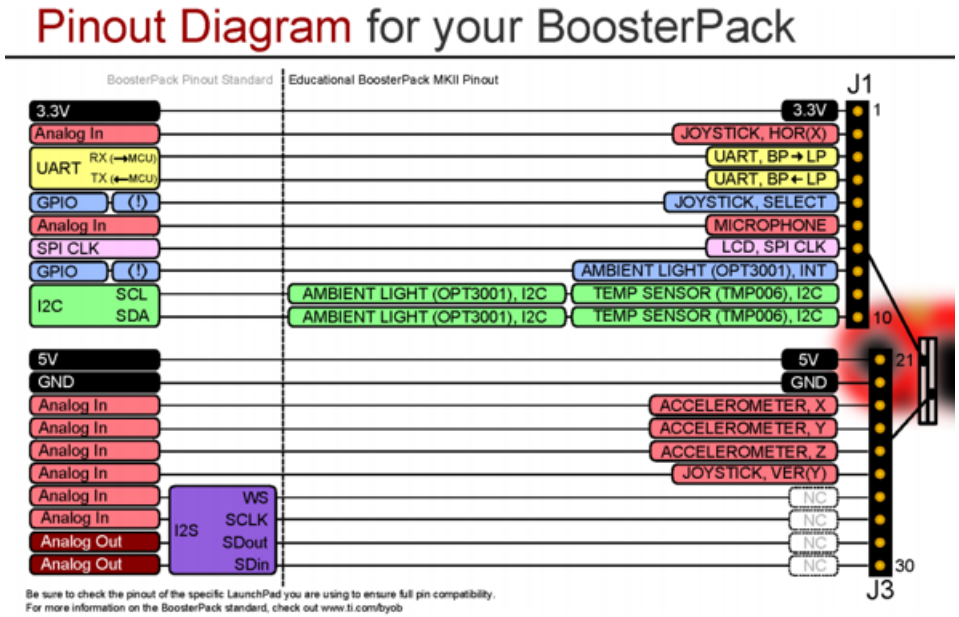


¿Dónde?

- La MSP430F5529 presenta un par de pines para comunicación serial. Estos corresponden a **P3.4** (UCA0RXD) y **P3.3** (UCA0TXD).

- Estos mismos pines también se encuentran directamente conectados al BoosterPack.

- No tenemos jumpers, **¿cómo emplearemos el UART?**



Revisemos el detalle del Launchpad

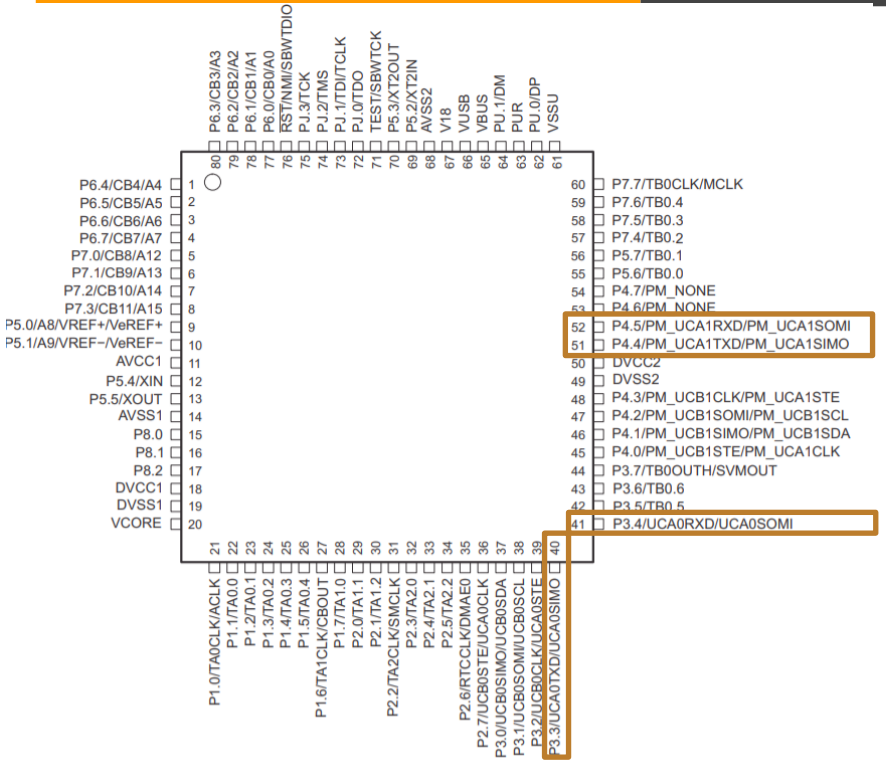


Figure 9. MSP430F5529 Pinout

[Página 11]

- Además de P3.3 y P3.4, la MSP430F5529 cuenta con otro par de pines para UART, **P4.4 (Tx)** y **P4.5 (Rx)**.

- **¿Por qué no figuran en el pinout anterior?**

Revisemos el detalle del Launchpad

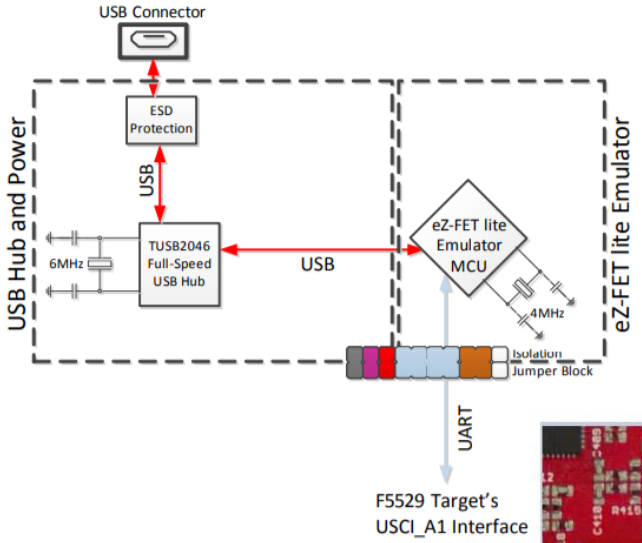


Figure 14. Backchannel UART Pathway

[Páginas 16 y 17]

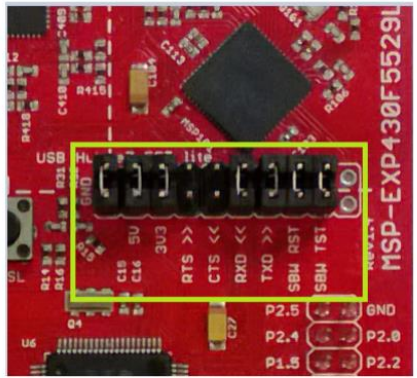
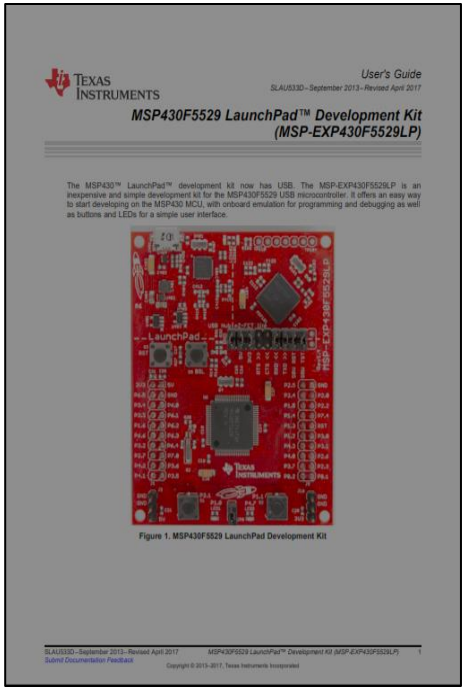
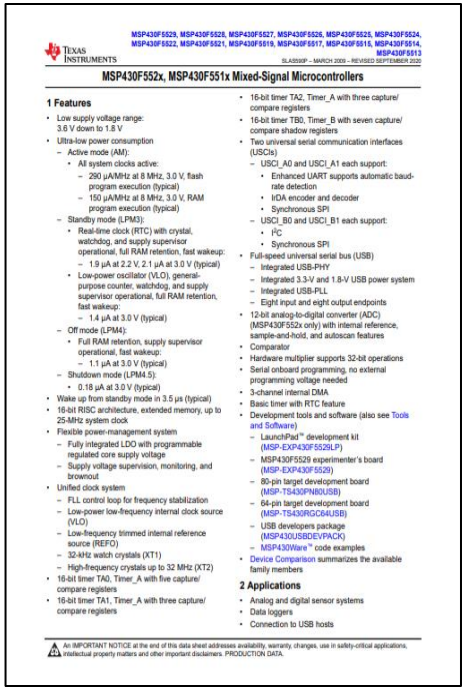


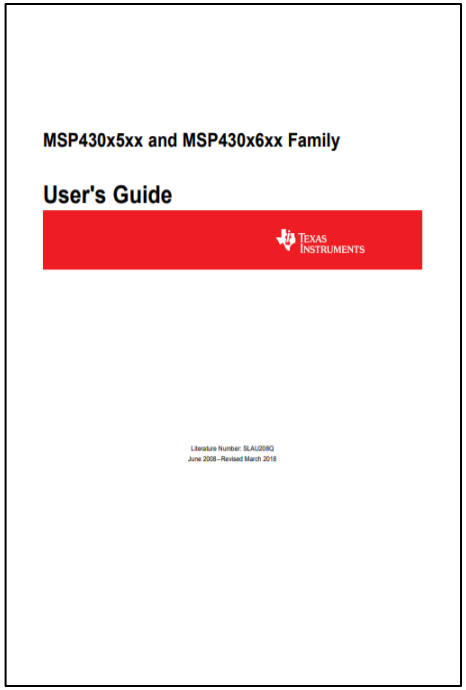
Figure 16. Isolation Jumper Block

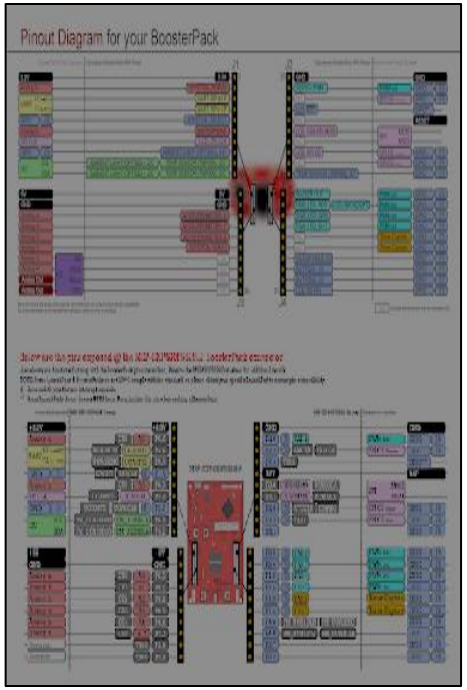
- Además de P3.3 y P3.4, la MSP430F5529 cuenta con otro par de pines para UART, **P4.4 (Tx)** y **P4.5 (Rx)**.
- **¿Por qué no figuran en el pinout anterior?**
- Están vinculados al conector USB del Launchpad.
- **POR FAVOR REVISEN QUE LOS JUMPERS TXD y RXD ESTÉN PUESTOS.**

The four horsemen of apocalypse









Launchpad | Especificaciones Técnicas | Manual de uso | Pinout

Especificaciones de Interés

8.29 USCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			1	MHz

8.30 USCI (UART Mode)

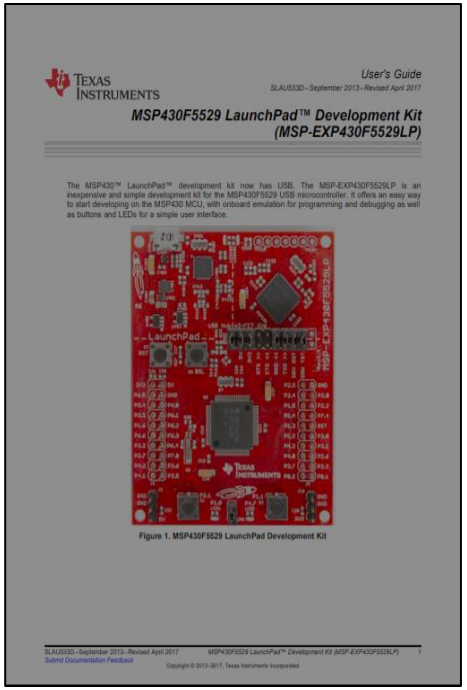
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

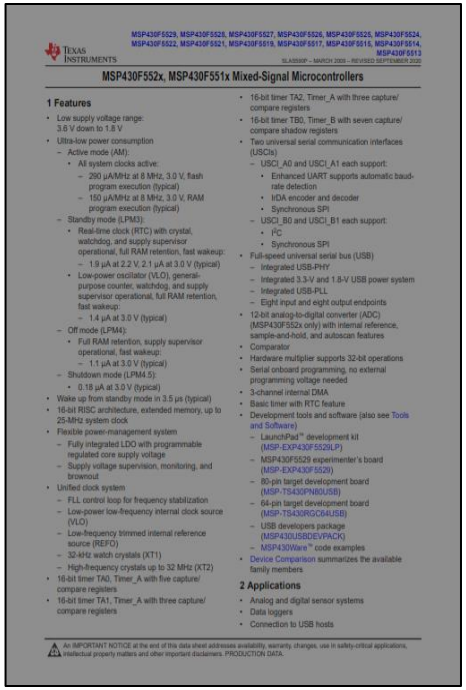
PARAMETER		V_{CC}	MIN	MAX	UNIT
t_t	UART receive deglitch time(1)	2.2 V	50	600	ns
		3 V	50	600	

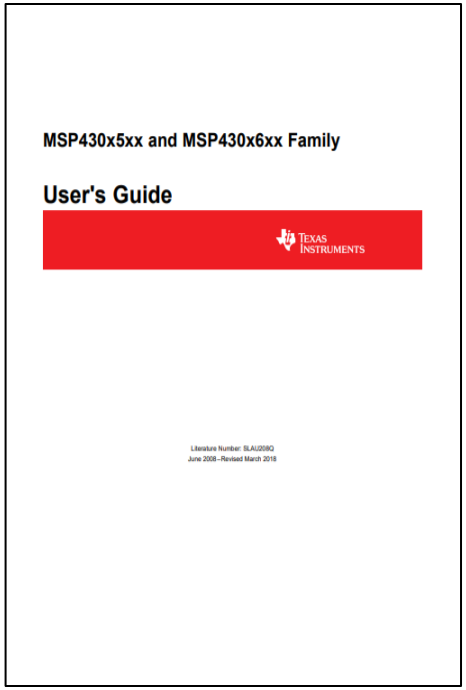
(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

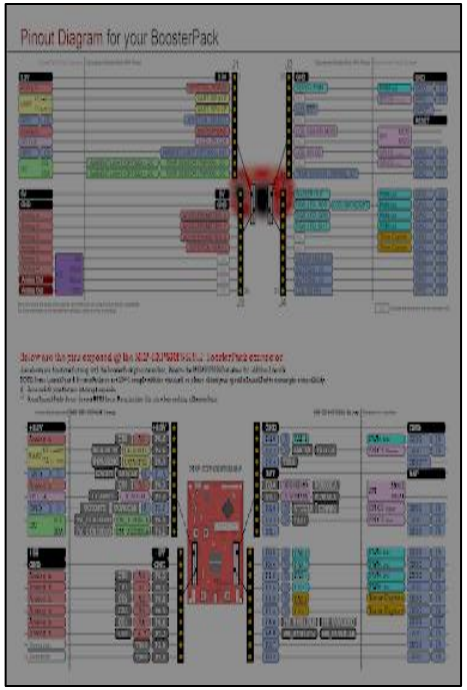
[Página 38]

The four horsemen of apocalypse





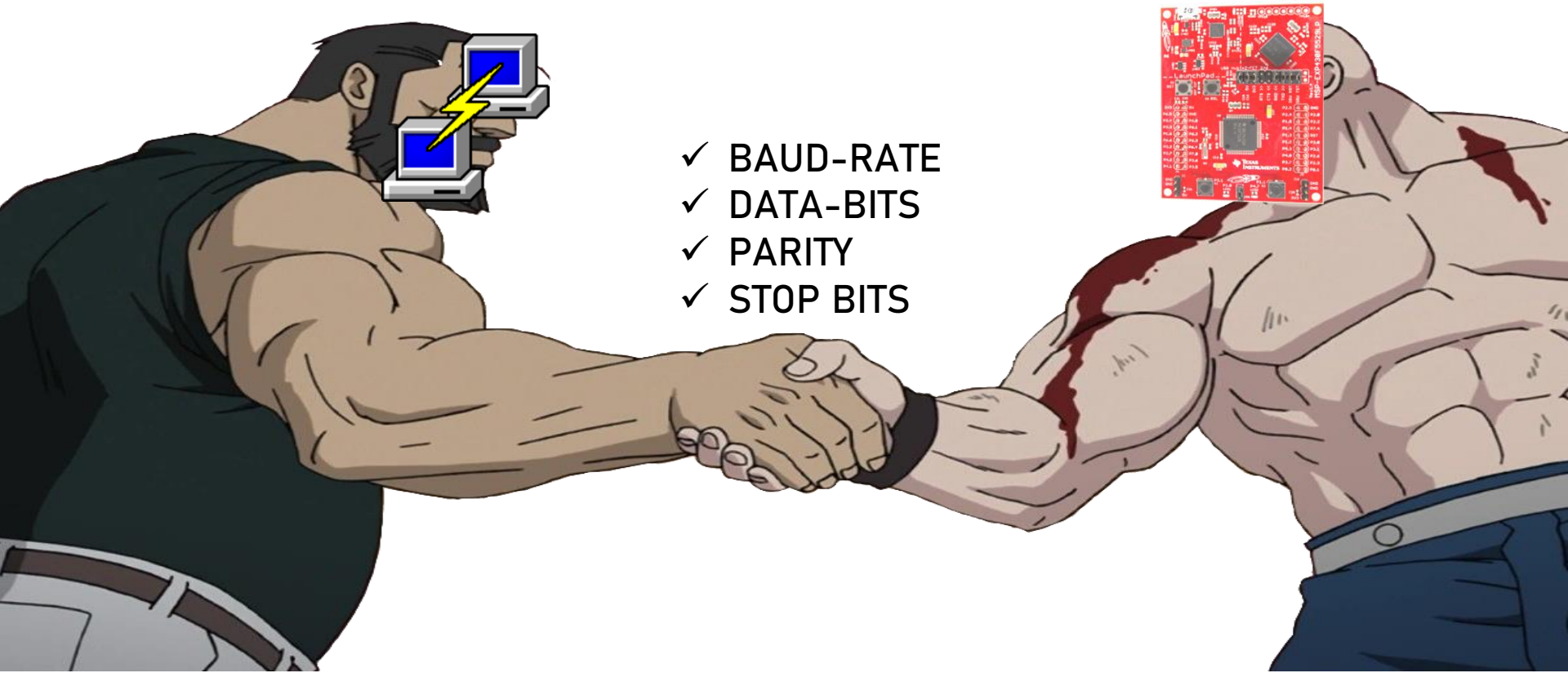




Launchpad | Especificaciones Técnicas | Manual de uso | Pinout

Configurando UART (User’s Guide Ch. 36)

Configurando UART: Handshake



Configurando UART: Registros

Table 36-6. USCI_A UART Mode Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	UCAxCTLW0	USCI_Ax Control Word 0	Read/write	Word	0001h	
00h	UCAxCTL1	USCI_Ax Control 1	Read/write	Byte	01h	Section 36.4.2
01h	UCAxCTL0	USCI_Ax Control 0	Read/write	Byte	00h	Section 36.4.1
06h	UCAxBRW	USCI_Ax Baud Rate Control Word	Read/write	Word	0000h	
06h	UCAxBR0	USCI_Ax Baud Rate Control 0	Read/write	Byte	00h	Section 36.4.3
07h	UCAxBR1	USCI_Ax Baud Rate Control 1	Read/write	Byte	00h	Section 36.4.4
08h	UCAxMCTL	USCI_Ax Modulation Control	Read/write	Byte	00h	Section 36.4.5
09h		Reserved - reads zero	Read	Byte	00h	
0Ah	UCAxSTAT	USCI_Ax Status	Read/write	Byte	00h	Section 36.4.6
0Bh		Reserved - reads zero	Read	Byte	00h	
0Ch	UCAxRXBUF	USCI_Ax Receive Buffer	Read/write	Byte	00h	Section 36.4.7
0Dh		Reserved - reads zero	Read	Byte	00h	
0Eh	UCAxTXBUF	USCI_Ax Transmit Buffer	Read/write	Byte	00h	Section 36.4.8
0Fh		Reserved - reads zero	Read	Byte	00h	
10h	UCAxABCTL	USCI_Ax Auto Baud Rate Control	Read/write	Byte	00h	Section 36.4.11
11h		Reserved - reads zero	Read	Byte	00h	
12h	UCAxIRCTL	USCI_Ax IrDA Control	Read/write	Word	0000h	
12h	UCAxIRTCTL	USCI_Ax IrDA Transmit Control	Read/write	Byte	00h	Section 36.4.9
13h	UCAxIRRCTL	USCI_Ax IrDA Receive Control	Read/write	Byte	00h	Section 36.4.10
1Ch	UCAxICTL	USCI_Ax Interrupt Control	Read/write	Word	0000h	
1Ch	UCAxIE	USCI_Ax Interrupt Enable	Read/write	Byte	00h	Section 36.4.12
1Dh	UCAxIFG	USCI_Ax Interrupt Flag	Read/write	Byte	00h	Section 36.4.13
1Eh	UCAxIV	USCI_Ax Interrupt Vector	Read	Word	0000h	Section 36.4.14

Configurando UART: Baud Rate

Table 36-4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0

BRCLK Frequency (Hz)	Baud Rate (baud)	UCBRx	UCBRSx	UCBRFx	Maximum TX Error (%)		Maximum RX Error (%)	
32 768	1200	27	2	0	-2.8	1.4	-5.9	2.0
32 768	2400	13	6	0	-4.8	6.0	-9.7	8.3
32 768	4800	6	7	0	-12.1	5.7	-13.4	19.0
32 768	9600	3	3	0	-21.1	15.2	-44.3	21.3
1 000 000	9600	104	1	0	-0.5	0.6	-0.9	1.2
1 000 000	19200	52	0	0	-1.8	0	-2.6	0.9
1 000 000	38400	26	0	0	-1.8	0	-3.6	1.8
1 000 000	57600	17	3	0	-2.1	4.8	-6.8	5.8
1 000 000	115200	8	6	0	-7.8	6.4	-9.7	16.1

Configurando UART: Registros

- Gran variedad de combinaciones para el formato del mensaje.

¿Cómo podemos hacer una configuración sencilla de cambiar?

UART: Tx y Rx char a char (User’s Guide Ch. 36)

Tx/Rx: Interruption Flags

Table 36-6. USCI_A UART Mode Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	UCAxCTLW0	USCI_Ax Control Word 0	Read/write	Word	0001h	
00h	UCAxCTL1	USCI_Ax Control 1	Read/write	Byte	01h	Section 36.4.2
01h	UCAxCTL0	USCI_Ax Control 0	Read/write	Byte	00h	Section 36.4.1
06h	UCAxBRW	USCI_Ax Baud Rate Control Word	Read/write	Word	0000h	
06h	UCAxBR0	USCI_Ax Baud Rate Control 0	Read/write	Byte	00h	Section 36.4.3
07h	UCAxBR1	USCI_Ax Baud Rate Control 1	Read/write	Byte	00h	Section 36.4.4
08h	UCAxMCTL	USCI_Ax Modulation Control	Read/write	Byte	00h	Section 36.4.5
09h		Reserved - reads zero	Read	Byte	00h	
0Ah	UCAxSTAT	USCI_Ax Status	Read/write	Byte	00h	Section 36.4.6
0Bh		Reserved - reads zero	Read	Byte	00h	
0Ch	UCAxRXBUF	USCI_Ax Receive Buffer	Read/write	Byte	00h	Section 36.4.7
0Dh		Reserved - reads zero	Read	Byte	00h	
0Eh	UCAxTXBUF	USCI_Ax Transmit Buffer	Read/write	Byte	00h	Section 36.4.8
0Fh		Reserved - reads zero	Read	Byte	00h	
10h	UCAxABCTL	USCI_Ax Auto Baud Rate Control	Read/write	Byte	00h	Section 36.4.11
11h		Reserved - reads zero	Read	Byte	00h	
12h	UCAxIRCTL	USCI_Ax IrDA Control	Read/write	Word	0000h	
12h	UCAxIRTCTL	USCI_Ax IrDA Transmit Control	Read/write	Byte	00h	Section 36.4.9
13h	UCAxIRRCTL	USCI_Ax IrDA Receive Control	Read/write	Byte	00h	Section 36.4.10
1Ch	UCAxICTL	USCI_Ax Interrupt Control	Read/write	Word	0000h	
1Ch	UCAxIE	USCI_Ax Interrupt Enable	Read/write	Byte	00h	Section 36.4.12
1Dh	UCAxIFG	USCI_Ax Interrupt Flag	Read/write	Byte	00h	Section 36.4.13
1Eh	UCAxIV	USCI_Ax Interrupt Vector	Read	Word	0000h	Section 36.4.14

Tx/Rx: Buffers

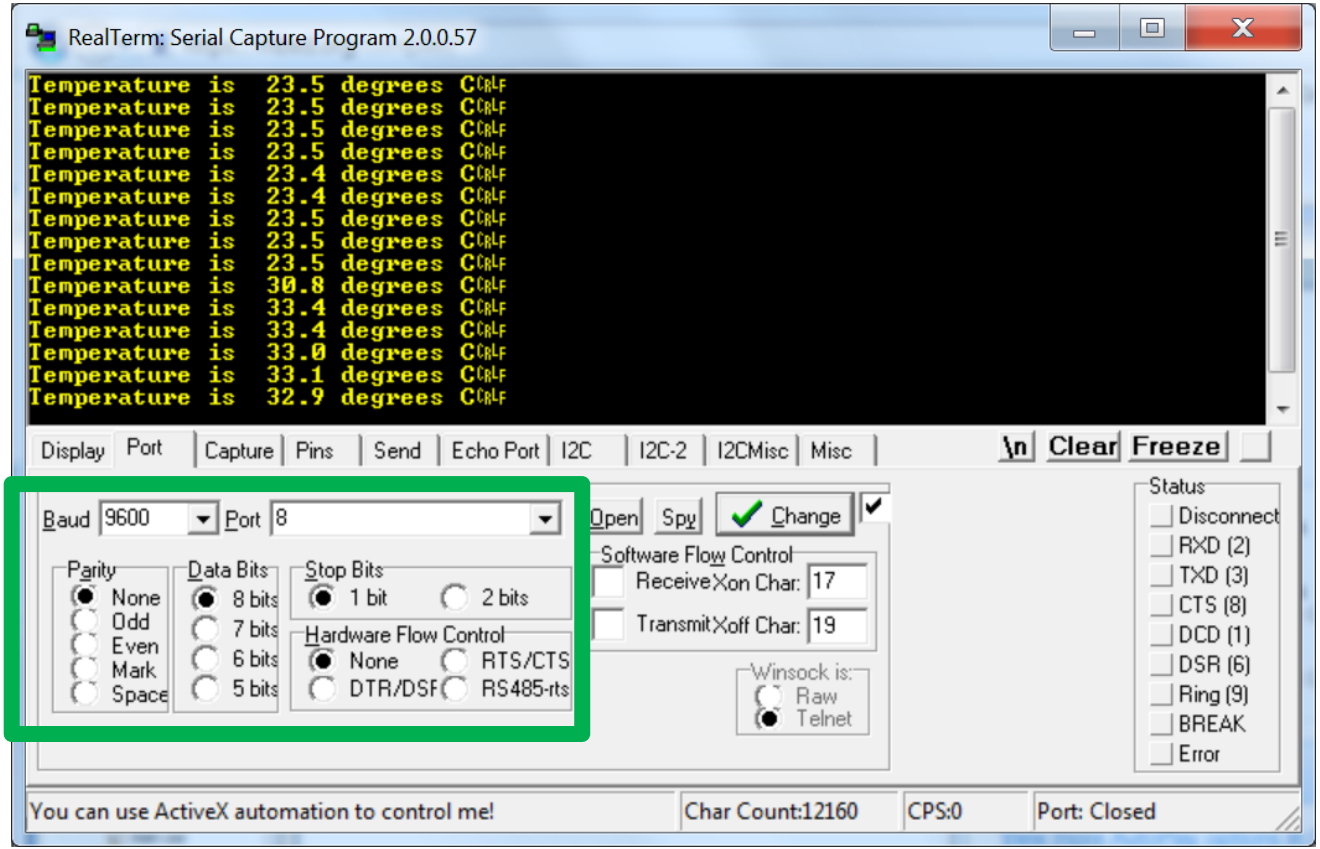
Table 36-6. USCI_A UART Mode Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	UCAxCTLW0	USCI_Ax Control Word 0	Read/write	Word	0001h	
00h	UCAxCTL1	USCI_Ax Control 1	Read/write	Byte	01h	Section 36.4.2
01h	UCAxCTL0	USCI_Ax Control 0	Read/write	Byte	00h	Section 36.4.1
06h	UCAxBRW	USCI_Ax Baud Rate Control Word	Read/write	Word	0000h	
06h	UCAxBR0	USCI_Ax Baud Rate Control 0	Read/write	Byte	00h	Section 36.4.3
07h	UCAxBR1	USCI_Ax Baud Rate Control 1	Read/write	Byte	00h	Section 36.4.4
08h	UCAxMCTL	USCI_Ax Modulation Control	Read/write	Byte	00h	Section 36.4.5
09h		Reserved - reads zero	Read	Byte	00h	
0Ah	UCAxSTAT	USCI_Ax Status	Read/write	Byte	00h	Section 36.4.6
0Bh		Reserved - reads zero	Read	Byte	00h	
0Ch	UCAxRXBUF	USCI_Ax Receive Buffer	Read/write	Byte	00h	Section 36.4.7
0Dh		Reserved - reads zero	Read	Byte	00h	
0Eh	UCAxTXBUF	USCI_Ax Transmit Buffer	Read/write	Byte	00h	Section 36.4.8
0Fh		Reserved - reads zero	Read	Byte	00h	
10h	UCAxABCTL	USCI_Ax Auto Baud Rate Control	Read/write	Byte	00h	Section 36.4.11
11h		Reserved - reads zero	Read	Byte	00h	
12h	UCAxIRCTL	USCI_Ax IrDA Control	Read/write	Word	0000h	
12h	UCAxIRTCTL	USCI_Ax IrDA Transmit Control	Read/write	Byte	00h	Section 36.4.9
13h	UCAxIRRCTL	USCI_Ax IrDA Receive Control	Read/write	Byte	00h	Section 36.4.10
1Ch	UCAxICTL	USCI_Ax Interrupt Control	Read/write	Word	0000h	
1Ch	UCAxIE	USCI_Ax Interrupt Enable	Read/write	Byte	00h	Section 36.4.12
1Dh	UCAxIFG	USCI_Ax Interrupt Flag	Read/write	Byte	00h	Section 36.4.13
1Eh	UCAxIV	USCI_Ax Interrupt Vector	Read	Word	0000h	Section 36.4.14


YA MUESTRA EL MALDITO
CÓDIGO

UART: Terminales

Recuerden: El Handshake es **muchomuyimportante**



IEE2463 Sistemas Electrónicos Programables

Javier Silva Orellana
jisilva8@uc.cl
GitHub: slothzilla328p

2do semestre 2020