1.2)

a) Performance via Pipelining

b) Performance via Parallelism

c) Performance via Prediction

d) Use Abstraction to Simplify Design

e) Hierarchy of Memories

f) Make the Common Case Fast

g) Design for Moore’s Law

h) Dependability via Redundancy

1.4)

a) 3,932,160 bytes/frame minimum

b) 0.3145728 seconds

1.5)

a) P1 = 1 / 2 = .5  
 P2 = 1 / 2.5 = .44

P3 = 2.2 / 4.0 = .55

P2 has the shortest CPU time

b) P1 = 20 Instructions

13.33333 Cycles

P2 =

c)

1.6)

a)

1.8.1 C = 2x(DP)/(V^2 \* F)

1.8.2 ttl diss power = ttl static + ttl dynamic

1.8.3 (Snew + Dnew)/(Sold + Dold) = 0.9

2) Solve for Dnew Capac (formula)

1)Solve for Sold = Vold \* I (Current (Power/Voltage))

3) Vnew

Snew

Dnew