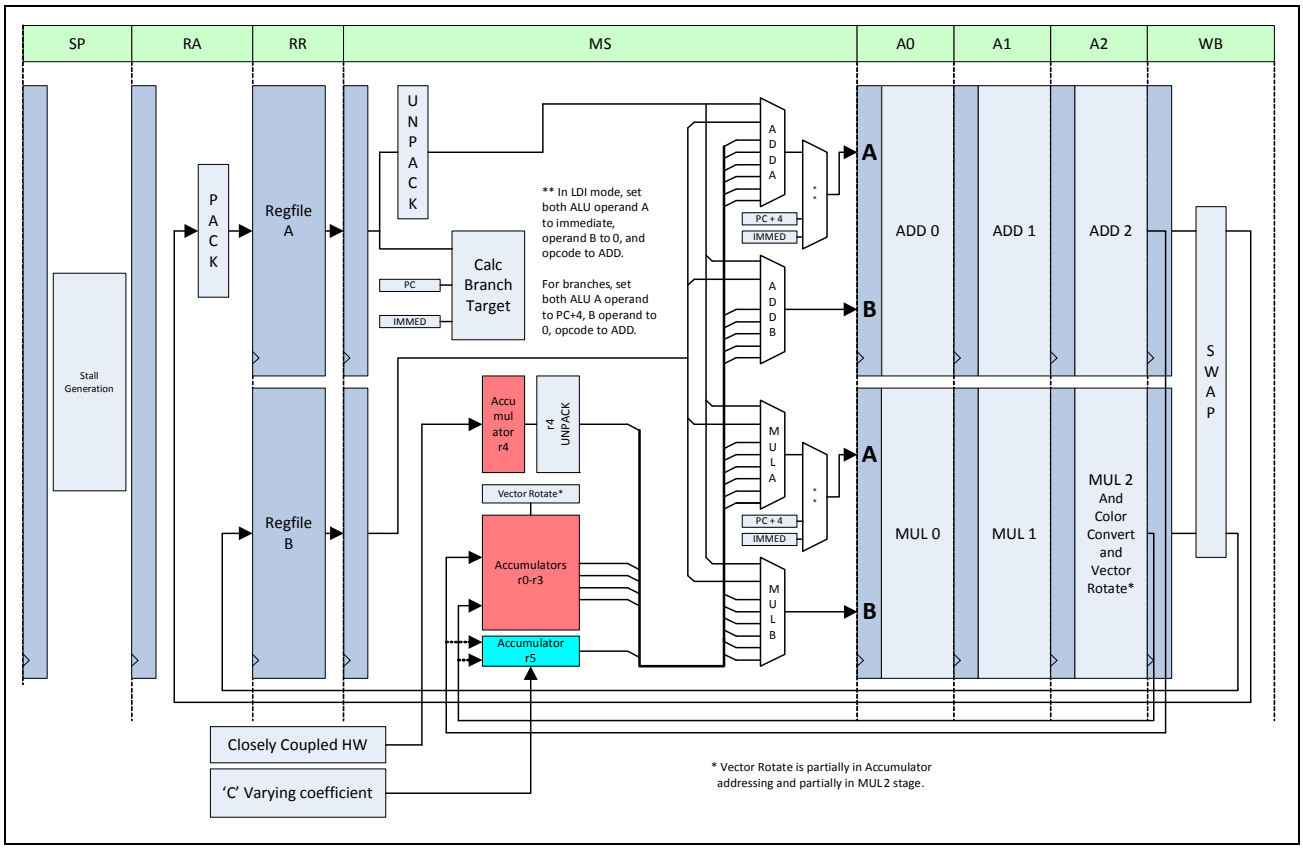
Quad Processor Architecture

Core Pipeline Operation

The front end of each QPU pipeline receives instructions from a shared instruction cache (icache). As one icache unit serves four QPUs in four successive clock cycles the front end pipelines of each of these four QPUs will be at different phases relative to each other. After instruction fetch there is a 're-synchronisation' pipeline stage which brings all of the QPUs into phase with each other. The re-synchronised parts of the QPU pipeline are shown in Figure 2 along with the names assigned to each pipeline stage.

Figure 2: QPU Core Pipeline



Processor Registers

The QPU contains two sets of physical registers consisting of a set of four general-purpose accumulators, two special-purpose accumulators, and two large register-file memories. The register space associated with each of the A and B regfiles can address 64 locations, 32 of these are backed by the physical registers while the other 32 are used to access register-space I/O.