## **Section 2: Architecture Overview**

Figure 1 shows the system block diagram for VideoCore IV 3D.

Control Lists **Control List Executor** Primitives [CLE] State Change Data (to fifos) General DMA Write Data VPM DMA Writer [VDW] Vertex Attributes/ Vertex Cache Manager & DMA General DMA Read Data [VCM and VCD] Clipped Primitives Vertex Attributes / Pre-shaded Vertices / General DMA Read Data Primitive Tile Binner Tile Lists (primitives & state) [PTB] Clipped Primitives Primitive Setup Engine [PSE] Front End Pipe [FEP] (Rasteriser, Early-Z, Z, W interp, 1/W) Vertex Shade Req Coverage Accumulate AXI Pipe [CAP] ARB Coverage QPU Scheduler Vertex Pipe [QPS] Memory [VPM] Frame Buffer Data Scoreboard & shaded Quad Z, vertices Colour Slice 0 Interpolator [VRI] Quad Processor QPU 0, 0 Coeffs Mem | Functions Unit [SFU] QPU 0, 1 Uniforms Cache [QUC] QPU 0, 2 Special Icache [QIC] QPU 0, 3 Texture and Memory Lookup Unit [TMU] **\*** L2 Cache [L2C] Slice 1 Slice 2 Slice 3

Figure 1: VideoCore® IV 3D System Block Diagram