

Figure 1: VideoCore® IV 3D System Block Diagram

The diagram illustrates the VideoCore® IV 3D System Block Diagram. The system is organized into several key components and data paths:

- AXI ARB:** The central interface for the system, connected to the L2 Cache and the Control List Executor (CLE).
- Control List Executor (CLE):** Receives Control Lists and State Change Data (to fifos) from the AXI ARB. It outputs Primitives to the VPM DMA Writer (VDW) and the Primitive Tile Binner (PTB).
- VPM DMA Writer (VDW) and Vertex Cache Manager & DMA (VCM and VCD):** These components handle General DMA Write Data and Vertex Attributes/General DMA Read Data. They are connected to the AXI ARB and the VPM DMA Writer (VDW).
- Primitive Tile Binner (PTB):** Receives Clipped Primitives and Tile Lists (primitives & state) from the AXI ARB. It outputs Prims to the Primitive Setup Engine (PSE).
- Primitive Setup Engine (PSE):** Receives Clipped Primitives from the AXI ARB. It outputs Fragment Shade Req, Vertex Shade Req, and General Program Req to the QPU Scheduler (QPS).
- Front End Pipe (FEP):** (Rasteriser, Early-Z, Z, W interp, 1/W). It receives data from the PSE and outputs Quad XX Flags-Z, 1/W to the Scoreboard.
- Coverage Accumulate Pipe (CAP):** Receives data from the FEP and outputs Quad Z, Colour to the Scoreboard.
- Scoreboard:** Receives data from the FEP and CAP. It outputs Varying Interpolation Coefficients to the Interpolator (VRI) and Frame Buffer Data to the AXI ARB.
- Interpolator (VRI) and Coeffs Mem:** These components handle Varying Interpolation Coefficients and Quad Z, Colour data.
- Uniforms Cache (QUC), Icache (QIC), and Texture and Memory Lookup Unit (TMU):** These components are connected to the L2 Cache and the Interpolator (VRI).
- QPU Scheduler (QPS):** Receives data from the PSE and outputs Start PC to the Quad Processor (QPU).
- Quad Processor (QPU):** Consists of multiple slices (Slice 0, Slice 1, Slice 2, Slice 3). Each slice contains a Quad Processor (QPU 0, 0, QPU 0, 1, QPU 0, 2, QPU 0, 3) and a Special Functions Unit (SFU).
- Vertex Pipe Memory (VPM):** Receives data from the QPU Scheduler (QPS) and outputs Unshaded & shaded vertices and General Data to the Quad Processor (QPU).
- L2 Cache (L2C):** Connected to the AXI ARB and the Uniforms Cache (QUC), Icache (QIC), and Texture and Memory Lookup Unit (TMU).

Figure 1: VideoCore® IV 3D System Block Diagram

The diagram illustrates the VideoCore® IV 3D System Block Diagram, showing the flow of data and control signals between various components across four slices (0, 1, 2, 3).

Key Components and Data Flow:

- Control Lists:** Input to the Control List Executor [CLE].
- State Change Data (to fifos):** Input to the VPM DMA Writer [VDW].
- General DMA Write Data:** Input to the VPM DMA Writer [VDW].
- Vertex Attributes/General DMA Read Data:** Input to the Vertex Cache Manager & DMA [VCM and VCD].
- Clipped Primitives:** Input to the Primitive Tile Binner [PTB] and the Primitive Setup Engine [PSE].
- Tile Lists (primitives & state):** Input to the Primitive Tile Binner [PTB].
- Primitive Setup Engine [PSE]:** Outputs to the Front End Pipe [FEP] (Rasteriser, Early-Z, Z, W interp, 1/W).
- Front End Pipe [FEP]:** Outputs to the Coverage Accumulate Pipe [CAP] and the QPU Scheduler [QPS].
- Coverage Accumulate Pipe [CAP]:** Outputs to the Scoreboard.
- Scoreboard:** Outputs to the Interpolator [VRI] and the Coeffs Mem.
- Interpolator [VRI]:** Outputs to the Uniforms Cache [QUC], Icache [QIC], and Texture and Memory Lookup Unit [TMU].
- Coeffs Mem:** Outputs to the Uniforms Cache [QUC], Icache [QIC], and Texture and Memory Lookup Unit [TMU].
- Uniforms Cache [QUC]:** Outputs to the Icache [QIC] and Texture and Memory Lookup Unit [TMU].
- Icache [QIC]:** Outputs to the Texture and Memory Lookup Unit [TMU].
- Texture and Memory Lookup Unit [TMU]:** Outputs to the QPU Scheduler [QPS].
- L2 Cache [L2C]:** Outputs to the Uniforms Cache [QUC], Icache [QIC], and Texture and Memory Lookup Unit [TMU].
- QPU Scheduler [QPS]:** Outputs to the Vertex Pipe Memory [VPM] and the Quad Processor QPU 0, 0, QPU 0, 1, QPU 0, 2, and QPU 0, 3.
- Vertex Pipe Memory [VPM]:** Outputs to the Quad Processor QPU 0, 0, QPU 0, 1, QPU 0, 2, and QPU 0, 3.
- Quad Processor QPU 0, 0, QPU 0, 1, QPU 0, 2, and QPU 0, 3:** Outputs to the Special Functions Unit [SFU].
- Special Functions Unit [SFU]:** Outputs to the Quad Processor QPU 0, 0, QPU 0, 1, QPU 0, 2, and QPU 0, 3.

The diagram also shows the flow of data between the L2 Cache and the Uniforms Cache, Icache, and Texture and Memory Lookup Unit.

