ISL9110, ISL9112

1.2A High Efficiency Buck-Boost Regulators

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Rev.3.00
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The ISL9110 and ISL9112 are highly-integrated buck-boost switching regulators that accept input voltages either above or below the regulated output voltage. Unlike other Buck-Boost regulators, these regulators automatically transition between operating modes without significant output disturbance.

Both parts are capable of delivering up to 1.2A output current, and provide excellent efficiency due to their fully synchronous 4-switch architecture. No-load quiescent current of only 35µA also optimizes efficiency under light-load conditions. Forced PWM and/or synchronization to an external clock may also be selected for noise sensitive applications.

The ISL9110 is designed for standalone applications and supports 3.3V and 5V fixed output voltages or variable output voltages with an external resistor divider. Output voltages as low as 1V, or as high as 5.2V are supported using an external resistor divider.

The ISL9112 supports a broader set of programmable features that may be accessed using an I^2C bus interface. With a programmable output voltage range of 1.9V to 5V, the ISL9112 is ideal for applications requiring dynamically changing supply voltages. A programmable slew rate can be selected to provide smooth transitions between output voltage settings.

The ISL9110 and ISL9112 require only a single inductor and very few external components. Power supply solution size is minimized by a tiny 3mmx3mm package and a 2.5MHz switching frequency, which further reduces the size of external components.

Features

- Accepts input voltages above or below regulated output voltage
- Automatic and seamless transitions between Buck and Boost modes
- Input voltage range: 1.8V to 5.5V
- Output current: Up to 1.2A
- High efficiency: Up to 95%
- 35µA quiescent current maximizes light-load efficiency
- 2.5MHz switching frequency minimizes external component size
- Selectable Forced PWM mode and external synchronization
- I^2C Interface (ISL9112)
- Fully protected for overcurrent, over-temperature, and undervoltage
- Small 3mmx3mm TDFN Package

Applications

- Regulated 3.3V from a single Li-ion battery
- Smart phones and tablet computers
- Handheld devices
- Point-of-load regulators

Related Literature

For a full list of related documents, visit our website

- ISL9110, ISL9112 product pages

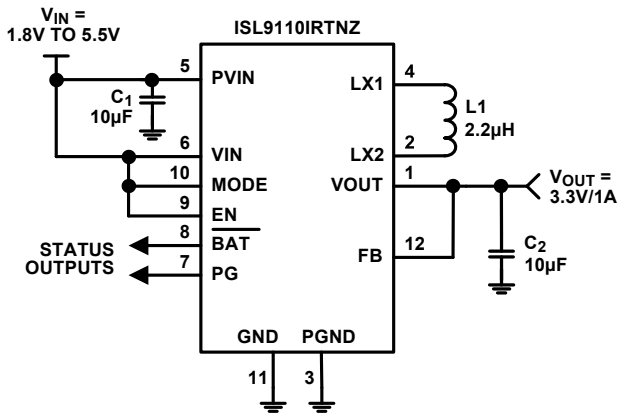

FIGURE 1. TYPICAL APPLICATION

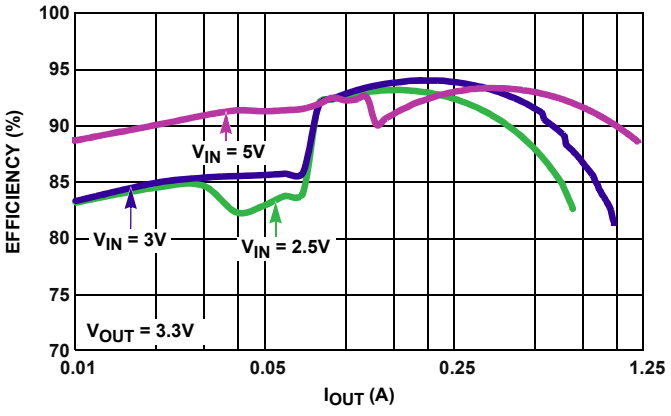

FIGURE 2. EFFICIENCY

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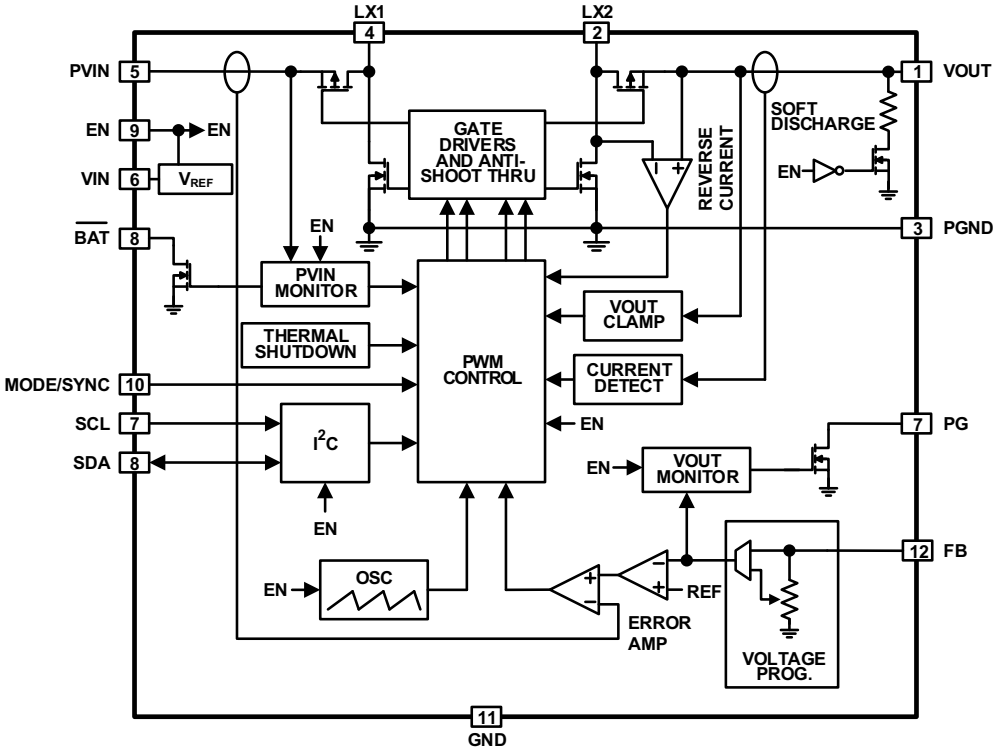
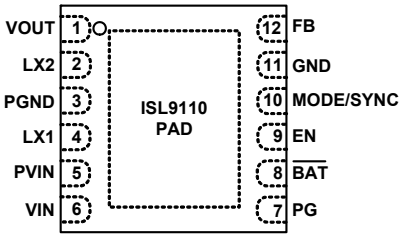
Block Diagram

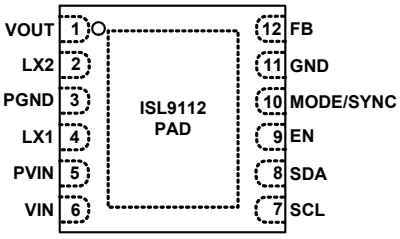


Pin Configurations

ISL9110
(12 LD TDFN)
TOP VIEW



ISL9112
(12 LD TDFN)
TOP VIEW



Pin Descriptions

PIN #	ISL9110	ISL9112	DESCRIPTION
1	VOUT	VOUT	Buck/boost output. Connect a 10µF capacitor to PGND.
2	LX2	LX2	Inductor connection, output side.
3	PGND	PGND	Power ground for high switching current.
4	LX1	LX1	Inductor connection, input side.
5	PVIN	PVIN	Power input. Range: 1.8V to 5.5V. Connect a 10µF capacitor to PGND.
6	VIN	VIN	Supply input. Range: 1.8V to 5.5V.
7	PG	-	Open-drain output. Provides output power-good status.
	-	SCL	Logic input, I^2C clock.
8	$\overline{BAT}$	-	Open drain output. Provides input-power-good status.
	-	SDA	Logic I/O, open drain, I^2C data.
9	EN	EN	Logic input, drive high to enable device.
10	MODE / SYNC	MODE / SYNC	Logic input, high for auto PFM mode. Low for forced PWM operation. External clock sync input. Range: 2.75MHz to 3.25MHz.
11	GND	GND	Analog ground pin.
12	FB	FB	Voltage feedback pin.
PAD	PAD	PAD	Exposed pad; connect to PGND.

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	V_{OUT} (V)	HICCUP MODE	TEMP RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE	PKG. DWG. #
ISL9110IRTNZ	GASA	3.3	Enabled	-40 to +85	-	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110IRTNZ-T	GASA	3.3	Enabled	-40 to +85	6k	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110IRTNZ-T7A	GASA	3.3	Enabled	-40 to +85	250	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110IRT7Z	GATA	5.0	Enabled	-40 to +85	-	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110IRT7Z-T	GATA	5.0	Enabled	-40 to +85	6k	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110IRT7Z-T7A	GATA	5.0	Enabled	-40 to +85	250	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110IRTAZ	GAUA	ADJ.	Enabled	-40 to +85	-	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110IRTAZ-T	GAUA	ADJ.	Enabled	-40 to +85	6k	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110IRTAZ-T7A	GAUA	ADJ.	Enabled	-40 to +85	250	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9112IRTNZ	GAVA	3.3	Enabled	-40 to +85	-	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9112IRTNZ-T	GAVA	3.3	Enabled	-40 to +85	6k	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9112IRTNZ-T7A	GAVA	3.3	Enabled	-40 to +85	250	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9112IRT7Z	GAWA	5.0	Enabled	-40 to +85	-	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9112IRT7Z-T	GAWA	5.0	Enabled	-40 to +85	6k	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9112IRT7Z-T7A	GAWA	5.0	Enabled	-40 to +85	250	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110BIRTAZ	GBAF	ADJ.	Disabled	-40 to +85	-	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C
ISL9110BIRTAZ-T	GBAF	ADJ.	Disabled	-40 to +85	6k	12 Ld Exposed Pad 3x3 TDFN	L12.3x3C

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL9110, ISL9112 product information pages. For more information about MSL, see TB363.
4. The ISL9110 and ISL9112 can be special ordered with any output voltage between 1.9V and 5.0V in 100mV steps.

Absolute Maximum Ratings

PVIN, VIN . . . . . -0.3V to 6.5V
LX1, LX2 (Note 7) . . . . . -0.3V to 6.5V
FB (Adjustable version) . . . . . -0.3V to 2.7V
FB (Fixed V_{OUT} versions) . . . . . -0.3V to 6.5V
GND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A) 250V
Latch-Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
12 Ld TDFN Package (Notes 5, 6)	42	5.5

Maximum Junction Temperature (Plastic Package) . . . . . +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range . . . . . 1.8V to 5.5V
Load Current Range . . . . . 0A to 1.2A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. LX1 and LX2 pins can withstand switching transients of -1.5V for 100ns, and 7V for 20ms.

Analog Specifications

$V_{VIN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, L1 = 2.2µH, $C_1 = C_2 = 10µF$, $T_A = +25°C$. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP (Note 9)	MAX (Note 8)	UNIT
POWER SUPPLY						
Input Voltage Range	V_{IN}		**1.8**		**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising		1.725	**1.775**	V
		Falling	**1.550**	1.650		V
V_{IN} Supply Current	I_{VIN}	PFM mode, no external load on Vout (Note 10)		35	**60**	µA
V_{IN} Supply Current, Shutdown	I_{SD}	EN = GND, V_{IN} = 3.6V		0.05	**1.0**	µA
OUTPUT VOLTAGE REGULATION						
Output Voltage Range	V_{OUT}	ISL9110IRTAZ, I_{OUT} = 100mA	**1.00**		**5.20**	V
		ISL9112, I_{OUT} = 100mA	**1.90**		**5.00**	V
Output Voltage Accuracy		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 0mA, PWM mode	**-2**		**+2**	%
		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
FB Pin Voltage Regulation	V_{FB}	For adjustable output version	**0.79**	0.80	**0.81**	V
FB Pin Bias Current	I_{FB}	For adjustable output version			**1**	µA
Line Regulation, PWM Mode	$\Delta V_{OUT} / \Delta V_{IN}$	I_{OUT} = 500mA, V_{OUT} = 3.3V, MODE = GND, V_{IN} step from 2.3V to 5.5V		±0.005		mV/mV
Load Regulation, PWM Mode	$\Delta V_{OUT} / \Delta I_{OUT}$	V_{IN} = 3.7V, V_{OUT} = 3.3V, MODE = GND, I_{OUT} step from 0mA to 500mA		±0.005		mV/mA
Line Regulation, PFM Mode	$\Delta V_{OUT} / \Delta V_I$	I_{OUT} = 100mA, V_{OUT} = 3.3V, MODE = VIN, V_{IN} step from 2.3V to 5.5V		±12.5		mV/V
Load Regulation, PFM Mode	$\Delta V_{OUT} / \Delta I_{OUT}$	V_{IN}=3.7V, V_{OUT} = 3.3V, MODE = VIN, I_{OUT} step from 0mA to 100mA		±0.4		mV/mA
Output Voltage Clamp	V_{CLAMP}	Rising, V_{IN} = 3.6V	**5.25**		**5.95**	V
Output Voltage Clamp Hysteresis		V_{IN} = 3.6V		400		mV
DC/DC SWITCHING SPECIFICATIONS						
Oscillator Frequency	f_{SW}		**2.25**	2.50	**2.75**	MHz

Analog Specifications $V_{VIN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, L1 = 2.2µH, $C_1 = C_2 = 10µF$, $T_A = +25°C$. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP (Note 9)	MAX (Note 8)	UNIT
Minimum On Time	t_{ONMIN}			80		ns
LX1 Pin Leakage Current	$I_{PFETLEAK}$		**-1**		**1**	µA
LX2 Pin Leakage Current	$I_{NFETLEAK}$		**-1**		**1**	µA
SOFT-START and SOFT DISCHARGE						
Soft-Start Time	t_{SS}	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Buck mode. $V_{IN} = 4V$, $V_{OUT} = 3.3V$, $I_O = 200mA$		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Boost mode. $V_{IN} = 2V$, $V_{OUT} = 3.3V$, $I_O = 200mA$		2		ms
VOUT Soft-Discharge ON-Resistance	R_{DISCHG}	$V_{IN} = 3.6V$, EN < VIL		120		Ω
POWER MOSFET						
P-Channel MOSFET ON-Resistance	R_{DSON_P}	$V_{IN} = 3.6V$, $I_O = 200mA$		0.12	**0.17**	Ω
		$V_{IN} = 2.5V$, $I_O = 200mA$		0.15	**0.23**	Ω
N-Channel MOSFET ON-Resistance	R_{DSON_N}	$V_{IN} = 3.6V$, $I_O = 200mA$		0.10	**0.15**	Ω
		$V_{IN} = 2.5V$, $I_O = 200mA$		0.13	**0.23**	Ω
P-Channel MOSFET Peak Current Limit	I_{PK_LMT}	$V_{IN} = 3.6V$	**2.0**	2.4	**2.8**	A
PFM/PWM TRANSITION						
Load Current Threshold, PFM to PWM		$V_{IN} = 3.6V$, $V_{OUT} = 3.3V$		200		mA
Load Current Threshold, PWM to PFM		$V_{IN} = 3.6V$, $V_{OUT} = 3.3V$		75		mA
External Synchronization Frequency Range			**2.75**		**3.25**	MHz
Thermal Shutdown				155		°C
Thermal Shutdown Hysteresis				30		°C
BATTERY MONITOR AND POWER GOOD COMPARATORS						
Battery Monitor Voltage Threshold	VT_{BMON}		**1.85**	2.0	**2.15**	V
Battery Monitor Voltage Hysteresis	VH_{BMON}			100		mV
Battery Monitor Debounce Time	t_{BMON}			25		µs
PG Delay Time (Rising)				1		ms
PG Delay Time (Falling)				20		µs
Minimum Supply Voltage for Valid PG Signal		EN = V_{IN}	**1.2**			V
PG Range - Lower (Rising)	PG_{RNGLR}	Percentage of programmed voltage		90		%
PG Range - Lower (Falling)	PG_{RNGLF}	Percentage of programmed voltage		87		%
PG Range - Upper (Rising)	PG_{RNGUR}	Percentage of programmed voltage		112		%
PG Range - Upper (Falling)	PG_{RNGUF}	Percentage of programmed voltage		110		%
Compliance Voltage - PG, $\overline{BAT}$		$V_{IN} = 3.6V$, $I_{SINK} = 1µA$			**0.3**	V

Analog Specifications $V_{VIN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, L1 = 2.2µH, $C_1 = C_2 = 10µF$, $T_A = +25°C$. Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP (Note 9)	MAX (Note 8)	UNIT
LOGIC INPUTS						
Input Leakage	I_{LEAK}			0.05	**1**	µA
Input HIGH Voltage	V_{IH}		**1.4**			V
Input LOW Voltage	V_{IL}				**0.4**	V

I^2C Interface Timing Specification For SCL, and SDA pins, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS (Note 11)	MIN (Note 8)	TYP (Note 9)	MAX (Note 8)	UNIT
Pin Capacitance	C_{pin}				15	pF
SCL Frequency	f_{SCL}				400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{sp}	Any pulse narrower than the max spec is suppressed			50	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling edge crossing V_{IL}, until SDA exits the V_{IL} to V_{IH} window			900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing V_{IH} during a STOP condition, to SDA crossing V_{IH} during the following START condition	1300			ns
Clock LOW Time	t_{LOW}	Measured at the V_{IL} crossings	1300			ns
Clock HIGH Time	t_{HIGH}	Measured at the V_{IH} crossings	600			ns
START Condition Set-Up Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge; both crossing V_{IH}	600			ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing V_{IL} to SCL falling edge crossing V_{IH}	600			ns
Input Data Set-Up Time	$t_{SU:DAT}$	From SDA exiting the V_{IL} to V_{IH} window, to SCL rising edge crossing V_{IL}	100			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL rising edge crossing V_{IH} to SDA entering the V_{IL} to V_{IH} window	0			ns
STOP Condition Set-Up Time	$t_{SU:STO}$	From SCL rising edge crossing V_{IH}, to SDA rising edge crossing V_{IL}	600			ns
STOP Condition Hold Time for Read, or Volatile Only Write	$t_{HD:STO}$	From SDA rising edge to SCL falling edge; both crossing V_{IH}	1300			ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing V_{IL}, until SDA enters the V_{IL} to V_{IH} window	0			ns
SDA and SCL Rise Time	t_R	From V_{IL} to V_{IH}	20 + 0.1 x Cb		250	ns
SDA and SCL Fall Time	t_F	From V_{IH} to V_{IL}	20 + 0.1 x Cb		250	ns
Capacitive Loading of SDA or SCL	Cb	Total on-chip and off-chip	10		400	pF
SDA and SCL Bus Pull-Up Resistor Off-Chip	Rpu	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ~2.5kΩ For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Typical values are for $T_A = +25°C$ and $V_{IN} = 3.6V$.
10. Quiescent current measurements are taken when the output is not switching.
11. ISL9112 only. Limits established by characterization and are not production tested.

Typical Performance Curves

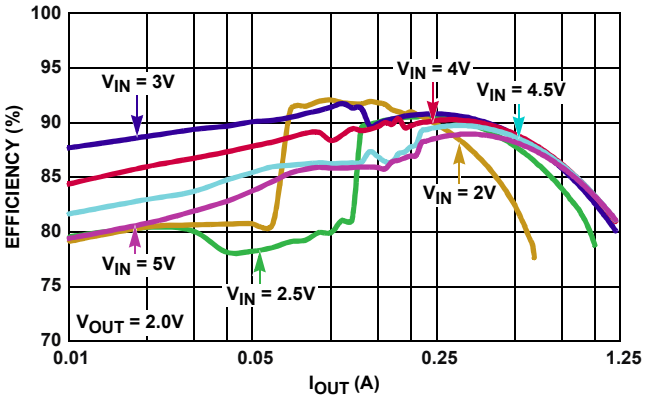


FIGURE 3. EFFICIENCY vs OUTPUT CURRENT, V_{OUT} = 2V

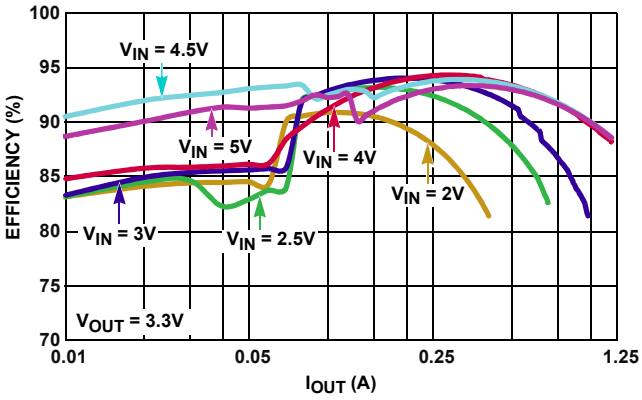


FIGURE 4. EFFICIENCY vs OUTPUT CURRENT, V_{OUT} = 3.3V

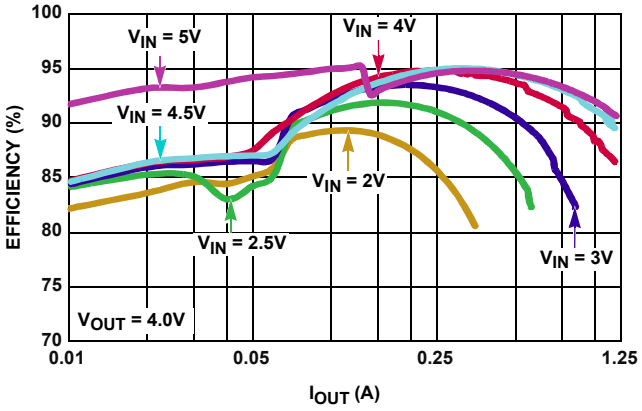


FIGURE 5. EFFICIENCY vs OUTPUT CURRENT, V_{OUT} = 4V

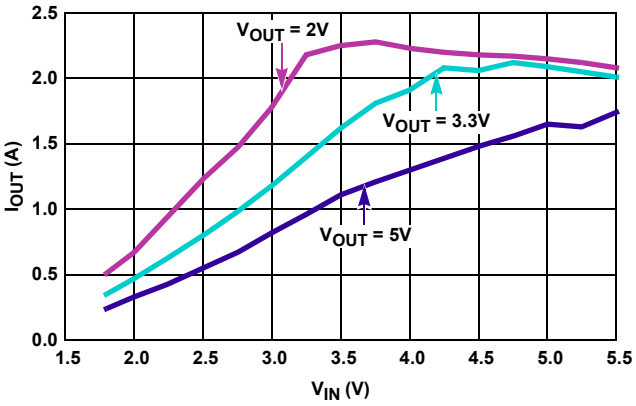


FIGURE 6. MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE

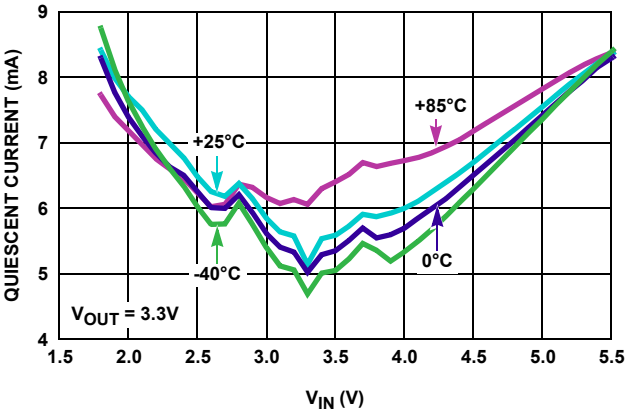


FIGURE 7. PWM MODE QUIESCENT CURRENT, V_{OUT} = 3.3V, NO LOAD

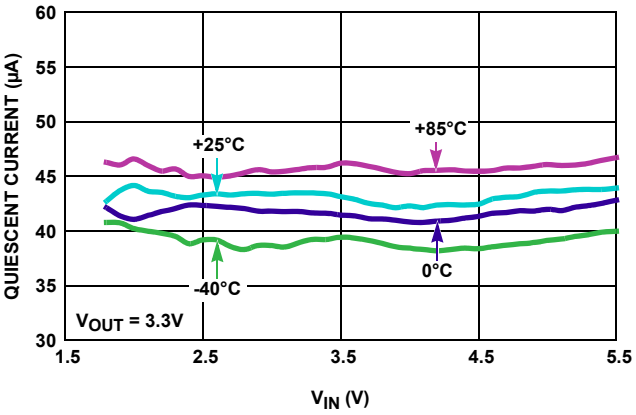


FIGURE 8. PFM MODE QUIESCENT CURRENT, V_{OUT} = 3.3V, NO LOAD

Typical Performance Curves (Continued)

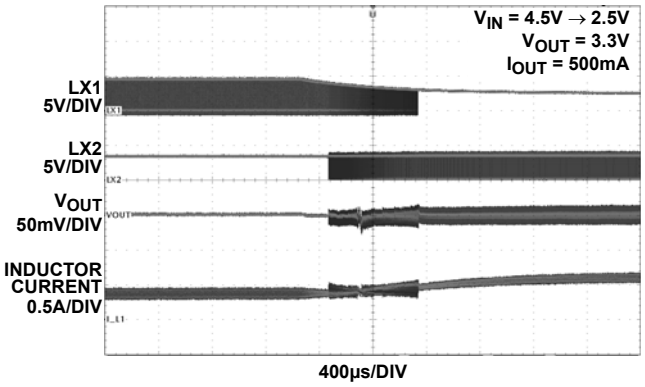


FIGURE 9. STEADY STATE TRANSITION FROM BUCK TO BOOST

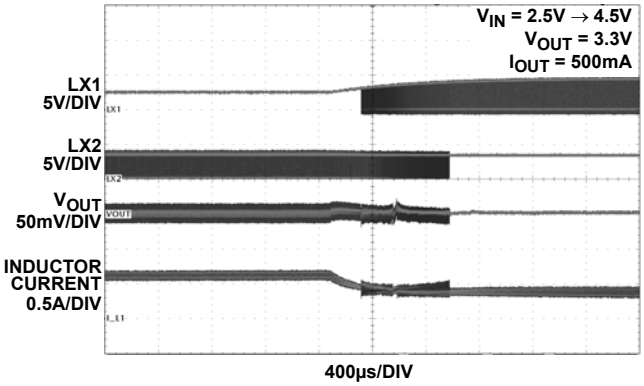


FIGURE 10. STEADY STATE TRANSITION FROM BOOST TO BUCK

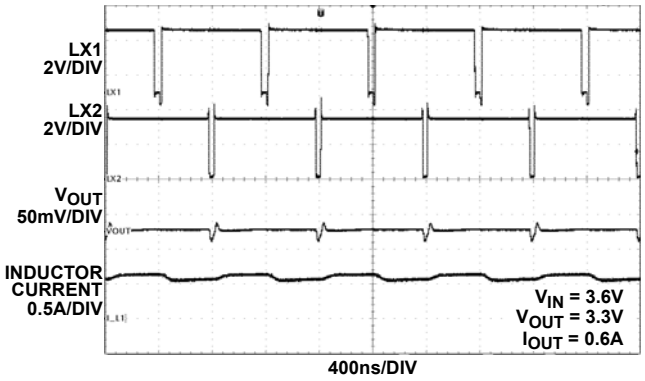


FIGURE 11. STEADY STATE V_{IN} NEAR V_{OUT}

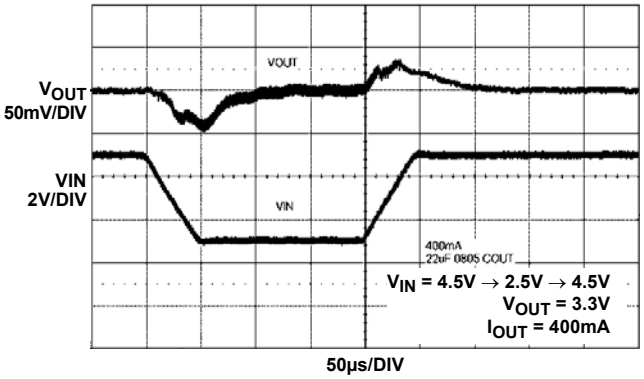


FIGURE 12. INPUT TRANSIENT

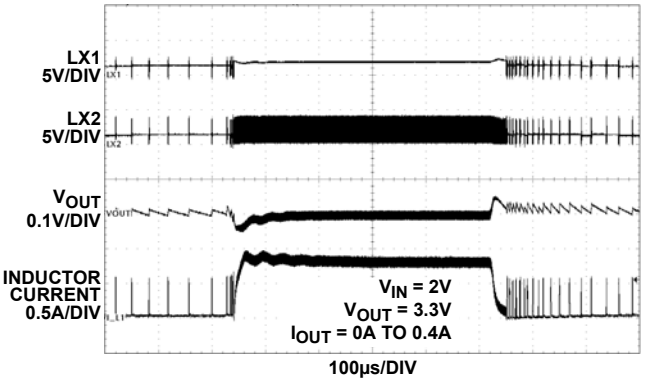


FIGURE 13. TRANSIENT LOAD RESPONSE

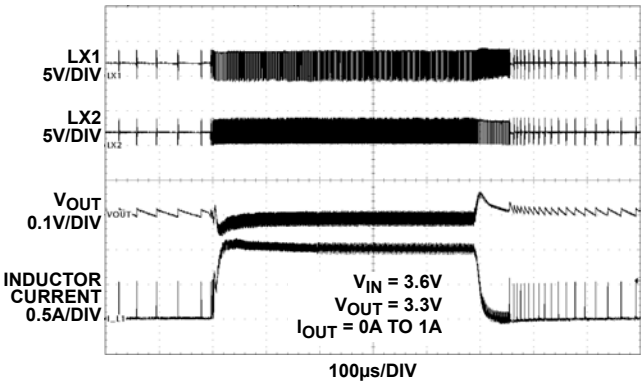


FIGURE 14. TRANSIENT LOAD RESPONSE

Typical Performance Curves (Continued)

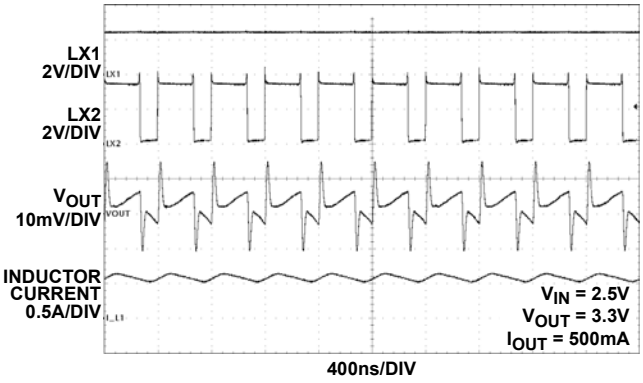


FIGURE 15. SWITCHING WAVEFORMS, BOOST MODE

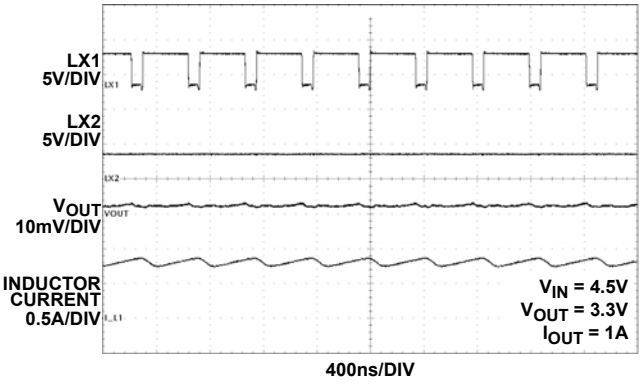


FIGURE 16. SWITCHING WAVEFORMS, BUCK MODE

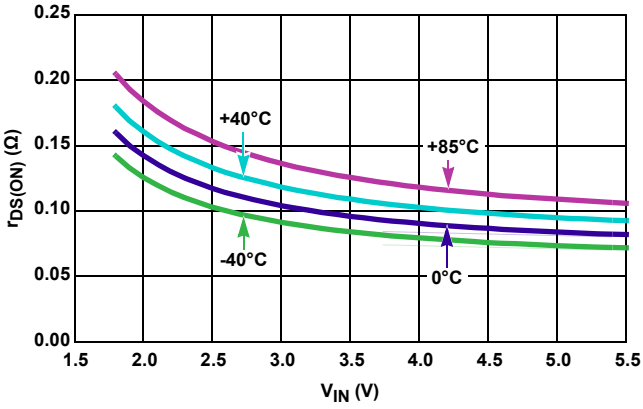


FIGURE 17. NFET $R_{DS(ON)}$ vs INPUT VOLTAGE

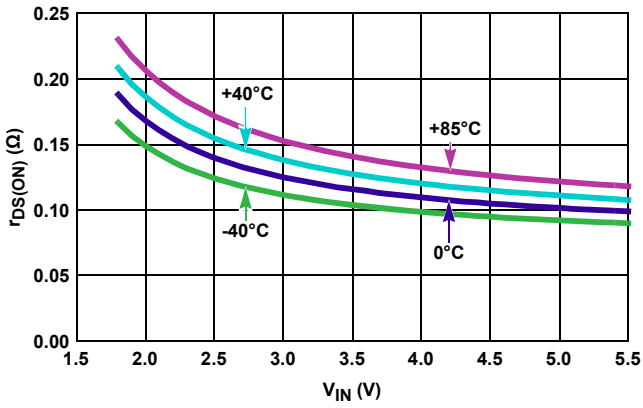


FIGURE 18. PFET $R_{DS(ON)}$ vs INPUT VOLTAGE

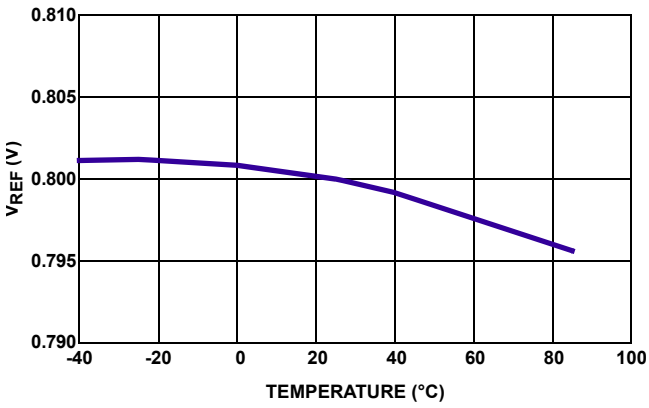


FIGURE 19. V_{REF} vs TEMPERATURE, T_A = -40°C TO +85°C

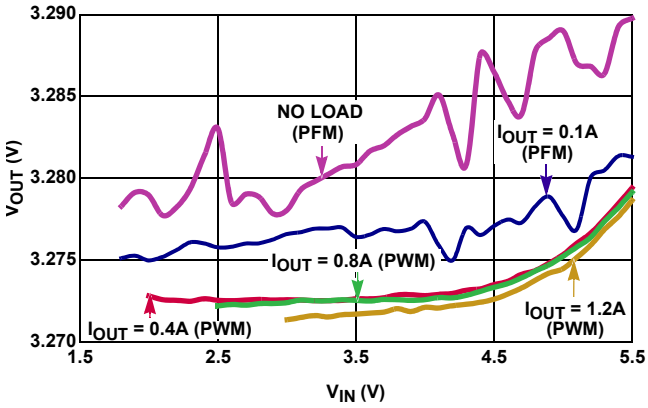


FIGURE 20. OUTPUT VOLTAGE vs V_{IN} VOLTAGE (V_{OUT} = 3.3V)

Typical Performance Curves (Continued)

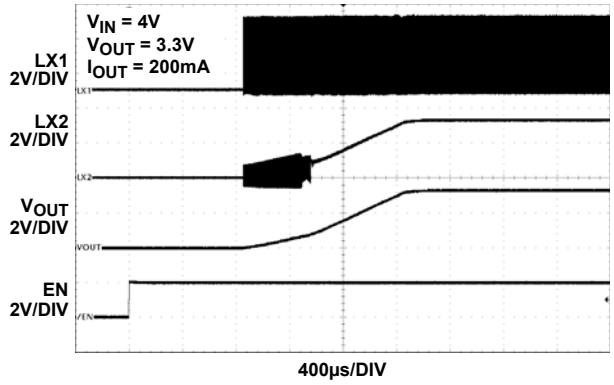


FIGURE 21. SOFT-START, V_{IN} = 4V, V_{OUT} = 3.3V

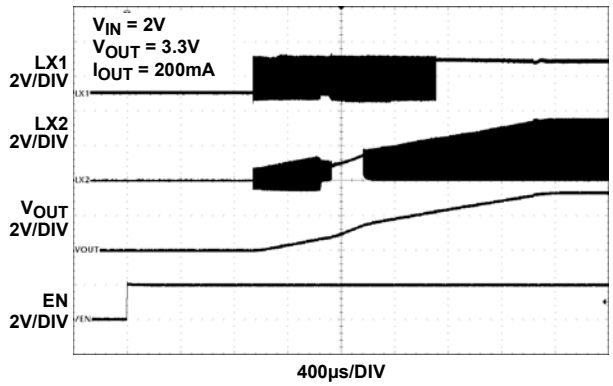


FIGURE 22. SOFT-START, V_{IN} = 2V, V_{OUT} = 3.3V

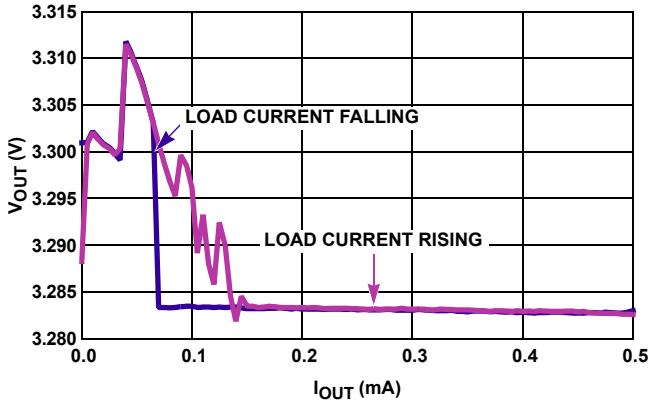


FIGURE 23. OUTPUT VOLTAGE vs LOAD CURRENT (V_{IN} = 2.5V, V_{OUT} = 3.3V, AUTO PFM/PWM MODE)

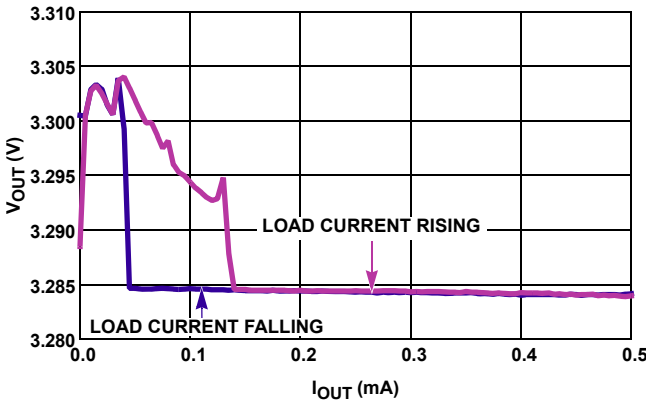


FIGURE 24. OUTPUT VOLTAGE vs LOAD CURRENT (V_{IN} = 4.5V, V_{OUT} = 3.3V, AUTO PFM/PWM MODE)

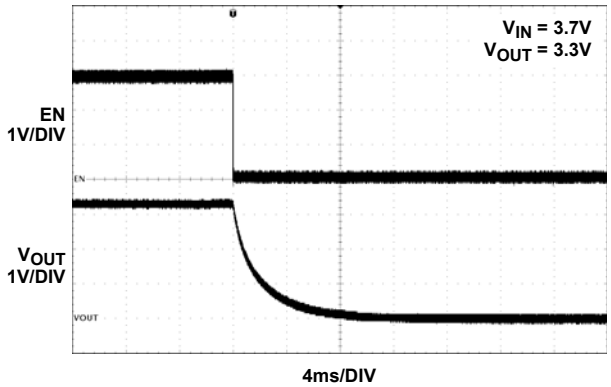


FIGURE 25. OUTPUT SOFT-DISCHARGE

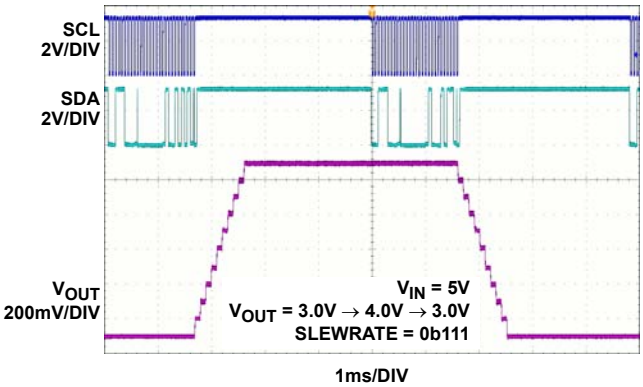


FIGURE 26. DIGITAL SLEW OPERATION (ISL9112)

Functional Description

Functional Overview

Refer to the "Block Diagram" on page 3. The ISL9110 and ISL9112 implement a complete buck boost switching regulator, with PWM controller, internal switches, references, protection circuitry, and control inputs.

The PWM controller automatically switches between Buck and Boost modes as necessary to maintain a steady output voltage, with changing input voltages and dynamic external loads.

The ISL9110 provides output power-good and input power-good open-drain status outputs on Pins 7 and 8. In the ISL9112, these pins are used for an I^2C interface, allowing programmable output voltage and access to the ultrasonic mode and slew rate limit control bits.

Internal Supply and References

Referring to the "Block Diagram" on page 3, the ISL9110 and ISL9112 provide two power input pins. The PVIN pin supplies input power to the DC/DC converter, while the VIN pin provides operating voltage source required for stable V_{REF} generation. Separate ground pins (GND and PGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

A master enable pin EN allows the device to be enabled. Driving EN low invokes a power-down mode, where most internal device functions, including input and output power good detection, are disabled.

Soft Discharge

When the device is disabled by driving EN low, an internal resistor between VOUT and GND is activated. This internal resistor has typical 120Ω resistance.

POR Sequence and Soft-Start

Bringing the EN pin high allows the device to power-up. A number of events occur during the start-up sequence. The internal voltage reference powers up, and stabilizes. The device then starts operating. There is a typical 1ms delay between assertion of the EN pin and the start of switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping V_{OUT} voltage. While output voltage is lower than approximately 20% of the target output voltage, switching frequency is reduced to a fraction of the normal switching frequency to aid in producing low duty cycles necessary to avoid input inrush current spikes. When the output voltage exceeds 20% of the target voltage, switching frequency is increased to its nominal value.

When the target output voltage is higher than the input voltage, there is a transition from Buck mode to Boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

The V_{OUT} ramp time is not constant for all operating conditions. Soft-start into Boost mode takes longer than soft-start into Buck mode. The total soft-start time into Buck mode is typically 2ms, whereas the typical soft-start time into Boost mode is typically 3ms. Increasing the load current increases these typical soft-start times.

Overcurrent Protection

When the current in the P-channel MOSFET is sensed to reach the current limit for 16 consecutive switching cycles, the internal protection circuit is triggered, and switching is stopped for approximately 20ms. The device then performs a soft-start cycle. If the external output overcurrent condition exists after the soft-start cycle, the device detects 16 consecutive switching cycles reaching the peak current threshold. The process repeats as long as the external overcurrent condition is present. This behavior is called 'Hiccup mode'.

Short-Circuit Protection

The ISL9110 and ISL9112 provides short-circuit protection by monitoring the feedback voltage. When feedback voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-channel MOSFET peak current limit remains active during this state.

Undervoltage Lockout

The Undervoltage Lockout (UVLO) feature prevents abnormal operation in the event that the supply voltage is too low to ensure proper operation. When the V_{IN} voltage falls below the UVLO threshold, the regulator is disabled.

PG Status Output (ISL9110 only)

An open-drain output power-good signal is provided in the ISL9110. An internal window comparator detects when V_{OUT} is significantly higher or lower than the target output voltage. The PG output is driven low when sensed V_{OUT} voltage is outside of this 'power-good' window. When V_{OUT} voltage is inside the 'power-good' window, the PG pin goes Hi-Z.

The PG detection circuit detects this condition by monitoring voltage on the FB pin. Hysteresis is provided for the upper and lower PG thresholds to avoid oscillation of the PG output.

$\overline{BAT}$ Status Output (ISL9110 only)

The ISL9110 provides an open-drain input power-good status output. The $\overline{BAT}$ status pin is driven low when V_{IN} rises above the VT_{BMON} threshold. The $\overline{BAT}$ status output goes Hi-Z when V_{BAT} falls below the VT_{BMON} threshold. Hysteresis is provided for the VT_{BMON} threshold to avoid oscillation of the $\overline{BAT}$ output.

Ultrasonic Mode (ISL9112 only)

The ISL9112 provides an ultrasonic mode that can be enabled through I^2C control by setting the ULTRA bit in the control register.

In ultrasonic mode, the PFM switching frequency is forced to be above the audio frequency range.

This ultrasonic mode applies only to PFM mode operation. With the ULTRA bit set to '1', PFM mode switching frequency is forced well above the audio frequency range (f_{SW} becomes typically

60kHz). This mode of operation, however, reduces the efficiency at light load.

Thermal Shutdown

A built-in thermal protection feature protects the ISL9110 and ISL9112 if the die temperature reaches +155°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal-shutdown mode. When the die temperature falls to +125°C (typical), the device resumes normal operation.

When exiting thermal shutdown, the ISL9110 and ISL9112 execute their soft-start sequence.

External Synchronization

An external sync feature is provided. Applying a clock signal with a frequency between 2.75MHz and 3.25MHz at the MODE/SYNC input forces the ISL9110 and ISL9112 to synchronize to this external clock. The MODE/SYNC input supports standard logic levels.

Buck-Boost Conversion Topology

The ISL9110 and ISL9112 operate in either Buck or Boost mode. When operating in conditions where V_{IN} is close to V_{OUT}, the ISL9110 alternates between Buck and Boost mode as necessary to provide a regulated output voltage.

Figure 27 shows a simplified diagram of the internal switches and external inductor.

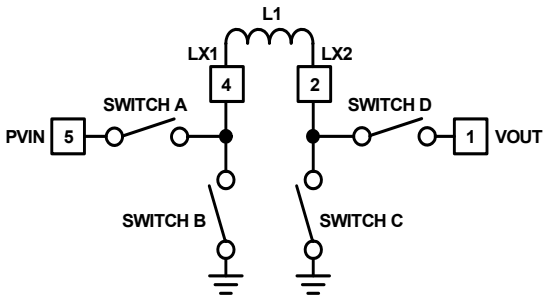


FIGURE 27. BUCK BOOST TOPOLOGY

PWM Operation

In buck PWM mode, Switch D is continuously closed, and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

In boost PWM mode, Switch A remains closed and Switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

PFM Operation

During PFM operation in Buck mode, Switch D is continuously closed, and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation.

During PFM operation in Boost mode, the ISL9110 and ISL9112 closes Switch A and Switch C to ramp up the current in the inductor. When inductor current reaches a certain threshold, the device turns off Switches A and C, then turns on Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

In most operating conditions, there are multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops, and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

Operation With VIN Close to VOUT

When the output voltage is close to the input voltage, the ISL9110 and ISL9112 rapidly and smoothly switches from Boost to Buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

Output Voltage Programming

The ISL9110 is available in fixed and adjustable output voltage versions. To use the fixed output version, the VOUT pin must be connected directly to FB.

In the adjustable output voltage version (ISL9110IRTAZ), an external resistor divider is required to program the output voltage. The FB pin has very low input leakage current, so it is possible to use large value resistors (for example, R_1 = 1MΩ and R_2 = 324kΩ) in the resistor divider connected to the FB input.

The ISL9112 is available in a fixed output version only. The factory programmed output voltage can be changed using the I^2C interface. Details about the ISL9112 programmable VOUT voltage can be found in "Register Description (ISL9112)" on page 14.

Digital Slew Rate Control (ISL9112 only)

When changing voltages using the I^2C interface, the ISL9110 can be programmed to control the rate of voltage increase or decrease as it transitions from one voltage setting to the next.

The default configuration disables this digital slew rate feature. To enable the slew rate feature, an I^2C command is sent to the ISL9112, changing the value of the SLEWRATE bit field to a value other than 0b000. Details about the digital slew rate settings can be found in Table 1.

TABLE 1. REGISTER ADDRESS 0x01: SLEW RATE CONTROL

BIT	NAME	TYPE	RESET	DESCRIPTION
2:0	SLEWRATE	R/W	000	Slew rate control (typ), expressed as µs per LSB change in DCDOUT value: 0b000 = 0µs/ΔLSB 0b001 = 1.5µs/ΔLSB 0b010 = 3.1µs/ΔLSB 0b011 = 6.3µs/ΔLSB 0b100 = 12.5µs/ΔLSB 0b101 = 25µs/ΔLSB 0b110 = 50µs/ΔLSB 0b111 = 100µs /ΔLSB
7:3	Reserved	R/W	00000	

Register Description (ISL9112)

The ISL9112 has a two I^2C accessible control registers that are used to set output voltage, operating mode, and digital slew rate. These registers can be read and written to at any time that the ISL9112 is enabled. Attempts to communicate with the ISL9112 using its I^2C interface when the ISL9112 is disabled (EN = Low) are not supported.

TABLE 2. REGISTER ADDRESS 0x00: VOLTAGE CONTROL

BIT	NAME	TYPE	RESET	DESCRIPTION
4:0	DCDOUT	R/W	00000	V_{OUT} programming. See Table 3.
5	ULTRA	R/W	0	Ultrasonic mode select. Not applicable in forced PWM mode: 0: Ultrasonic feature disabled 1: Ultrasonic feature enabled
6	Reserved	R/W	0	
7	I2CEN	R/W	0	I^2C programming enable bit: 0: Device ignores I^2C command, and uses last programmed DCDOUT and ULTRA settings; or if no I^2C communication has occurred since POR, the factory programmed default DCDOUT and ULTRA settings are used. 1: Device uses the I^2C programmed DCDOUT and ULTRA settings.

Bits DCDOUT[4:0] set the output voltage, as shown in Equation 1 and Table 3. The ISL9112 output voltage range is 1.9V to 5.0V.

$$V_{OUT} = 1.9V + (n \bullet 0.1V), \text{ where } n = 0 \text{ to } 31 \quad \text{(EQ. 1)}$$

The power-up output voltage is at 3.3V for ISL9112IRTNZ and 5V for ISL9112IRT7Z. To change to other voltages after power-up, first write the DCDOUT register to match the power-up voltage while keeping the I2CEN bit = 0, then set the I2CEN bit to 1 and set the new desired DCDOUT register value.

TABLE 3. DCDOUT[4:0] VALUE vs OUTPUT VOLTAGE

DCDOUT[4:0]	OUTPUT VOLTAGE (V)
0b00000	1.9
0b00001	2.0
0b00010	2.1
0b00011	2.2
0b00100	2.3
0b00101	2.4
0b00110	2.5
0b00111	2.6
0b01000	2.7
0b01001	2.8
0b01010	2.9
0b01011	3.0
0b01100	3.1
0b01101	3.2
0b01110	3.3
0b01111	3.4
0b10000	3.5
0b10001	3.6
0b10010	3.7
0b10011	3.8
0b10100	3.9
0b10101	4.0
0b10110	4.1
0b10111	4.2
0b11000	4.3
0b11001	4.4
0b11010	4.5
0b11011	4.6
0b11100	4.7
0b11101	4.8
0b11110	4.9
0b11111	5.0

I^2C Serial Interface (ISL9112)

The ISL9112 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL9112 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 28). Upon power-up of the ISL9112, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL9112 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 28). A START condition is ignored during the power-up sequence and when EN input is low.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 28). A STOP condition at the end of a write operation initiates the reconfiguration of the ISL9112's voltage feedback loop as necessary to provide the programmed output voltage.

An Acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 29).

The ISL9112 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and again after successful receipt of a Register Address Byte. The ISL9112 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0b0011100 as the seven MSBs, corresponding to the ISL9112 I^2C Slave Address. The LSB of the Identification byte is the Read/$\overline{\text{Write}}$ bit. Its value is "1" for a Read operation, and "0" for a Write operations (see Table 4).

TABLE 4. IDENTIFICATION BYTE FORMAT

0	0	1	1	1	0	0	R/$\overline{\text{W}}$
(MSB)							(LSB)

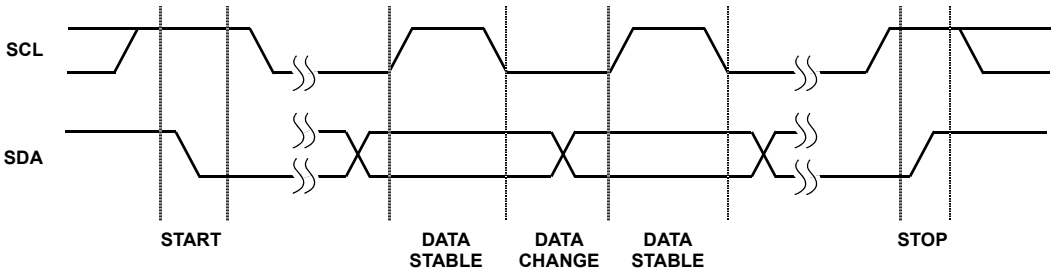


FIGURE 28. VALID DATA CHANGES, START AND STOP CONDITIONS

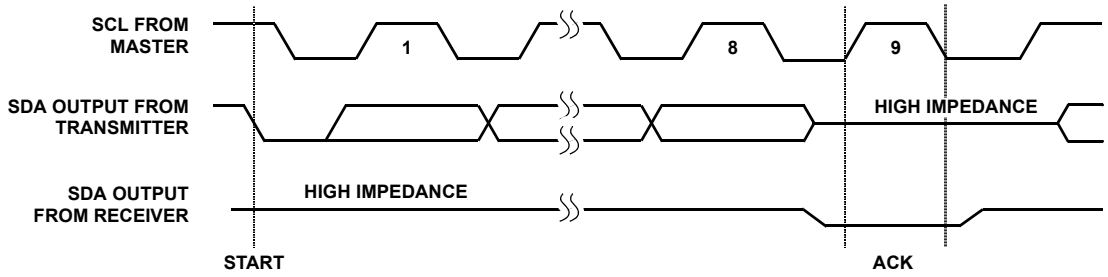


FIGURE 29. ACKNOWLEDGE RESPONSE FROM RECEIVER

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte (containing the Slave Address with the R/$\overline{W}$ bit set to 0), a valid Register Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL9112 responds with an ACK. The master then sends a STOP to complete the command.

STOP conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and its associated ACK signal. If a STOP condition is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the ISL9112 ignores the command, and does not change the output voltage or other settings.

Read Operation

A Read operation is shown in Figure 31. It consists of 4 bytes. The host generates a START condition, then transmits an Identification byte (containing the Slave Address with the R/$\overline{W}$ bit set to 0). The ISL9112 responds with an ACK. The host then transmits the Register Address byte, and the ISL9112 responds with another ACK.

The host generates a Repeat START condition, or a STOP condition followed by a START condition. It then transmits an Identification byte (containing the Slave Address with the R/$\overline{W}$ bit set to 1). The ISL9112 responds with an ACK, indicating it is ready to begin providing the requested data.

The ISL9112 then transmits the data byte by asserting control of the SDA pin while the host generates clock pulses on the SCL pin. When transmission of the data byte is complete, the host generates a NACK condition followed by a STOP condition. This completes the I^{2}C Read operation.

The ISL9112 register map supports only one register, at register address 0x00. Attempts to read other register addresses are not supported, and should not be attempted. Similarly, I^{2}C block reads and writes are not supported by the ISL9112. The ISL9112 has only one register to read or write, therefore block reads and writes are not necessary.

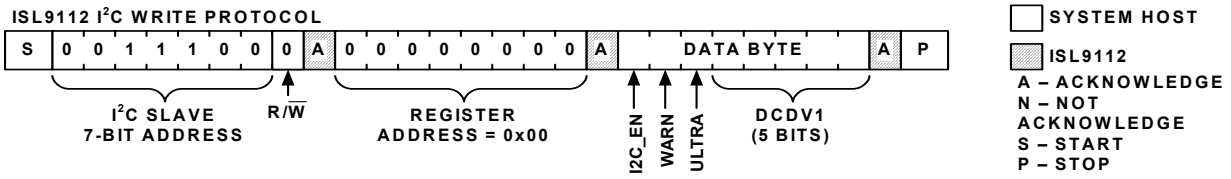


FIGURE 30. I^{2}C REGISTER WRITE PROTOCOL

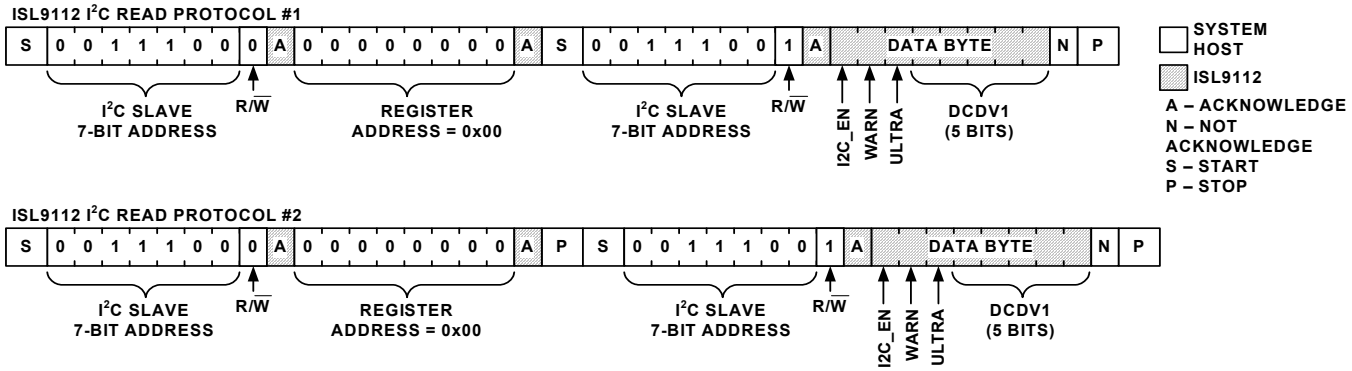


FIGURE 31. I^{2}C REGISTER READ PROTOCOL

Applications Information

Component Selection

The ISL9112 and the fixed-output versions of the ISL9110 require only three external power components to implement the buck boost converter: an inductor, an input capacitor, and an output capacitor.

The adjustable ISL9110 versions require three additional components to program the output voltage. Two external resistors program the output voltage, and a small capacitor is added to improve stability and response.

An optional input supply filtering capacitor ("C_3" in Figure 32) can be used to reduce the supply noise on the VIN pin, which provides power to the internal reference. In most applications, this capacitor is not needed.

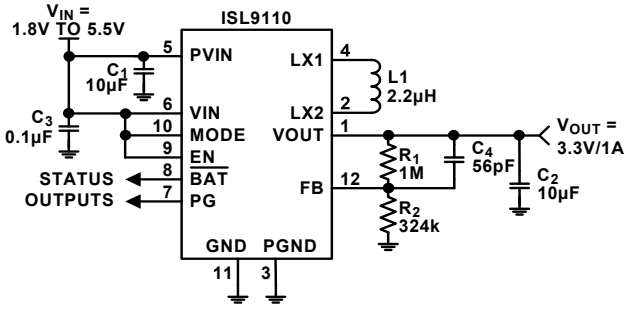


FIGURE 32. TYPICAL ISL9110IRTAZ APPLICATION

Output Voltage Programming, Adjustable Version

Setting and controlling the output voltage of the ISL9110IRTAZ (adjustable output version) can be accomplished by selecting the external resistor values.

Equation 2 can be used to derive the R_1 and R_2 resistor values:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 2)}$$

When designing a PCB, include a GND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Place the resistors R_1 and R_2 close to the FB pin.

Feed-Forward Capacitor Selection

A small capacitor in parallel with resistor R_1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 56pF for R_1 = 1MΩ. An NPO type capacitor is recommended.

Non-Adjustable Version FB Pin Connection

The fixed output versions of the ISL9110 and the I^2C-adjustable ISL9112 do not require external resistors or a capacitor on the FB pin. Simply connect VOUT to FB, as shown in Figure 33.

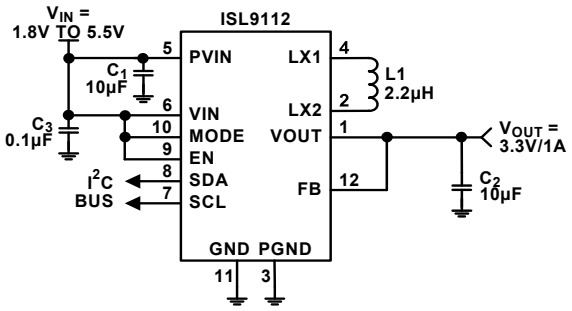


FIGURE 33. TYPICAL ISL9110IRTNZ APPLICATION

Inductor Selection

Use an inductor with high frequency core material (for example, ferrite core) to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 2.2µH inductor with ≥2.4A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

TABLE 5. INDUCTOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
Coilcraft	LPS4018	www.coilcraft.com
Murata	LQH44P	www.murata.com
Taiyo Yuden	NRS4018 NRS5012	www.t-yuden.com
Sumida	CDRH3D23/HP CDRH4D22/HP	www.sumida.com
Toko	DEM3518C	www.toko.co.jp

PVIN and VOUT Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 10µF. The recommended V_{OUT} capacitor value is 10µF to 22µF.

TABLE 6. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X5R	www.avx.com
Murata	X5R	www.murata.com
Taiyo Yuden	X5R	www.t-yuden.com
TDK	X5R	www.tdk.com

Application Example 1.

An application using the fixed-output ISL9110IRTNZ is shown in Figure 34. This application requires only three external components.

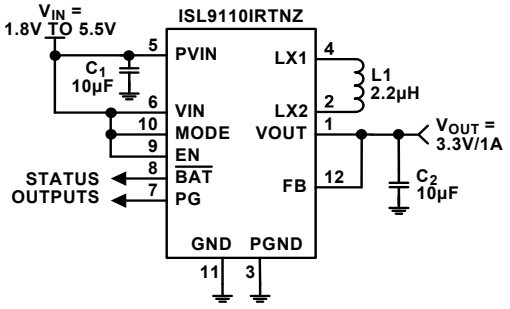


FIGURE 34. TYPICAL ISL9110IRTNZ APPLICATION

Application Example 2.

An application requiring V_{OUT} = 3.0V, using the adjustable-output ISL9110IRTAZ is shown in Figure 35. This application requires six external components.

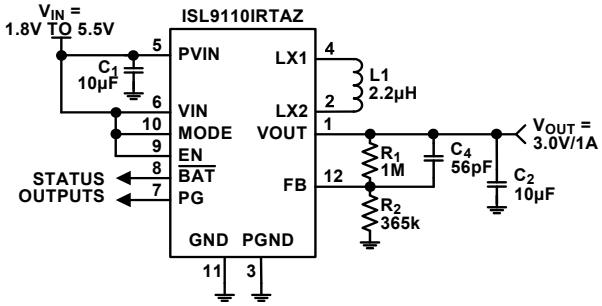


FIGURE 35. TYPICAL ISL9110IRTAZ APPLICATION

Application Example 3.

An application requiring V_{OUT} = 3.3V, using the I^2C-controllable ISL9112IRTNZ is shown in Figure 36. This application requires three external components. Output voltage can be changed using I^2C control.

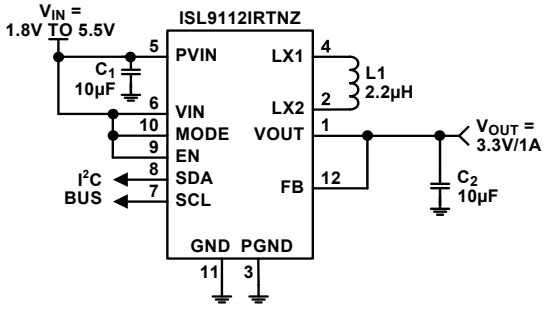


FIGURE 36. TYPICAL ISL9112IRTNZ APPLICATION

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL9110. Place the input and output capacitors as close to the IC as possible. Keep the ground connections of the input and output capacitors as short as possible, and on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

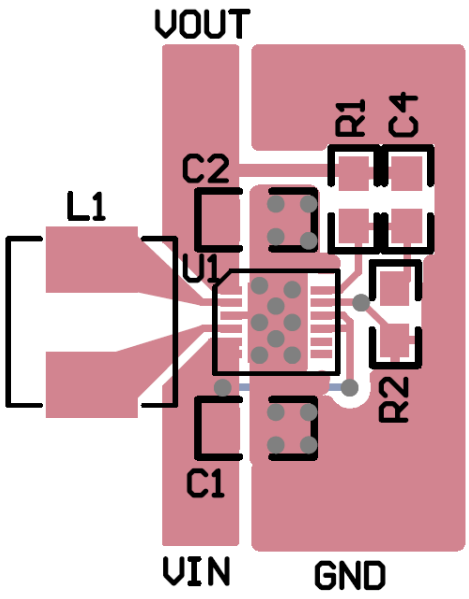


FIGURE 37. RECOMMENDED PCB LAYOUT

The TDFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to the PGND supply. Its primary function is to provide heat sinking for the IC. However, because of the connection to PGND, the thermal pad must be tied to the GND supply to prevent unwanted current flow to the thermal pad. Maximum AC performance is achieved if the thermal pad is attached to a dedicated ground layer in a multi-layered PC board.

The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer eliminates the need for individual thermal pad area. When a dedicated layer is not possible, an isolated thermal pad on another layer should be used. Pad area requirements should be evaluated on a case by case basis.

General PowerPAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.

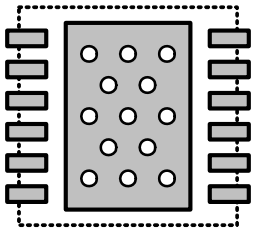


FIGURE 38. PCB VIA PATTERN

Renesas recommends that the thermal pad area is filled with vias. Fill the thermal pad area with vias that are spaced three times their radius (typically), center-to-center, from each other. Keep the vias small but not so small that their inside diameter prevents solder wicking through the holes during reflow.

It is important that the vias have a low thermal resistance for efficient heat transfer. Do not use “thermal relief” patterns to connect the vias to the ground plane. Instead use a solid connection with no gaps for improved thermal performance.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Aug 3, 2018	FN7649.3	Updated Related Literature section. Moved TOC to page 2. Updated Ordering information table by adding tape and reel parts, adding unit column, removing evaluation board part numbers, and updating Note 1. In “Register Description (ISL9112)” on page 14 updated paragraph under Equation 1. Removed Products section. Updated POD L12.3x3C to the latest revision changes are as follows: Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). Updated Disclaimer.
Jul 13, 2012	FN7649.2	Corrected Application Note titles in “” on page 1. On page 3, pin configuration diagrams, changed "MODE" to "MODE/SYNC". On page 4, added ISL9110BIRTAZ to ordering table. On page 4, added "Hiccup Mode" column in ordering table. On page 4, corrected Evaluation Board numbers. On page 13, corrected "EN/SYNC", to "MODE/SYNC" in “External Synchronization”
August 30, 2011	FN7649.1	Page 4: Removed "ISL9110EVAL1Z" from “Ordering Information” table Added "ISL9110IRTAZ-EVAL1Z" to “Ordering Information” table Added "ISL9110IRTNZ-EVAL1Z" to “Ordering Information” table Added "ISL9110IRT7Z-EVAL1Z" to “Ordering Information” table Added "ISL9112IRT7Z-EVAL1Z" to “Ordering Information” table “Inductor Selection” on page 17: Corrected "A 10µH inductor.." to "A 2.2µH inductor.."
June 16, 2011	FN7649.0	Initial release.

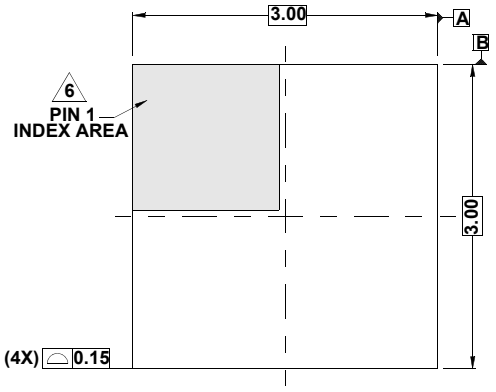
Package Outline Drawing

For the most recent package outline drawing, see L12.3x3C.

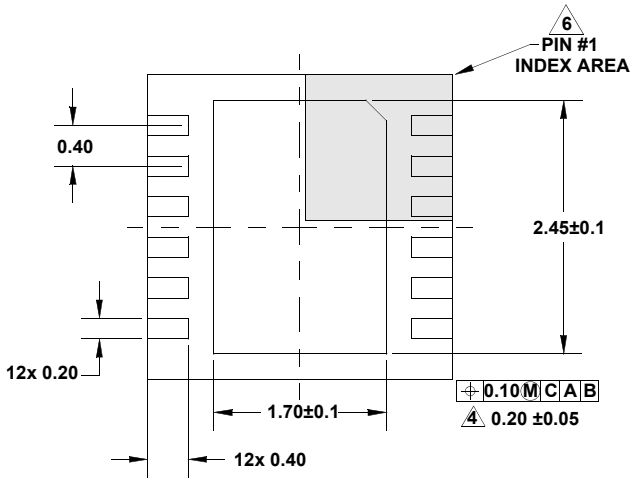
L12.3x3C

12 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (0.4mm PITCH)

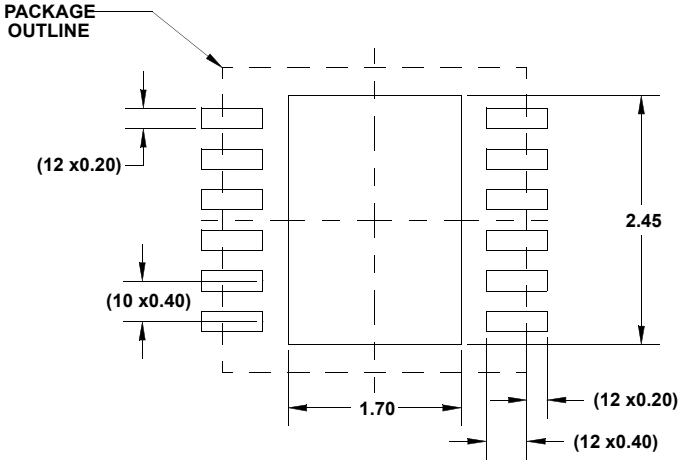
Rev 1, 4/15



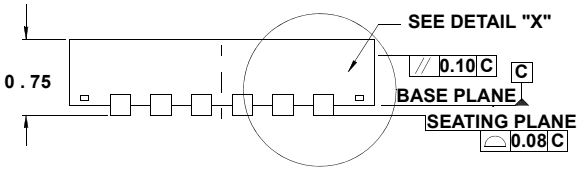
TOP VIEW



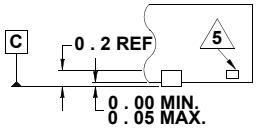
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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(Rev.4.0-1 November 2017)

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