Sinuo LIU

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EDUCATION

École Polytechnique Fédérale de Lausanne (EPFL) *Sept. 2025 -2027 (expected)*
Master of Energy Science and Technology in Electrical and Electronics Engineering Section *Lausanne, Switzerland*

- **Intention orientation:** Energy conversion devices design
- **GPA:** 5.32/6.0
- **Relevant Courses:** Industrial Electronics I & II, Energy Storage Systems, Convex Optimization, Electromagnetic Compatibility, Heat and mass transfer, Fundamentals & processes for photovoltaic devices

Harbin Institute of Technology (Shenzhen) *Sept. 2021 - Jun. 2025*
Bachelor of Engineering in Electrical Engineering *Shenzhen, China*

- **GPA:** 3.821/4.0 **Average grade:** 91.486/100.0 **Rank:** 3/84
- **Honors: National Scholarship**, Outstanding graduate, Second-class Scholarship, Outstanding Student
- **Relevant Courses:** Electromagnetic Fields, Power Electronics, Electrical Machines and Drives, Power System Analysis, Switching Power Supply Principles and Design, Automatic Control Theory.

RESEARCH PROJECTS

Control Development for a 10kV DAB using RT-HIL *Feb. 2026 - June 2026*
Supervisor: Drazen Dujic and Amin Darvishzadeh, Power Electronics Laboratory (PEL),EPFL *Lausanne, Switzerland*

- Develop a control ecosystem for a 1kV/10kV 250kW Dual Active Bridge (DAB) converter utilizing series-connected 3.3kV SiC MOSFET modules.
- Establish a high-fidelity real-time simulation model of the DAB converter on the PLECS RT-box platform, incorporating prototype-measured parameters for validation.
- Master the ABB Power Electronics Controller (PEC) ecosystem, implementing firmware, state machines, and closed-loop control algorithms via MATLAB/Simulink embedded code support.
- Conduct extensive Real-Time Hardware-in-the-Loop (RT-HIL) testing to validate modulation schemes and optimize transient performance for reliable hardware deployment.

Research on Current Limiting of GFM Inverters under Power Grid Fault Conditions *Oct. 2024 - May 2025*
Harbin Institute of Technology (Shenzhen) *Shenzhen, China*

- Completed the state-space averaging modeling of a three-phase inverter, designed the parameter tuning for a Virtual Synchronous Control strategy, and introduced a virtual impedance current-limiting strategy. Utilized MATLAB/Simulink for simulation verification.
- Performed a comparative analysis of multiple current-limiting methods, optimizing grid-connected current performance (THD, overcurrent, and recovery time) under severe voltage sags.
- Authored the bachelor's thesis based on this research.

Bi-Directional Isolated DC-DC Converter Design Using CLLLC Topology *Mar. 2024 - Aug. 2024*
Harbin Institute of Technology (Shenzhen) *Shenzhen, China*

- Served as a hardware developer in Schneider's Go Green Power Electronics Innovation Project.
- Responsible for CLLLC topology modeling, resonant cavity parameter optimization, Simulink/SIMPLIS simulation, component selection, and magnetic/thermal design.
- Successfully implemented a DC-DC converter with 36-60Vdc input, 400Vdc output, and 1kW power, achieving 93% efficiency with less than 1% ripple, which is applicable to single-stage bidirectional OBC or energy storage systems. Passed aging tests and temperature rise tests.
- Won First Prize in the National College Electrical and Electronic Engineering Innovation Competition–Schneider Go Green Power Electronics Track (**Ranked 5th Nationally**).

PUBLICATIONS

- J. Yu, **S. Liu**, Y. Gu, and H. Liu, "CLLLC Resonant Converter with Full-Bridge Half-Bridge Switching for Improved Voltage Gain Range and Light-Load Efficiency," in *2025 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, Beijing, China, 2025, pp. 1–5. doi: 10.1109/WiPDA-Asia63772.2025.11183707.

PROFESSIONAL EXPERIENCE

NOVOSENSE Microelectronics Co., Ltd *Dec. 2024 - Mar. 2025*
System Application Engineer Intern *Novosense Shenzhen Office*

- Responsible for debugging and testing the low-voltage DC-DC converter (full-bridge, 360V to 13.8V) in the OBC system of Electric Vehicles.
- Optimized the driving circuit schemes for SiC and Si MOSFETs, resolving ringing issues.
- Completed the migration of the DSP code and conducted dynamic/steady-state performance tests for the DC-DC converter.
- Participated in the debugging of the flyback auxiliary power supply in a 10kW string photovoltaic inverter system.
- Performed comparative testing between self-developed current sensing chips and those of competitors. Provide technical documentation support to the team.

Exploring Timing Jitter in Repetition-Rate Scaling of Frequency Combs *Jul. 2023 - Aug. 2023*
Research Intern Supervisor: Professor Jungwon Kim *Korea Advanced Institute of Science and Technology (KAIST)*

- Conducted experiments on timing jitter in frequency combs based on optical fiber delay line and optical carrier interference and contributed to conclusions about the relationship between repetition rate and timing jitter based on results analysis using MATLAB, thereby advancing its applications in chip-level precision timing and ultrafast laser sintering.
- Achieved the highest grade (S) for performance and task completion during this internship.

SKILLS

- **Technical Proficiencies**: Switching Power Supply Design, Modeling and Simulation of Power Electronic Systems, Hardware Circuit Design.
- **Software and Tools**: Simulink, PSIM, SIMPLIS, PLECS, Altium Designer, COMSOL, Mathcad, DSP(CCS).
- **Programming:** C, MATLAB, LaTEX
- **Languages**: English (Advanced, IELTS 7.5), Chinese (Native), French(Beginner)