Übung 10, Aufgabe 2

Reaktionszeit-Spiel fuer zwei Personen

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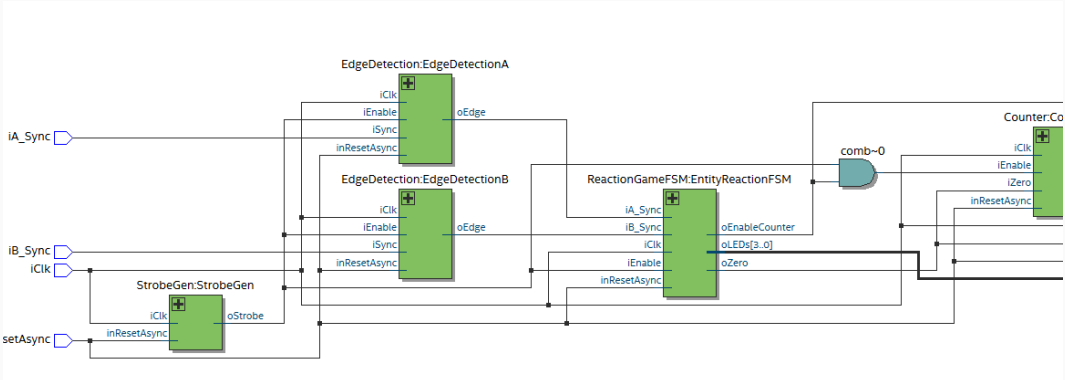
13. Januar 2026

FH Hagenberg

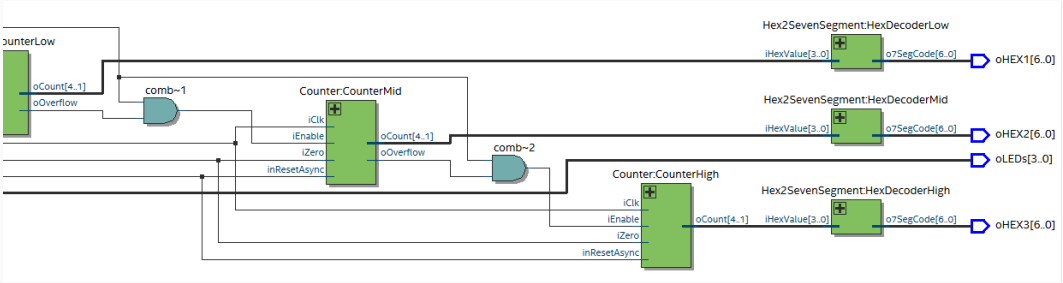
Agenda

- Struktur des Reaktionszeit-Spiels
- Edge Detection
- Finite State Machine
- Counter
- Hex to 7-Segment Decoder
- Simulation Reaction Time Game
- Ressource Summary

Struktur des Reaktionszeit-Spiels



Struktur des Reaktionszeit-Spiels

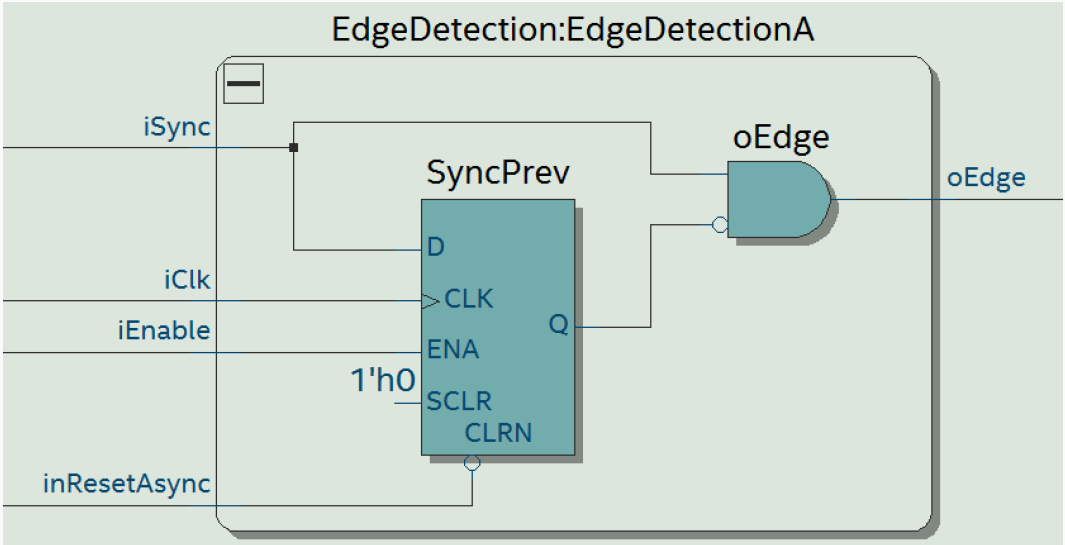


Edge Detection

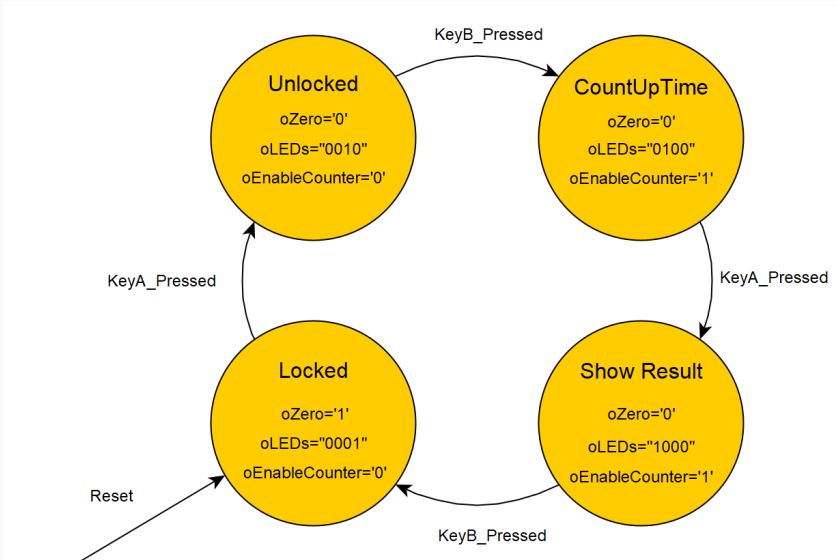
```vhdl
entity EdgeDetection is
port (
  iClk : in std_ulogic;
  inResetAsync : in std_ulogic;
  iEnable : in std_ulogic;
  iSync : in std_ulogic;
  oEdge : out std_ulogic);
end EdgeDetection;

```

```vhdl
architecture RTL of EdgeDetection is
  signal SyncPrev : std_ulogic;
begin

process (iClk, inResetAsync) is
  begin
    -- asynchronous reset
    if (inResetAsync = not('1')) then
      SyncPrev <= '0';

    elsif (rising_edge(iClk)) then
      if(iEnable = '1') then
        SyncPrev <= iSync;
      else
        SyncPrev <= SyncPrev;
      end if;
    end if;
end process;

-- combinational logic for edge detection
oEdge <= '1' when (iSync = '1' and SyncPrev = '0') else '0';

end architecture RTL;

```

Edge Detection RTL Viewer



Finite State Machine Moore



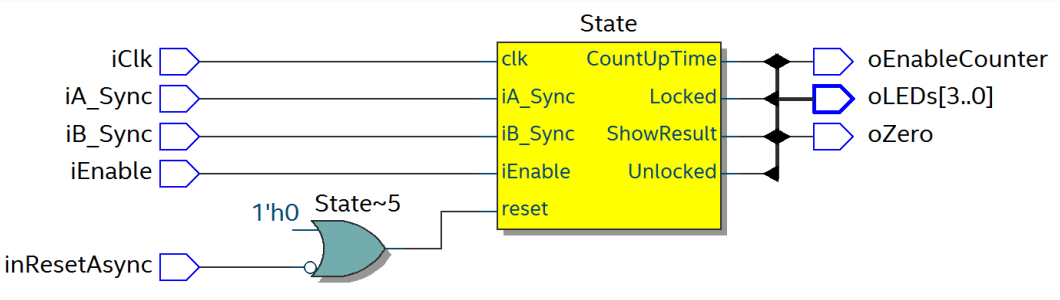
State Register

```
1   -- State Register
2   process (iClk, inResetAsync) is
3   begin
4     if (inResetAsync = not('1')) then
5       State <= Locked;
6     elsif (rising_edge(iClk)) then
7       if(iEnable = '0') then
8         State <= State; -- hold state when not enabled
9       else
10        State <= NextState;
11      end if;
12    end if;
13  end process;
```

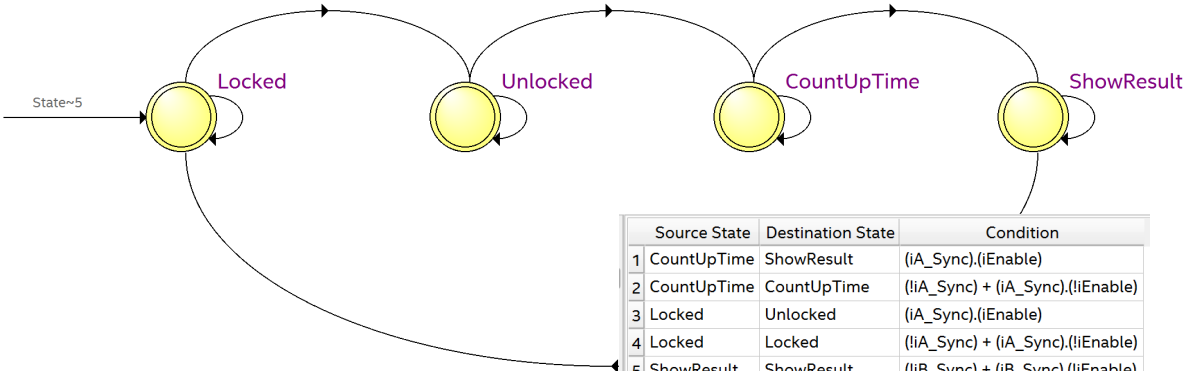
Next State Logic

```
-- State Transition Process
NextStateLogic : process (State,iEnable,iA_Sync,iB_Sync) is
begin

  NextState <= State;     -- default hold state
  oLeds <= cLEDOFF;       -- default all leds off
  oZero <= '0';           -- default zero off
  oEnableCounter <= '0'; -- default counter disabled

  case State is
    when Locked =>
      if(iA_Sync = '1') then
        NextState <= Unlocked;
      end if;
      oZero <= '1';                    -- reset counters
      oLeds(cLED_LOCKED_INDEX) <= '1'; -- indicate locked
       state

    when Unlocked =>
      if(iB_Sync = '1') then
        NextState <= CountUpTime;
      end if;
      oLeds(cLED_UNLOCKED_INDEX) <= '1'; -- indicate locked
       state

    when CountUpTime =>
      oEnableCounter <= '1'; -- enable counter
      if(iA_Sync = '1') then
        NextState <= ShowResult;
      end if;
      oLeds(cLED_COUNTUP_INDEX) <= '1'; -- indicate locked
       state

    when ShowResult =>
      if(iB_Sync = '1') then
        NextState <= Locked;
      end if;
      oLeds(cLED_SHOWRESULT_INDEX) <= '1'; -- indicate locked
       state

    when others =>
      NextState <= cStateAllOff;
  end case;

end process;
```

Finite State Machine RTL-Viewer



Finite State Machine State Machine Viewer



	Source State	Destination State	Condition
1	CountUpTime	ShowResult	(iA_Sync).(iEnable)
2	CountUpTime	CountUpTime	(!iA_Sync) + (iA_Sync).(!iEnable)
3	Locked	Unlocked	(iA_Sync).(iEnable)
4	Locked	Locked	(!iA_Sync) + (iA_Sync).(!iEnable)
5	ShowResult	ShowResult	(!iB_Sync) + (iB_Sync).(!iEnable)
6	ShowResult	Locked	(iB_Sync).(iEnable)
7	Unlocked	CountUpTime	(iB_Sync).(iEnable)
8	Unlocked	Unlocked	(!iB_Sync) + (iB_Sync).(!iEnable)

Finite State Machine RTL-Viewer

Flow Status	Successful - Thu Jan 8 10:21:47 2026
Quartus Prime Version	23.1std.1 Build 993 05/14/2024 SC Lite Edition
Revision Name	ReactionGameFSM
Top-level Entity Name	ReactionGameFSM
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	3 / 32,070 (< 1 %)
Total registers	4
Total pins	11 / 457 (2 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

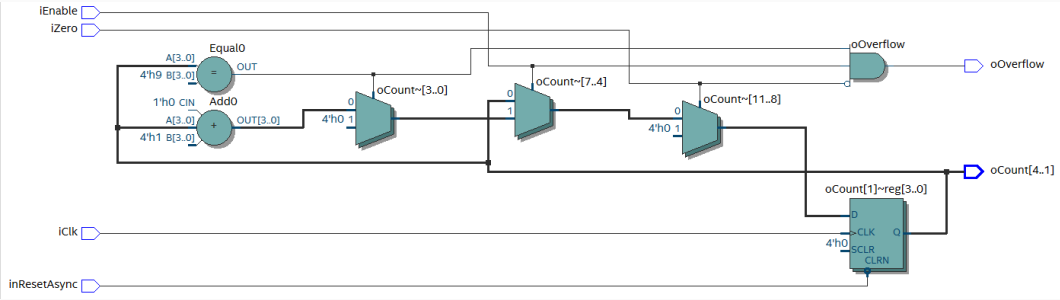
	Fmax	Restricted Fmax	Clock Name
1	651.89 MHz	645.99 MHz	iClk

Counter

```vhdl
entity Counter is
  generic(
    gCounterOverflowVal : natural := 10
  );
  port (
  iClk          : in  std_ulogic;
  iEnable       : in  std_ulogic;
  inResetAsync : in  std_ulogic;
  iZero         : in  std_ulogic;
  oOverflow     : out std_ulogic;
  oCount        : out unsigned(LogDualis(gCounterOverflowVal)
      downto 1));
end Counter;
```

```vhdl
architecture RTL of Counter is
begin

  -- combinational logic for overflow output
  oOverflow <= '1' when (iEnable = '1' and iZero = '0' and
      oCount = gCounterOverflowVal - 1) else '0';

  process(iClk, inResetAsync) is
  begin
    if inResetAsync = not('1') then
      oCount    <= (others => '0');
    elsif rising_edge(iClk) then
      if iZero = '1' then
        oCount <= (others => '0');
      elsif iEnable = '1' then
        if oCount = gCounterOverflowVal - 1 then
          oCount    <= (others => '0');
        else
          oCount <= oCount + 1;
        end if;
      end if;
    end if;
  end process;
end architecture RTL;
```

Counter RTL Viewer

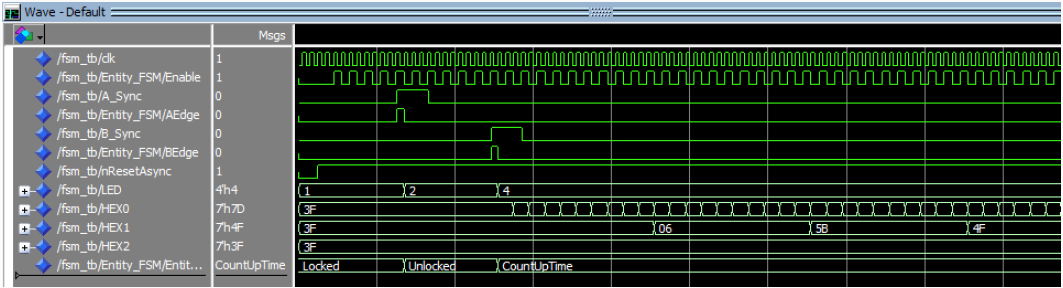


Hex to 7-Segment Decoder

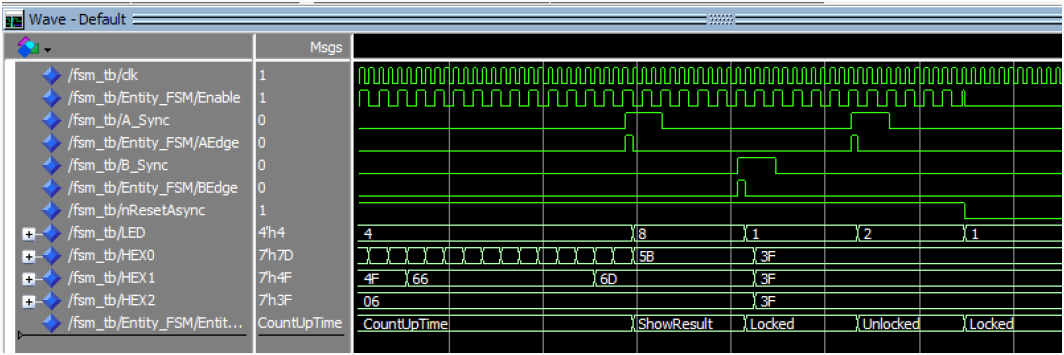
```
architecture Rtl of Hex2SevenSegment is

  function ToSevSeg(cValue : std_ulogic_vector(3 downto 0))
    return std_ulogic_vector is
  begin
    case cValue(3 downto 0) is
      when "0000" => return "0111111";
      when "0001" => return "0000110";
      when "0010" => return "1011011";
      when "0011" => return "1001111";
      when "0100" => return "1100110";
      when "0101" => return "1101101";
      when "0110" => return "1111101";
      when "0111" => return "0000111";
      when "1000" => return "1111111";
      when "1001" => return "1101111";
      when "1010" => return "1110111";
      when "1011" => return "1111100";
      when "1100" => return "0111001";
      when "1101" => return "1011110";
      when "1110" => return "1111001";
      when "1111" => return "1110001";
      when others => return "XXXXXXX";
    end case;
  end ToSevSeg;
```

```
begin

  o7SegCode <= ToSevSeg(iHexValue);

end Rtl;
```

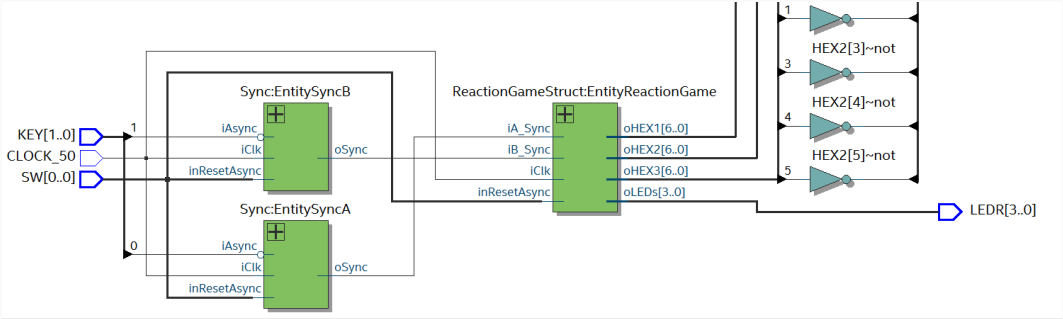
Simulation Reaction Time Game



Simulation Reaction Time Game



PCB Adapter


KEY[1..0]
CLOCK_50
SW[0..0]
1
0
Sync:EntitySyncB
iAsync
iClk
inResetAsync
oSync
Sync:EntitySyncA
iAsync
iClk
inResetAsync
oSync
ReactionGameStruct:EntityReactionGame
iA_Sync
iB_Sync
iClk
inResetAsync
oHEX1[6..0]
oHEX2[6..0]
oHEX3[6..0]
oLEDs[3..0]
1
HEX2[3]~not
3
HEX2[4]~not
4
HEX2[5]~not
5
LEDR[3..0]

Ressource Summery

- SyncStage: 2 x 2 Flip-Flops
- EdgeDetection: 2 x 1 Flip-Flops
- StrobeGen: 17 Flip-Flops
- FSM: 4 Flip-Flops
- Counter: 3 x 4 Flip-Flops

Gesamt Anzahl Flip-Flops: 39

Ressource Summery

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Jan 13 09:35:01 2026
Quartus Prime Version	23.1std.1 Build 993 05/14/2024 SC Lite Edition
Revision Name	ReactionGameOnDE1SOC
Top-level Entity Name	ReactionGameOnDE1SOC
Family	Cyclone V
Device	5CSEMA5F31C6
Timing Models	Final
Logic utilization (in ALMs)	36 / 32,070 (< 1 %)
Total registers	39
Total pins	29 / 457 (6 %)
Total virtual pins	0
Total block memory bits	0 / 4,065,280 (0 %)
Total DSP Blocks	0 / 87 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

	Fmax	Restricted Fmax	Clock Name
1	187.02 MHz	187.02 MHz	iClk

Test am DE1 SOC FPGA Board

▸ Video öffnen

Fragen?