TÉCNICO LISBOA

1ST ELECTRONIC INTEGRATED SYSTEMS PROJECT

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Course: Electronic Integrated Systems

Subject: Operational Amplifier

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1 Schematic Design

1.1 Prerequisites

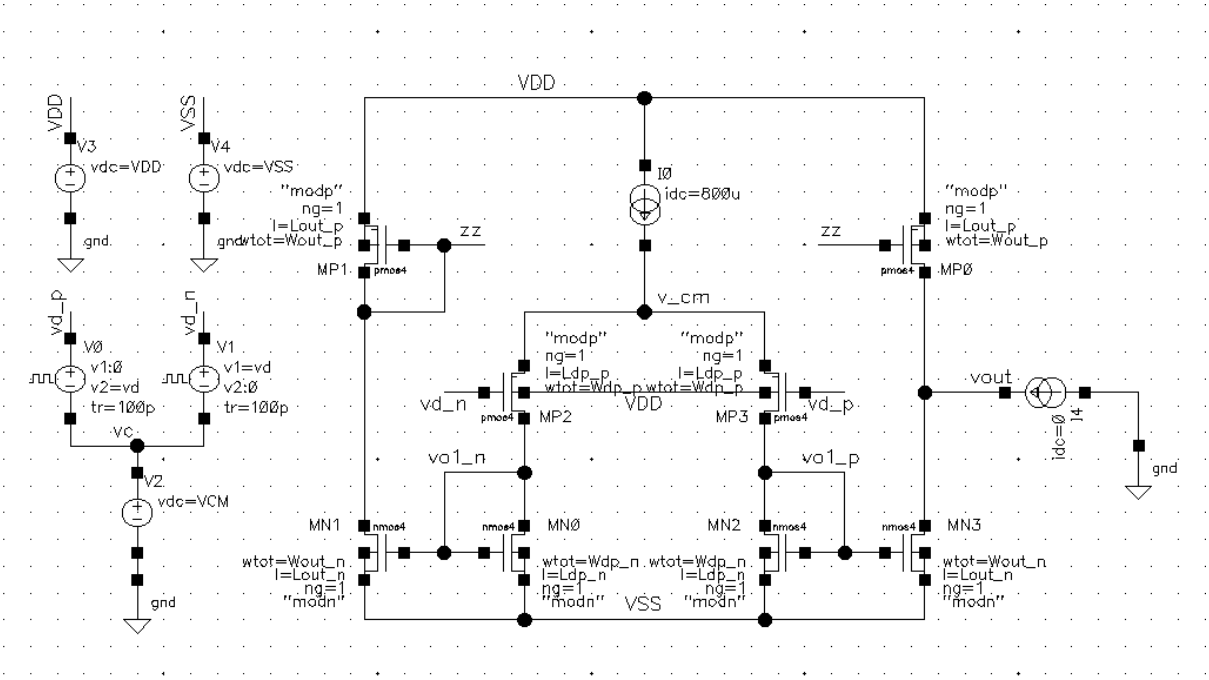


Figure 1: Schematic of one stage operational amplifier

Figure 1 shows the schematic of the operational amplifier. It has one stage with one pole at the output. Its differential gain A_{DM} is determined by the transconductance g_{m} of the differential input pair transistors, and the output resistance R_{out}, according to Equation 1. The goal is to achieve a power consumption of $I_{\mathrm{power}} \leq 5\,\mathrm{mA}$ and a differential gain $A_{\mathrm{DM}} \geq 36\,\mathrm{dB}$.

$$A_{\mathrm{DM}} = g_{\mathrm{m}} R_{\mathrm{out}} \tag{1}$$

The gain stage shall have a bias current of $800\,\mu A$. It is provided by an ideal current source, which will be replaced by a real transistor circuit once the rest of the operational amplifier has been designed.

The schematic also includes voltage sources at the inputs of the operational amplifiers. They provide a common mode voltage $v_C = (v_1 + v_2)/2$ and a differential voltage $v_D = v_1 - v_2$, where v_1 and v_2 are the input voltages. Their values are adjusted according to the simulation conducted.

Lastly, a current source is connected to the output. It enables simulations including draining and feeding current.

1.2 Differential pair and current mirrors

The channel width of all transistors are set to $10\,\mu m$ and the length to $0.35\,\mu m$, the latter value corresponds to the C35B4C3 technology node size. The supply voltages are $V_{DD} = 3.2\,V$ and $V_{SS} = 0\,V$. The inputs of the differential pair does not have a differential part ($v_d = 0\,V$). However, a DC common mode voltage of half the supply voltage ($V_C = 1.6\,V$) is applied to the input for biasing the operational amplifier. Next, the DC operating point is determined through simulation.

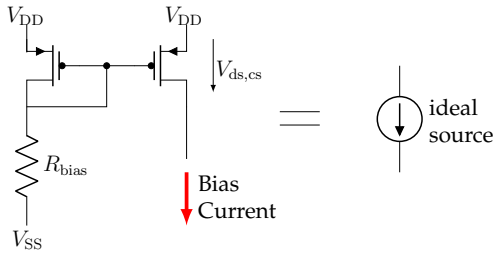
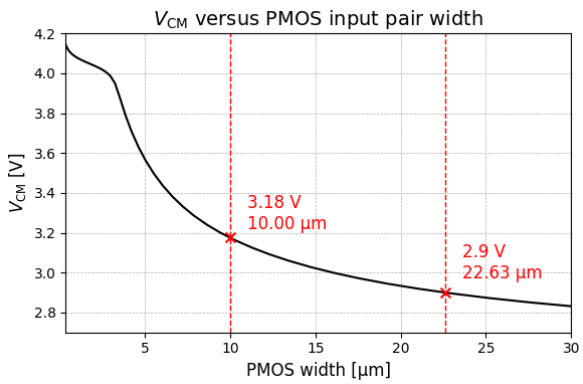


Figure 2: Current source transistor schematic

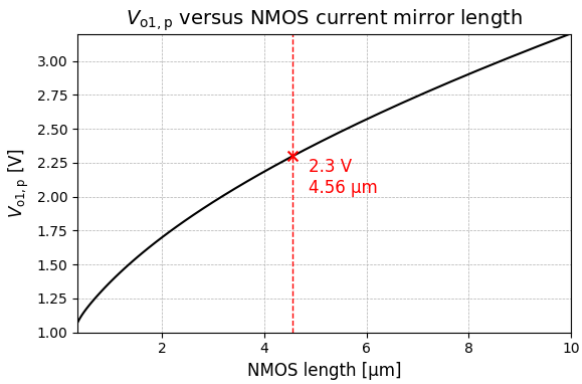
The operating point shall enable a voltage drop of at least $V_{ds,cs} = 300\,mV$ across the current source. Later, when the ideal current source is replaced by the transistor circuit demonstrated in Figure 2, this will guarantee its saturation. Setting the voltage at the common mode node to $V_{CM} = V_{DD} - V_{ds,cs} = 2.9\,V$ fulfills this requirement, where V_{CM} is the voltage at the node labeled v_cm in the schematic in Figure 1. Therefore, the input differential pair width is adjusted to $W_{dp\_p} = 22.63\,\mu m$, which leads to the desired V_{CM} value according to Figure 3a. Lastly, a large $V_{ds,cs}$ leads to a decrease of the source-gate voltage V_{SG} of the input pair, therefore increasing the transconductance g_m according to Equation 2.

$$g_m = \frac{I_D}{V_{SG} - V_t} \tag{2}$$

The required voltage drop of the PMOS input differential pair is its saturation voltage $V_{ds,sat} \geq 526.3\,mV$. This may be fulfilled by setting the voltages $V_{o1,p}$ and $V_{o1,n}$ at the NMOS current mirror gate nodes (labeled as vo1_n and vo1_p in the schematic) to 2.3 V. This is achieved by setting the NMOS current mirror channel length to $L_{dp\_n} = 4.56\,\mu m$, as shown by Figure 3b. All transistors in the NMOS current mirror have the same sizes, meaning $W_{dp\_n} = W_{out\_n}$ and $L_{dp\_n} = L_{out\_n}$



(a) V_{CM} versus $W_{\mathrm{dp\_p}}$



(b) $V_{\mathrm{o1,p}}$ versus $L_{\mathrm{dp\_n}}$

Figure 3: Relevant plots for adjusting $V_{\mathrm{ds,cs}}$

Increasing the channel length leads to a larger output resistance, and therefore gain. Furthermore, it will prove to be useful later when adjusting the DC operating point at the output node.

The next step involves the modification of the PMOS current mirror. First, it shall have a low drain-source conductance g_{ds} for a high gain. The NMOS current mirror has $g_{\mathrm{ds}} = 7.01\,\mu\mathrm{S}$, which would be a reasonable value for its PMOS counterpart. Increasing the channel length of the PMOS to $L_{\mathrm{out\_n}} = 2.99\,\mu\mathrm{m}$ achieves this goal, according to Figure 4.

Second, the DC output voltage bias shall equal $V_{\mathrm{O}} = V_{\mathrm{DD}}/2 = 1.6\,\mathrm{V}$. Currently, it is too low. Therefore, the PMOS current mirror channel width is increased to $W_{\mathrm{out\_p}} = 85.71\,\mu\mathrm{m}$. With an adjustment of the channel length to $L_{\mathrm{out\_n}} = 2.99\,\mu\mathrm{m}$, the DC bias output voltage equals $V_{\mathrm{O}} = 1.6\,\mathrm{V}$. All parameters which result from the design phase are listed in Table 1.

Parameter	Value [µm]
$L_{\mathrm{out\_p}}$	4.05
$W_{\mathrm{out\_p}}$	85.71
$L_{\mathrm{out\_n}}$	4.56
$W_{\mathrm{out\_n}}$	10
$L_{\mathrm{dp\_p}}$	0.35
$W_{\mathrm{dp\_p}}$	28.45
$L_{\mathrm{dp\_n}}$	4.56
$W_{\mathrm{dp\_n}}$	10

Table 1: Final parameter values

Now, the AC gain A_{DM} of the operational amplifier is investigated. The differential input voltage equals $v_{\mathrm{d}} = 1\,\mathrm{V}$. The resulting plot in Figure 5 indicates a sufficient gain of $A_{\mathrm{DM}} = 38.07\,\mathrm{dB}$. Furthermore, the cut-off frequency reaches $f_{\mathrm{c}} = 14.31\,\mathrm{MHz}$. Equation 3 yields a gain-bandwidth product of $GBW = 1.15\,\mathrm{GHz}$.

$$GBW = A_{\mathrm{DM}} \cdot f_{\mathrm{c}} \tag{3}$$

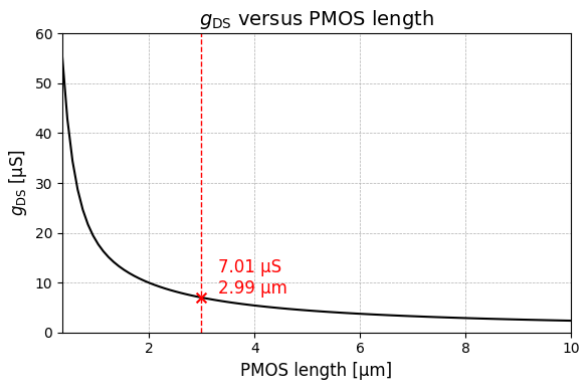


Figure 4: g_{DS} versus PMOS length

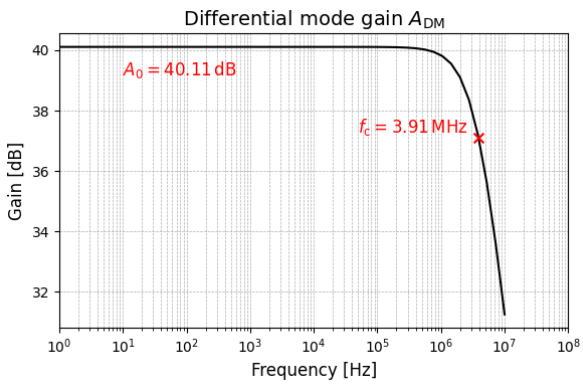


Figure 5: A_{DM} over frequency

1.3 Bias current

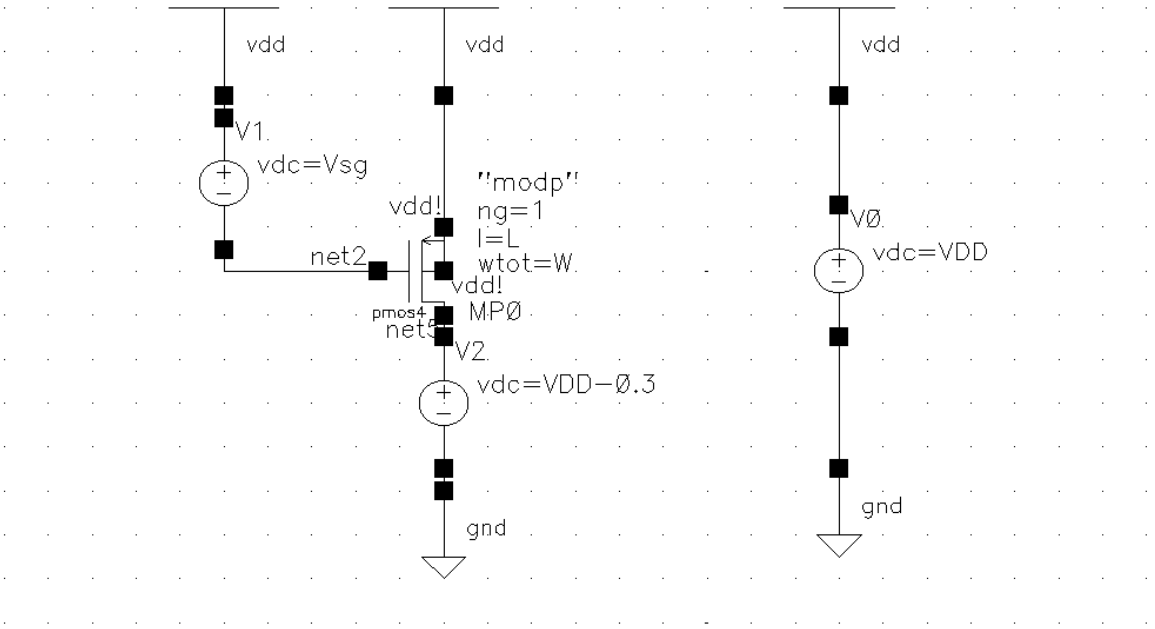


Figure 6: Testbench of current mirror

The schematic used to replace the ideal current mirror providing the bias current was already presented previously in Figure 2. Its first transistor is scaled with simulation results obtained from the testbench in Figure 6. There, a sweep of the source-gate voltage V_{SG} and the PMOS channel width is conducted. A drain current $I_D = 800\,\mu A$ is determined at a width of $W = 200\,\mu m$ and a source-gate voltage of $V_{SG} = 981.1\,mV$.

Now the remaining PMOS transistor with the resistor attached to the drain is added. The PMOS transistor's dimension is set equal to the first one, essentially creating a current mirror with a ratio of 1:1. Sweeping the resistance values demonstrates, that $R_{bias} = 2.227\,k\Omega$ delivers the desired $V_{SG} = 981.1\,mV$ to the PMOS transistors.

The node voltage V_{CM} is slightly reduced. This is compensated by increasing the differential input pair channel width to $W_{dp\_p} = 28.69\,\mu m$. Figure 7 shows the final operational amplifier schematic with annotated DC bias points including the bias current

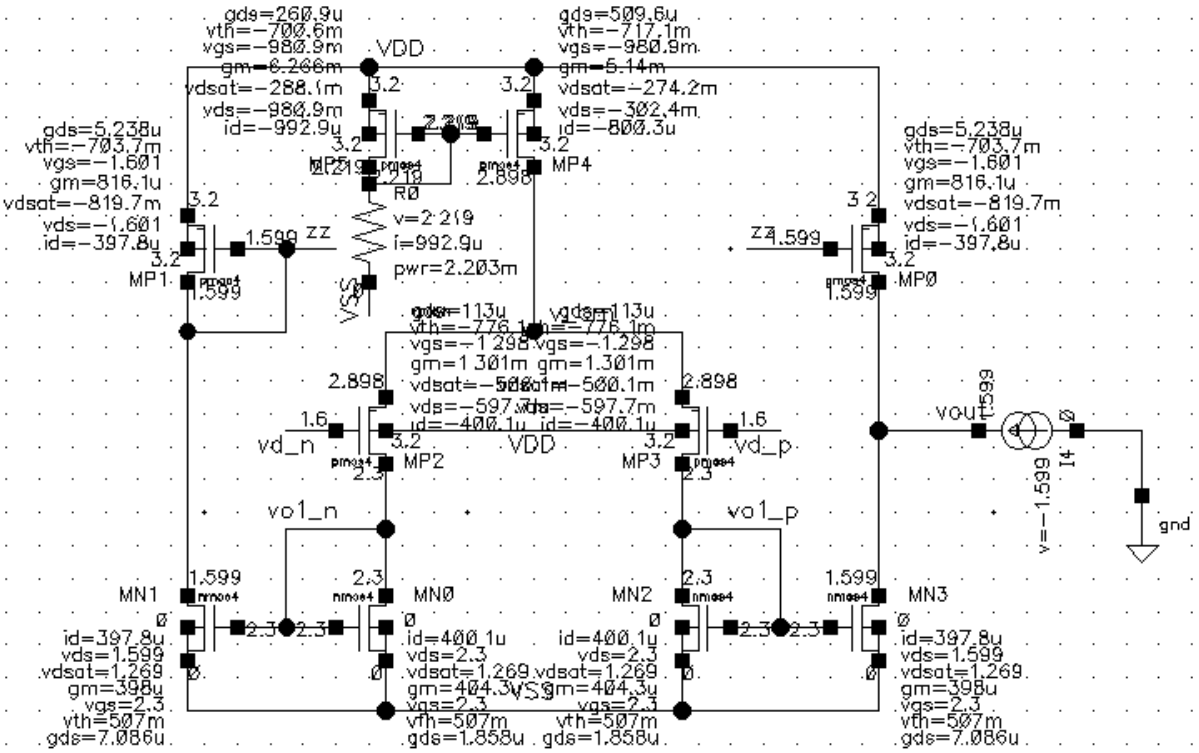


Figure 7: Final operational amplifier schematic with DC bias points

transistors. **The total current consumption of all branches equals 2.59 mA**, which is below the threshold of 5 mA. Lastly, the schematic is turned into a hierarchical topology for the next steps.

Assigned values for the amplifier design:

1. $VDD = 3.2\ V$
2. $VSS = 0\ V$
3. $I_{diff} = 800\ mA$
4. Minimum low frequency gain A = 36 dB
5. current consumption 5 mA

1.3.1 Description

In order to complete the assigned tasks, first we had to create a schematic for a one-stage operational amplifier. Following tasks must be completed:

1. Bias point simulation
2. Frequency response of the differential mode $A_d(f)$ and common mode $A_c(f)$ gains, and CMRR(f) (in decibels) also
3. Frequency response of the differential and common mode input impedance and output impedance (real and imaginary parts)
4. Input referred offset voltage

5. Frequency response of the power supply rejection ratios (in decibels)
6. Input common mode voltage range and output voltage range
7. Phase margin
8. Output rise and fall slew-rate (V/μs)
9. Total supply bias current and power consumption
10. Simulate Ad(f) for the process, voltage (±10%), and temperature dispersion ($-40°$,$125°$).

After creating a schematic and setting all transistors to their default dimensions, we could continue to set the bias point to our desired value. As a current source for the differential pair, an ideal current source with a value of 800 mA was used. To create a current source as an active element, we had to set the voltage drop across the current source to at least 300 mV. That gives us an additional 2.9 V for the differential pair. The voltage drop across the current source was affected by the design of the widths of the differential pair transistors.

Bias current To set the assigned current for the differential pair, we first used an ideal current source set to 800 mA. After obtaining the desired voltage drop across the current source and the gain of the OpAmp, the current source was designed in a few steps. First, we designed the dimensions for a transistor, defining the final current flowing to the differential pair, which we achieved by defining ideal voltage sources for V_{GS}. All parameters were found by sweeping the dimensions of the desired part. The same thing was done for the resistor. The resistor had a default sheet resistance set to 1220 $\Omega/\square$. After defining the important value of a poly resistor throughout the layout design, which will be described further in the report, we faced the reality that the dimensions of the transistor were too small. For that, we used a different method and defined the recommended dimensions for the resistor, with an L/W ratio greater than 5, and the width cannot be smaller than $2\,\mu m$. After this, we were able to continue with the parallel combination of three transistors, which defined the final value corresponding to what we needed. The width of transistors is shown in the figure 8.

Params	Values [μm]
W_{GS}	200
L_{GS}	0.35
W	200
L	0.35
W_R	2
L_R	10

Table 2: Dimensions of components for current bias source, final resistance $R = 2222\ \Omega$

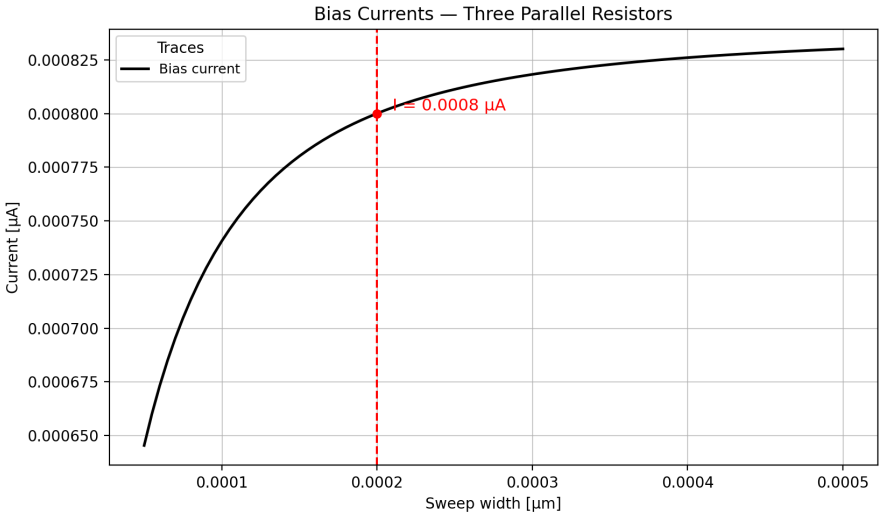


Figure 8: Bias current depending on width of biasing transistors

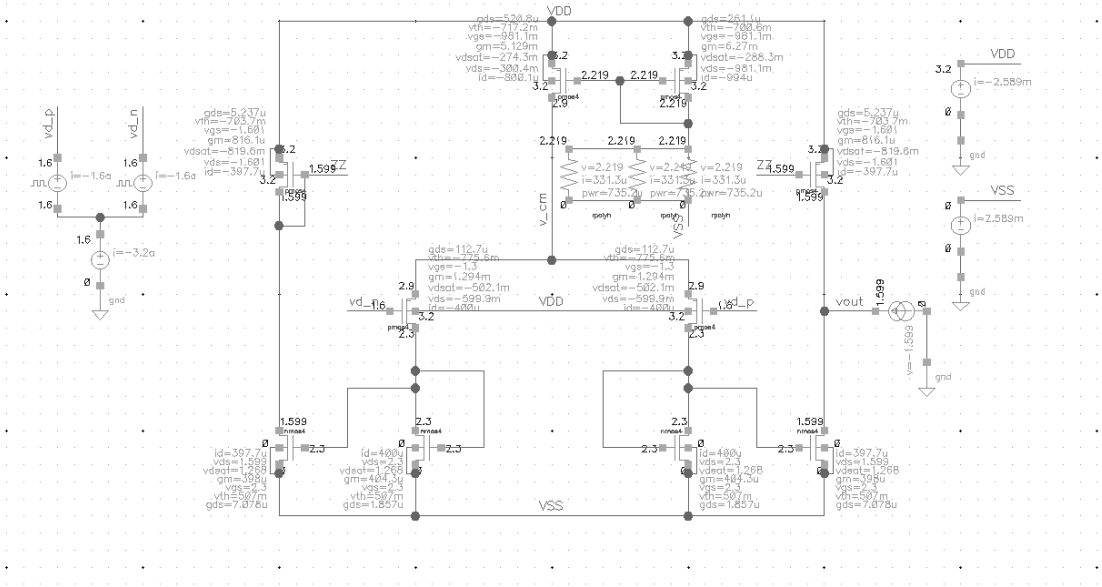


Figure 9: Schematic with operating points (modified).

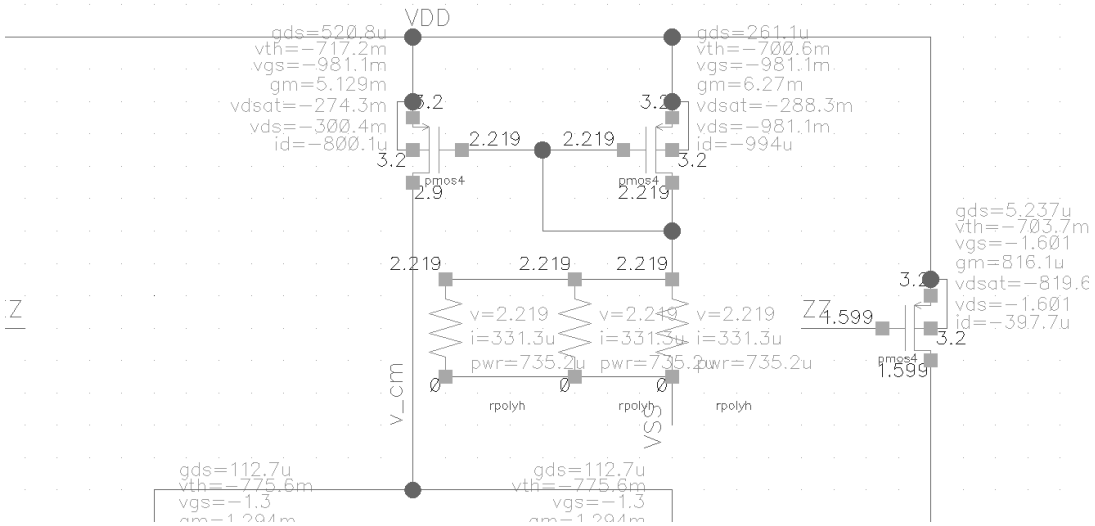


Figure 10: Close-up of the modified current source.

2 Simulations

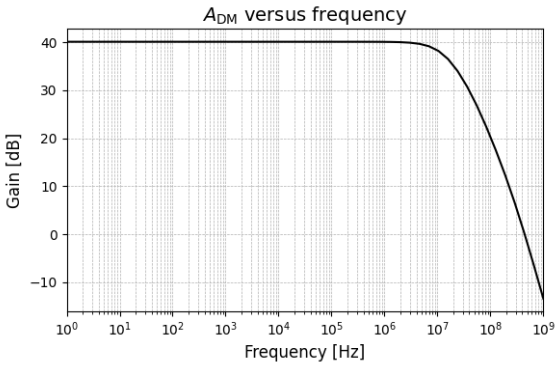
Frequency response of differential input and common mode input

On the first graph in the Figure 11 we obtained an assigned gain just right above 36 dB. Thanks to the design of the output transistor's dimensions, we were able to obtain this high gain. Unfortunately, because of this, we also obtained high common mode gain at higher frequencies, which isn't ideal. From both graphs, we calculated the final CMMR ratio and plotted it into the third graph. It can be seen that at higher frequencies, the CMMR goes into negative values. The final graph shows the phase margin, where the circuit obtained phase $-157.63°$ at 0 dB gain, and because the phase is still above $-180°$, we can define that the operational amplifier is stable. The phase margin is not ideal because it is only $22.37°$, but it is optimal enough for the next simulations.

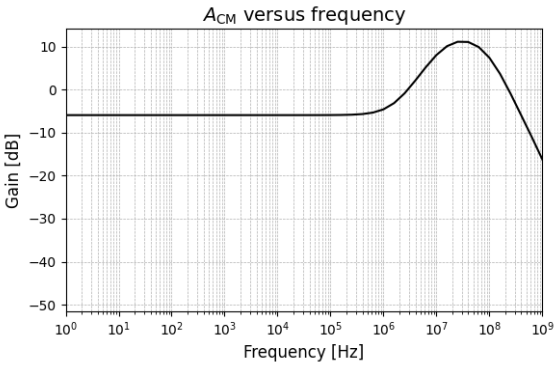
For CMRR computation can be used one of the following equations:

$$\mathrm{CMRR}_{\mathrm{dB}} = 20 \cdot \log_{10}\left(\frac{A_{dm}}{A_{cm}}\right)$$

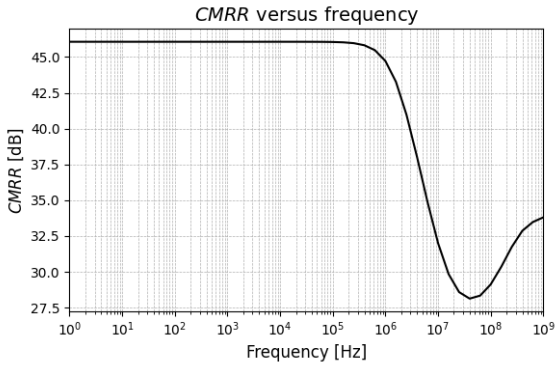
$$\mathrm{CMRR}_{\mathrm{dB}} = A_{dm,\mathrm{dB}} - A_{cm,\mathrm{dB}}$$



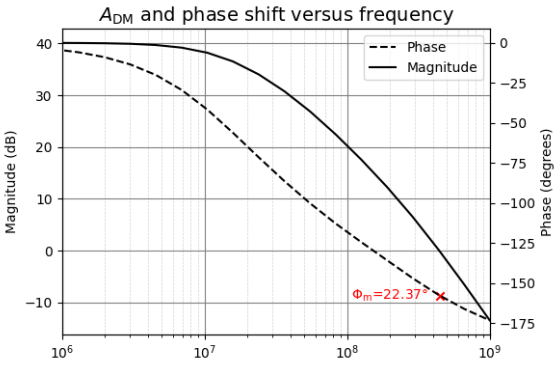
Differential mode $A_d(f)$ [dB]



Common mode $A_c(f)$ [dB]



CMRR ratio [dB]

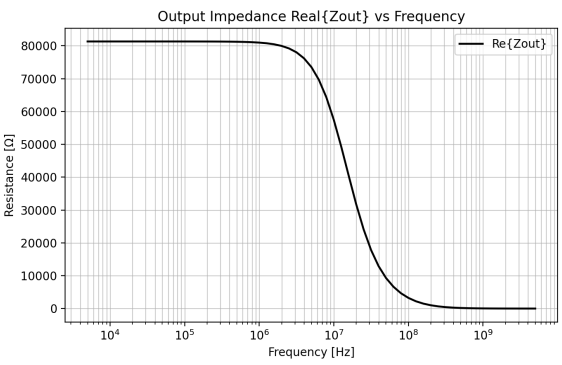


Phase Margin [°]

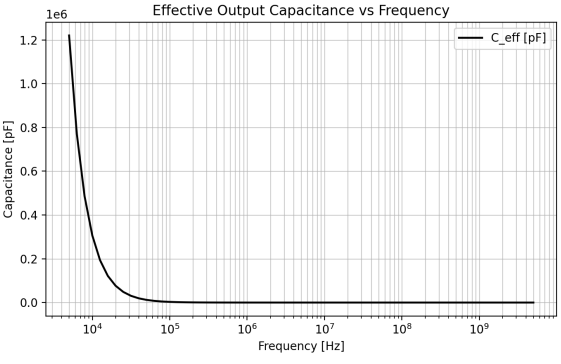
Figure 11: Overview summary of frequency domain simulations

Input impedance of differential and common mode

Output impedance

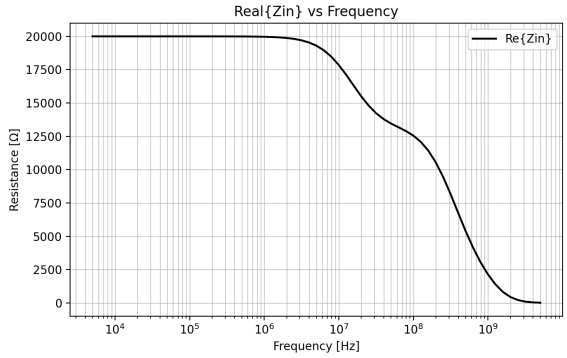


Output impedance, real part Z_{out} [Ω]

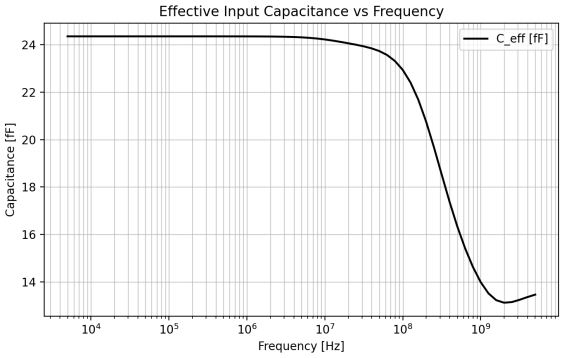


Output impedance, imaginary part Z_{out} [pF]

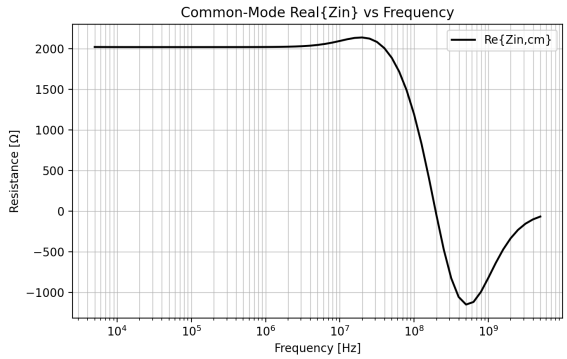
Figure 13: Overview summary of frequency domain simulations, output impedance



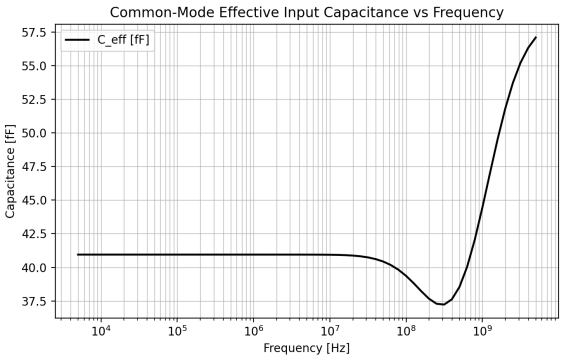
Differential mode input impedance - real part [Ω]



Differential mode input impedance - imaginary part [pF]



Common mode input impedance - real part [Ω]



Common mode input impedance - imaginary part [pF]

Figure 12: Overview summary of frequency domain simulations, input impedance

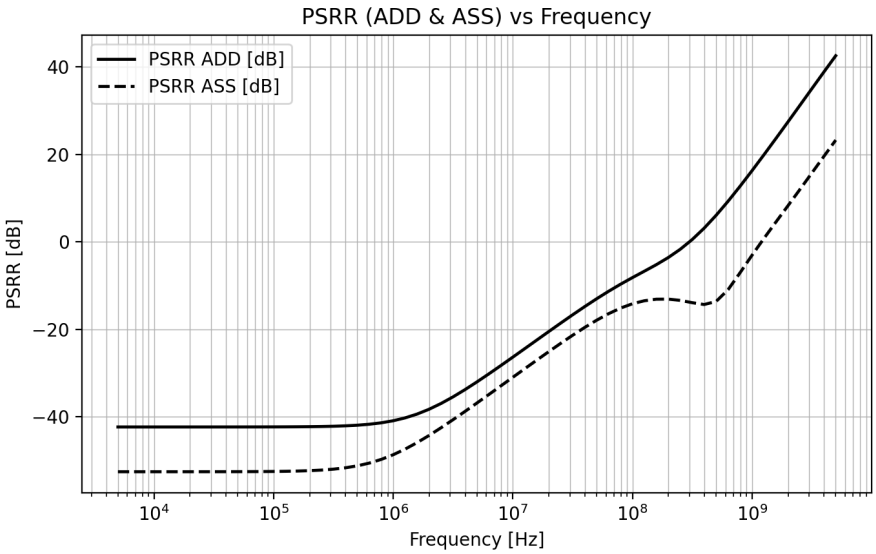
For the impedance of an OpAmp, in the ideal case, we work with infinite input impedance and zero output impedance. In the real case, that isn't possible. For the case of a differential mode input impedance, we obtained impedance with a value around 12 kΩ, which is very low. For output impedance, we obtained values of the real part around 7 kΩ, but we were looking for the lowest possible. Same for the imaginary part, where the capacitance reached a value of 1.6 pF and with higher frequency it decreases with an exponential pattern.

For PSRR computation can be used one of the following equations:

$$\mathrm{PSRR}_{DD,\mathrm{dB}} = 20 \cdot \log_{10}\left(\frac{A_{dm}}{A_{DD}}\right)$$

$$\mathrm{PSRR}_{DD,\mathrm{dB}} = A_{dm,\mathrm{dB}} - A_{DD,\mathrm{dB}}$$

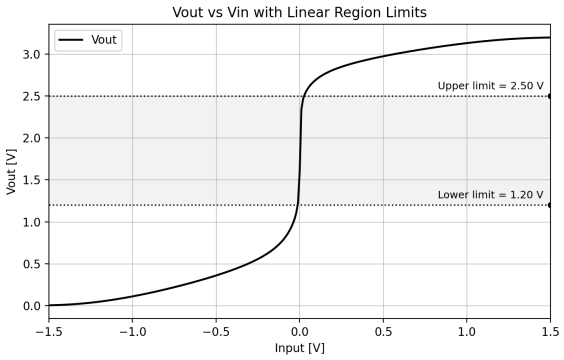
Frequency response of the power supplies rejection ratio PSRR [dB]



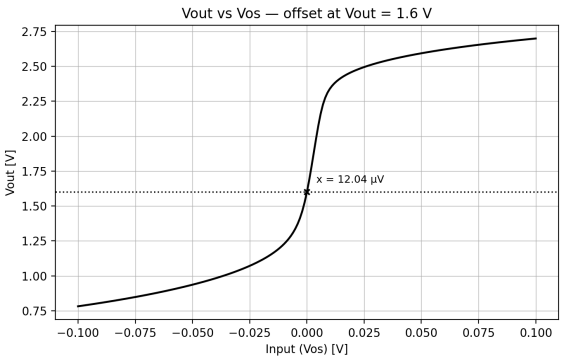
V_{DD} Positive and Negative PSRR [dB]

Figure 14: Overview of Power Supply Rejection Ratio [dB]

Input common mode voltage range and output dynamic range, voltage offset



Input voltage range and output dynamic range [V]



Voltage offset [V]

Figure 15: Overview summary of frequency domain simulations, voltage and dynamic range

For simulation of the voltage range and corresponding output range was used dc simulation with input voltage sweep. From shown graph we can say, that the input voltage range is from -0.1 V to 0.1 V. The output voltage range is defined from 1.2 V to 2.5 V. For the same simulation, we were able to obtain the offset voltage, which is shown in the Figure 15 on the second graph. The offset is 12.04 µV. I ideal situation

the voltage offset should be 0 V, but here we can see, that in real situation, that is not possible.

Time domain and slew rate observation

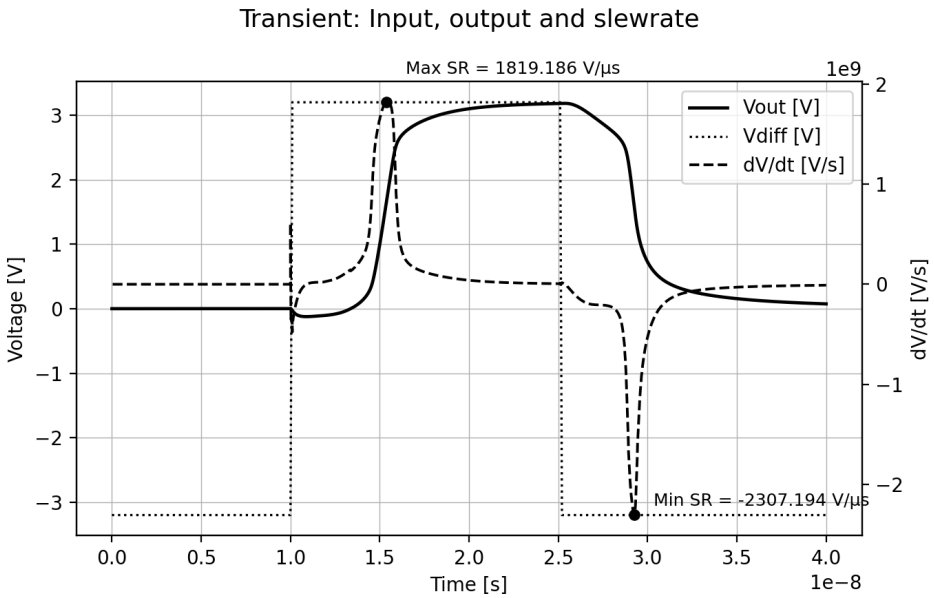


Figure 16: Time domain response of the circuit to the pulse, Slew rate [$V/\mu s$]

In the time domain, we obtained the response to an ideal input pulse. Due to the smaller frequency bandwidth, the final response of the operational amplifier is slower; for that reason, we were forced to extend the input pulse. The width of the pulse was extended to 15 ns. In the Figure 16 shows the input pulse, the output, and the derivative of the output. From the maximum and minimum values of the derivative, we can obtain the slew rate of the rising and falling edges. The slew rate for the rising edge is $1.82\ kV/\mu s$, and the slew rate for the falling edge is $-2.31\ kV/\mu s$.

Frequency domain, voltage and temperature dispersion

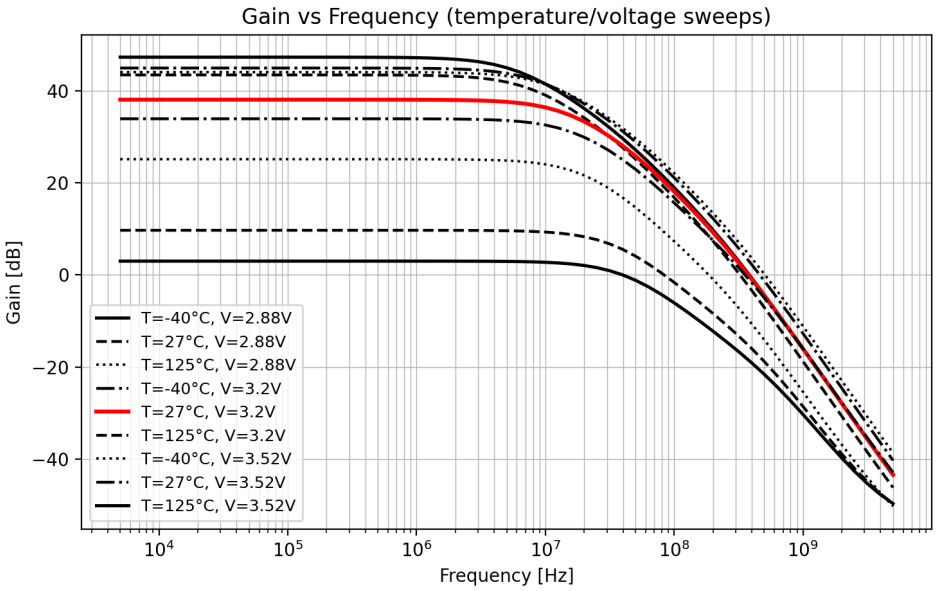


Figure 17: Voltage and temperature dispersion, results for different variants [dB]

The voltage and temperature dispersion simulation showed us different situations involving voltage and temperature fluctuations, as well as the response of the OpAmp gain. From Figure 17, it is evident that the temperature rapidly decreases the circuit's gain. Additionally, with a higher input voltage, the final gain decreases until it reaches almost 0 dB for lower frequencies. If we could obtain the temperature of $-40°$ and lower the input voltage, the gain would increase to above 40 dB. The influence of temperature and voltage variations is significant and cannot be neglected.

3 Layout

The layout of the operational amplifier is surrounded by metal pads, which would be used after production to connect the integrated circuit to external circuitry. This is visible in Figure 18. Each pad center has a distance of 120 µm to each other.

Figure 19 shows a close-up image of the layout. The PMOS are located near each other and are contained in the same n-well. They are surrounded by a guard ring. Together with the n-well it has a potential of V_{DD}, which protects the transistors from distortions, body effects and substrate current.

Three resistors are put in parallel which represent the original resistor. They each have a value of $R = 6.67\,\mathrm{k}\Omega$, together therefore approximating the value of $2.22\,\mathrm{k}\Omega$ very well. Similar to the PMOS, they are located in a n-well and have a separate guard ring surround them.

The NMOS are located to the bottom left and right of the PMOS and are also contained by guard rings. In contrast to the PMOS, the NMOS are not put in a separate well.

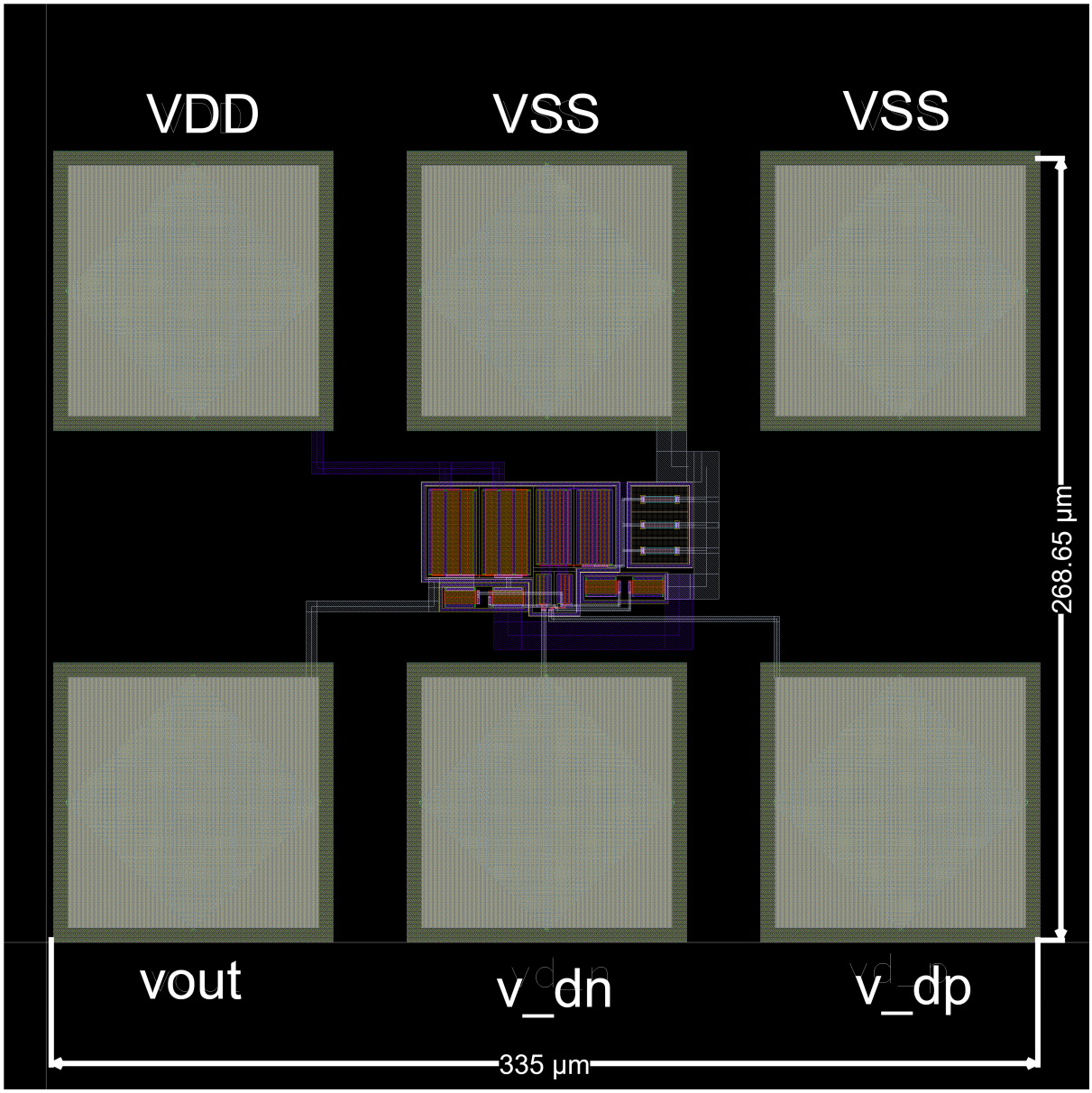


Figure 18: Layout of the operational amplifier

Instead, they are located in the p-type substrate of the wafer. The guard ring is now connected to V_{SS} for the same reasons as stated above.

The physical layout differs from the schematic. It brings parasitic capacitances with it, which influence the behavior of the operational amplifier. It is therefore important to extract those parasitics and re-simulate the most important characteristics. Figure 20 shows the testbench used, for which the operational amplifier is represented into a symbol.

Figure 21 demonstrates how the differential gain A_{DM} changes with the parasitics. The low-frequency gain remained roughly equal, however, the corner frequency reduced significantly to $f_{\mathrm{c}} = 3.94\,\mathrm{MHz}$. On a positive note, the parasitics also decrease the common mode gain A_{CM} in the high frequencies, as can be seen in Figure 22.

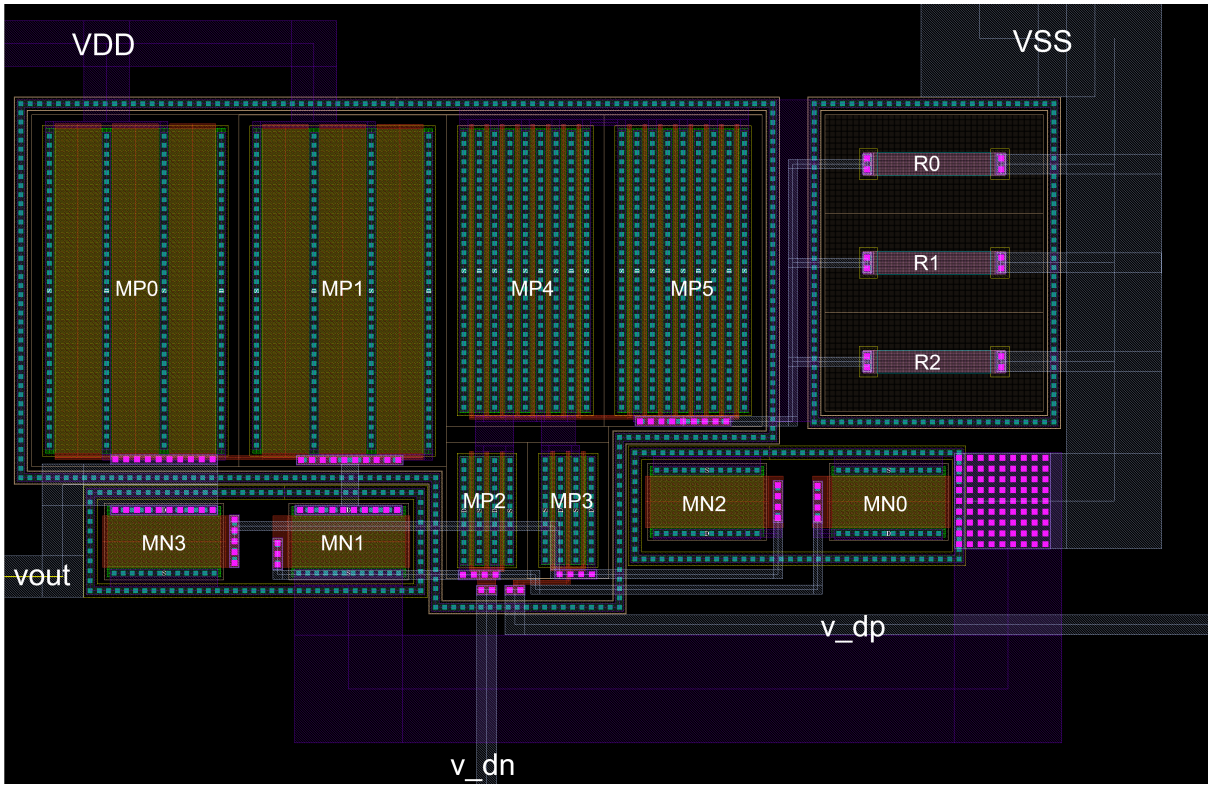


Figure 19: Close-up of the layout

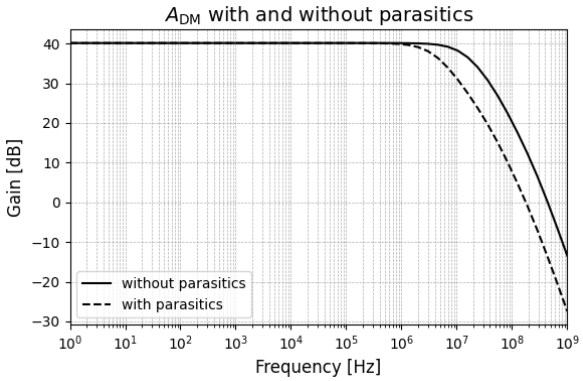


Figure 21: A_{DM} with and without parasitics

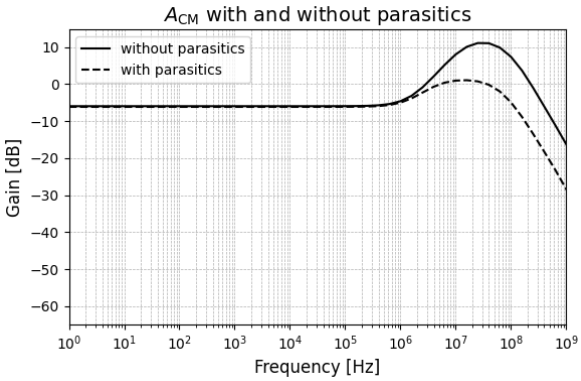


Figure 22: A_{CM} with and without parasitics

The $CMMR$ changes according to A_{DM} and A_{CM}, as Figure 24 shows. The parasitics cause it to increase in high frequencies due to the significantly reduced common mode gain A_{CM}. On the schematic in the Figure 23, the obtained values for parasitic capacitance from the physical layout are shown. The values of the parasitic capacitances are also shown clearly in Table 3. Parasitic capacitances appear on each node, and their value depends on the trace length, width, and layer placement. For example, we can see that the node VSS has the biggest impact on overall parasitic capacitance. From the layout on Figure 18 we can see that this trace has biggest width and length and up to all of that it also appears on layer Metal 1, which is the closest one to the substrate. The smallest capacitances have nodes v_cm and zz, which both have short traces, which only serve to connect transistors over short distances.

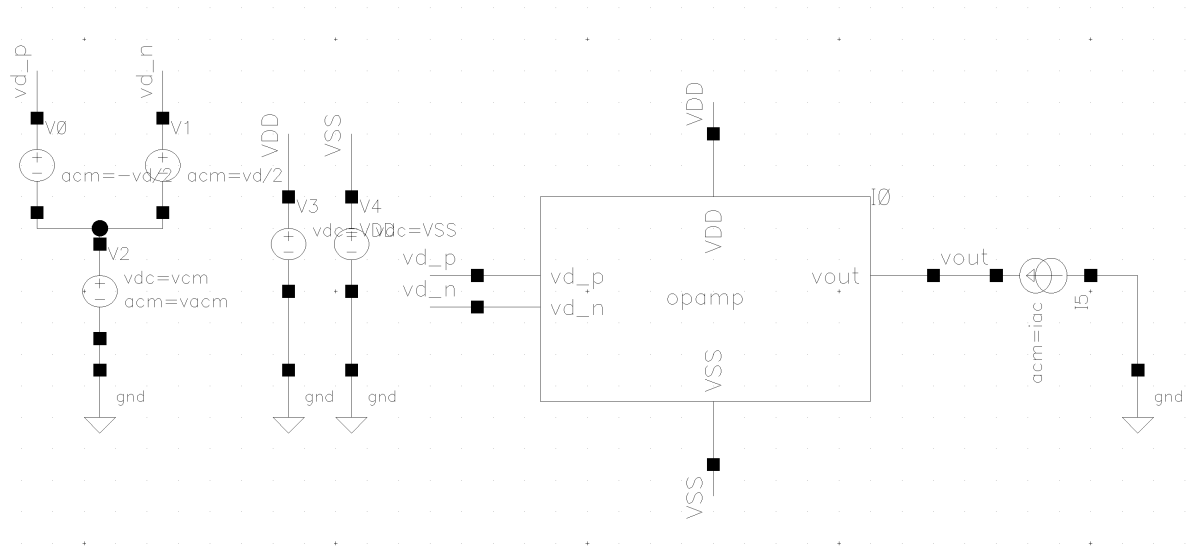


Figure 20: Testbench of schematic with parasitics

Table 3: Extracted Parasitic Capacitances of Important Nodes

Node	**Description**	**Capacitance [fF / pF]**
/zz	Internal node	24.83 fF
/vout	Output node	305.2 fF
/vd_p	Differential input (+)	300.3 fF
/vd_n	Differential input (–)	291.4 fF
/v_cm	Common-mode input	22.51 fF
/VSS	Ground reference	1.0 pF
/VDD	Supply rail	388.7 fF

The parasitics also have an effect on the phase margin of the operational amplifier. As Figure 25 demonstrates, the phase margin Φ_m when considering parasitics is increased from 22.37 to 35.07. This means that the parasitic capacitances slow the operational amplifier down, thereby increasing stability. With an increasing phase margin, the bandwidth slightly decreases. It does so, because the additional capacitances in the operational amplifier require time-consuming charging.

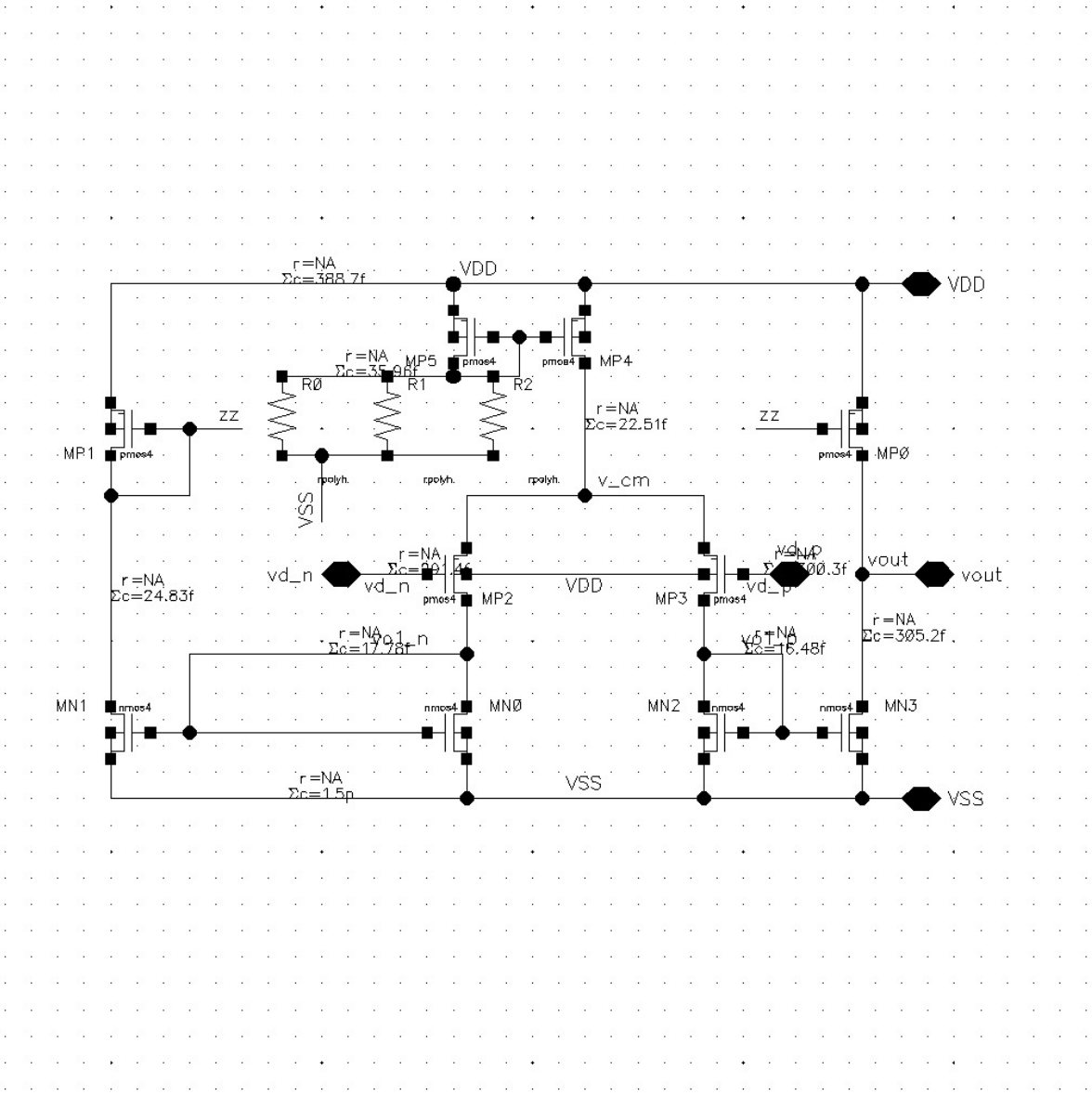


Figure 23: Schematic with parasitic values

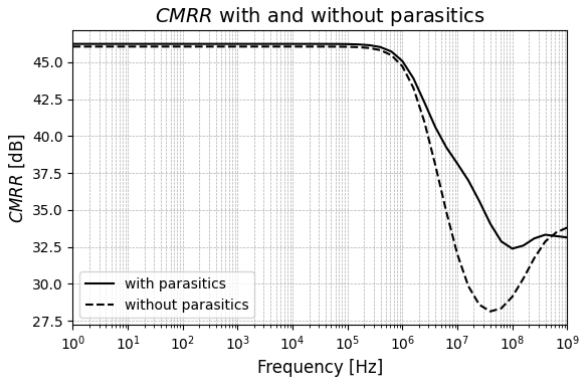


Figure 24: $CMRR$ with and without parasitics

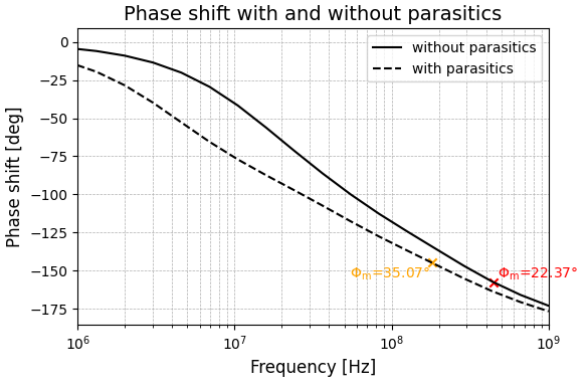


Figure 25: Phase shift and phase margins Φ_{m} with and without parasitics