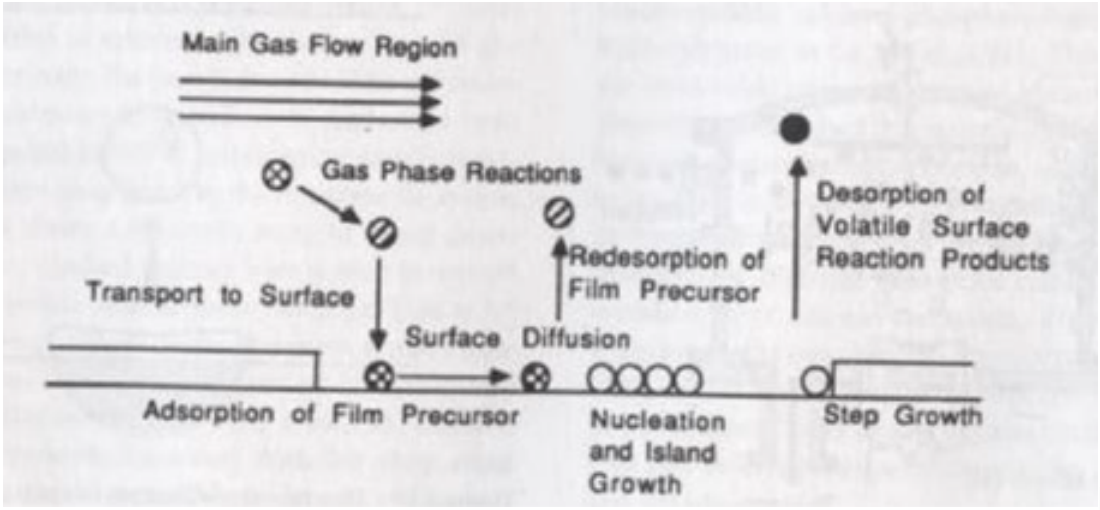
Keio University

1858

CALAMVS GLADIO FORTIOR

Miki Norihisa & Takahashi Hidetoshi's course - 2020

MEMS: design and fabrication
Report 4: Film deposition



[1]

Academic year 2019-2020
Tsuda Hiroyuki's Laboratory

Santacatterina Simon - 81923479

Contents

1 Introduction

The microfabrication of MEMS is divided into many different processes. At first, there is a Silicon wafer, on this one a thin film is deposited. Then the next step is to put, on top of the thin film, a photoresist coating which will react with UV light and create a particular pattern after the development process. Finally, an etching process is performed, using the photoresist layer as a mold, and then the photoresist layer is removed. Therefore, on the top of the Si wafer, we have a thin film with the same pattern as the one from the mold.

Various thin film deposition techniques exist. The choice of a particular technique in a particular process depends on factors such as: the film composition (material, purity), the adhesion, the thickness, the uniformity, the step coverage, and the deposition rate and cost. In this report, the thin film deposition techniques will be addressed to describe the following processes:

1. 0.5 μm of oxide layer on silicon substrate
2. 0.1 μm of poly silicon on oxide layer
3. 0.1 μm Au layer on oxide
4. 100 μm conductive layer (copper) + insulation layer on silicon wafer

2 0.5 μm of oxide layer on silicon substrate

2.1 Process

At first, there is a silicon substrate (wafer), on this substrate, there is a need for growing a layer of silicon dioxiode SiO_2. To perform this process, the substrate Si is heated up in a furnace and put into contact with other composite (brought with pipes), together they react through the oxidation reaction. There is two kind of reaction : wet oxidation and dry oxidation.

The chemical reaction of wet oxidation is:

$$\mathrm{Si} + 2\mathrm{H_2O} \longrightarrow \mathrm{SiO_2} + 2\mathrm{H_2}$$

For this reaction the reactants are Si and H_2O and the products are SiO_2 and H_2.

The chemical reaction of dry oxidation is:

$$\mathrm{Si} + \mathrm{O_2} \longrightarrow \mathrm{SiO_2}$$

For this reaction the reactants are Si and O_2 and the products is SiO_2.

More precisely, the Si is heated up to 1000°C in the furnace. In the case of dry oxidation, there is only one way for the reaction to take place, it is by introducing vaporized O_2, this reaction gives an oxide layer of high quality. In the case of wet oxidation, there are two possible reaction, the wet oxidation where vaporized H_2O is introduced and pyrogenic, where vaporized O_2 and H_2 are introduced and react to form the vaporized H_2O. The wet oxidation gives lower quality but has a higher growth rate. So the SiO_2 layer can be built faster.

So here **if the layer must be of high quality, dry oxidation will be used**, instead, **if the goal is to increase the growth rate (and reduce the overall reaction time) then wet oxidation must be used**.

2.2 Thickness and time

For the oxidation reaction, the relation between the consumed silicon thickness X_s and the produced oxide thickness X_{os} is :

$$X_s = 0.46 X_{ox} \tag{1}$$

Therefore for building a 0.5 μm of oxide layer a 0.46*0.5 = 0.23 μm thick silicon layer will be consumed.

Also an important characteristic of the process is the time is takes to produce the thickness. The equation is approximated by the following :

$$X_{ox} = \sqrt{Bt} \tag{2}$$

So the time is obtained, with B as a parameter by:

$$t = \frac{X_{ox}^2}{B} \tag{3}$$

Therefore for $X_{ox} = 0.5\ \mu m$ it gives

$$t = \frac{0.25}{B} \tag{4}$$

As said previously, the reaction time is bigger for dry oxidation then B should be smaller for dry than for wet oxidation.

2.3 Film adhesion

SiO_2 the film adhesion of this layer can be very well controlled because either surface treatment can be performed by heating, to release the water or other composite, or the control of residual stress by annealing is possible because it can be heated above 600°C.

3 0.1 μm of poly silicon on oxide layer

Here in the case of poly silicon dioxide, the process is different from the previous one. In this case, the aim is to build a thin layer of 0.1 μm. Another process is used it is the Chemical Vapor Deposition (CVD).

In this section, a quick explanation of the general process of CVD is done and then the choice and characteristics of the particular suitable process is made.

3.1 Process

CVD is such that the material to be grown is put into vapor phase, here it is the Si. This vapored compound is either transmitted like this or diluted with an inert carrier gas (inert therefore non reacting, just used as conveyor). Then, this gas is carried to the spot where it should be grown, at the surface. There is a transport to the surface and, at the surface interface, it reacts. More precisely, there is successively absorption of the film precursor, nucleation and growth of the poly-silicon layers. The other products, non included is the silicon layer are rejected and carried out by the transport gas.

A scheme of this process is displayed in figure 1.

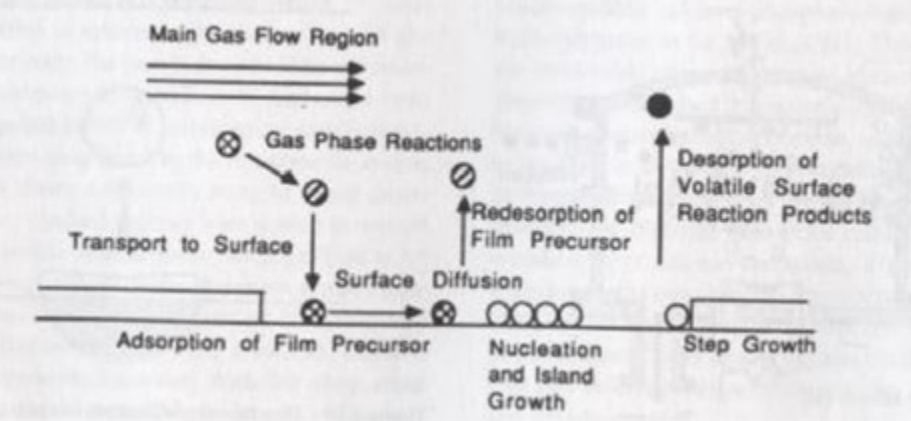


Figure 1: CVD process [1]

3.2 Final choice : LPCVD

In order to choose the LPCVD, it is required to look at the table summing up the CVD processes. This table shows that the most suitable process for growing poly-Si layers is the Low Pressure CVD. This table is displayed on figure 2.

TABLE 3.10 Review of CVD Processes

Process	Advantages	Disadvantages	Applications	Remark	Pressure/temp.
APCVD	Simple, high deposition rate, low temperature	Poor step coverage, particle contamination	Doped and undoped low-temperature oxides	Mass-transport controlled	100–10 kPa 350–400°C
LPCVD	Excellent purity and uniformity, conformable step coverage, large wafer capacity	High temperature and low deposition rate	Doped and undoped high temperature oxides, silicon nitride, poly-Si, W, WSi_2	Surface-reaction controlled	100 Pa 550–600°C
VLPCVD			Single-crystalline Si and compound semiconductor superlattices	Surface-reaction controlled	1.3 Pa
MOCVD	Excellent for epi on large surface areas	Safety concerns	Compound semiconductors for solar cells, laser, photocathodes, LEDs, HEMTs, and quantum wells	High volume, large surface area production	
PECVD	Lower substrate temperatures, fast, good adhesion, good step coverage, low pinhole density	Chemical (e.g., hydrogen) and particulate contamination	Low-temperature insulators over metals, passivation (nitride)	Tends to have more pinholes than LPCVD	2–5 Torr 300–400°C
Spray pyrolysis	Inexpensive	Difficult to control, not compatible with IC	Gas sensors, solar cells, ITO, large area		Atmospheric 100–180°C

Source: Adapted from K. F. Jensen, in *Microelectronics Processing*, D. W. Hess and K. F. Jensen, Eds., American Chemical Society, Washington, D.C., 1989;* and A. C. Adams, in *VLSI Technology*, S. M. Sze, Ed., McGraw-Hill, New York, 1988.[2]

Figure 2: CVD processes table [2]

As it is seen, the newly built layer has a excellent purity and uniformity, a comfortable step coverage and large wafer capacity. On the other hand, it requires high temperature and exhibit low deposition rate. The physical condition are 100 Pa for the pressure and $550 - 600°C$ for the temperature.

3.3 LPCVD : film adhesion

Another very important point of this technique is that the surface reaction is controlled during the formation. It means the adhesion properties can also be controlled.

Moreover this process gives a very high purity and uniformity. Therefore, the adhesion should be quite good. There might also be a possibility of annealing for the control of the residual stress.

4 0.1 μm Au layer on oxide

Here it is not anymore oxide that is required to be built but rather metals. Two techniques can be used for building thin layers of metals : Vapor deposition and Sputtering.

4.1 Vapor deposition

The set up of this process is displayed on figure 3.

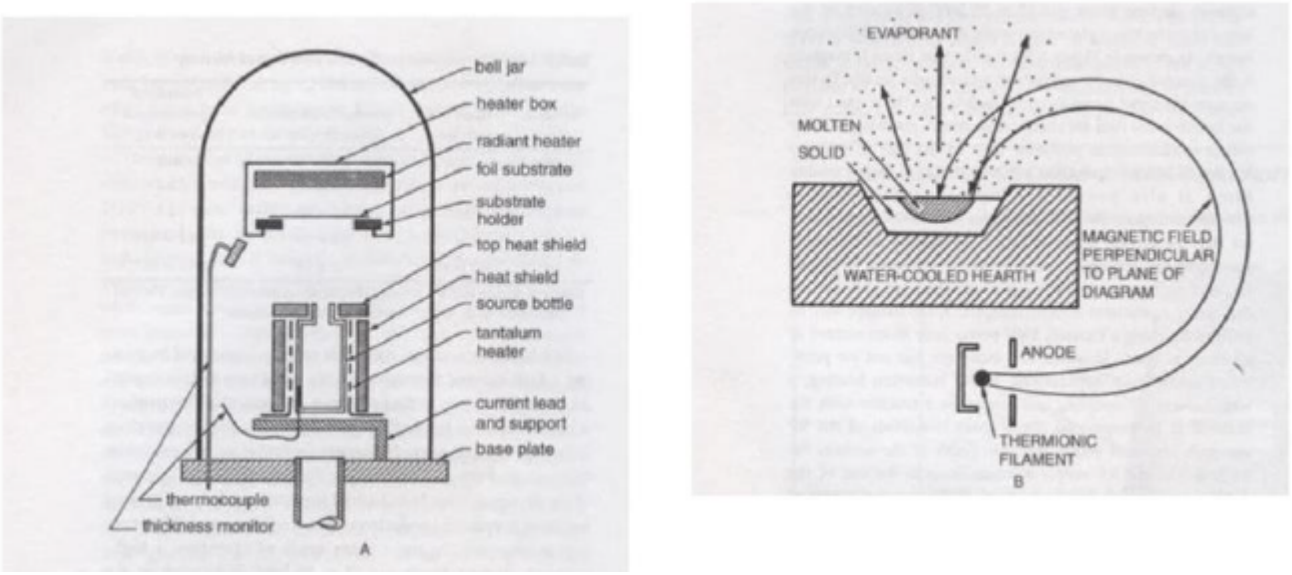


Figure 3: Vapor Deposition [3]

The explanation is rather simple. As seen on the left side of figure 3, the device is a bell jar, at 10^-4Pa. **But because the melting point of Au (gold) is really high, at** $1064°$**C, an e-beam is used to melt the gold and it is not melt by Resistive Heating.**. The metals is heated up, vaporized and flies straight up to the substrate where a film is created.

This process is simple, give a pure layer and fast. But in the case of gold, could induce a bad step coverage. Also it can't vaporized alloys, but this is not a concern here with Au.

4.2 Sputtering

The sputtering process is diplayed on figure 4.

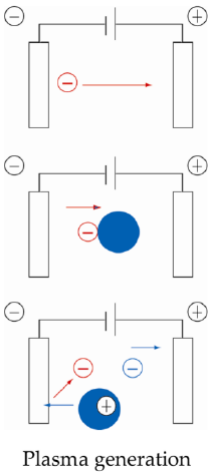


Figure 4: From top to bottom : the successive steps of sputtering [4]

This is how it goes:

1. On the left, negative electrode, the gold is put, on the right the oxide substrate is put and in the middle Argon gas. A potential is applied and electrons are extracted out of the cathode
2. Electrons, accelerated by the potential, collide with the argon atoms, on the way to the positive electrode. This creates a plasma.
3. the Argon + attracted by the cathode kicks gold atoms out of the layers and is it directed to the substrate

Different techniques than DC sputtering exist to enhanced the sputtering process : RF, magnetron.

This could allow surface cleaning and a better step coverage in our case. But is it complex and expensive.

4.3 Film adhesion

If anything as to be deposited on top of that:

In the case of building this 0.1 μm Au layer on oxide, the sputtering would allow to obtain a better film adhesion as we could use the surface treatment property of sputter etch.

But normally as the layer is made up of gold with a very meting point (1064°C), it should be possible to either heat the surface for surface treatment or do the annealing for releasing the residual stress and obtain better adhesion properties.

Between this layer and the oxide :

Contact metal is used. A possibility would be, as said in the course to use a first layer of Ti (titanium) also brought by Vapor Deposition

4.4 Final choice : Vapor deposition

Here, the target material to be layered is gold. Therefore it is not an alloy, and the final composition will be the same as the initial (only one kind of atom). By using sputtering it wouldn't gain anything about the final material composition or about using a material we couldn't use through Vapor Deposition. Also, by supposing the target is small, there is not gain in using a large sputter area. The only gains are about the step coverage and the cleaning of the surface.

So unless the application requires a very good step coverage and to have a good cleaning of the surface I would choose, the simple, quick and cheap option of Vapor Deposition with e-beam. Rather than the complex and expensive sputtering. Also because as student we don't have a lot of money so we need to save it

5 100 μm conductive layer (copper) + insulation layer on silicon wafer

5.1 Process

An example of this process can be seen on figure 5.

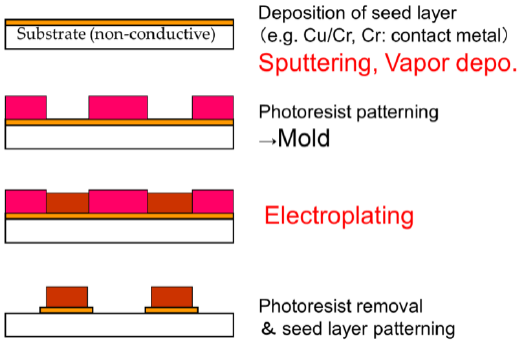


Figure 5: Example of electroplating on a insulation layer [5]

At first there is the deposit of the insulator layer, let's choose an oxide.

So here, before performing the electroplating, it is necessary to deposit a seed layer (conductive) to provide electron to the interface of the solution and the substrate surface. In other word, **it is necessary to have the first layer of conductive material, to play the role of the electrode, so that the Cu ions can agglomerate. In the case of Cu the seed layer is Cr (Chromium).**. Therefore Chromium is deposited through the Vapor Deposition process before the electrolating takes place. And then Cu also by vapor deposition. Now, the seed layer is built and the electroplating can take place.

Then, a mold can be used for creating special pattern but here for a simple layer it is not required.

And then the electroplating process takes place in a solution with a Cu electrodes then at the anode the reaction is :

$$\mathrm{Cu} \longrightarrow \mathrm{Cu}^{2+} + 2\mathrm{e}^{-}$$

And at the cathode it is :

$$\mathrm{Cu}^{2+} + 2\mathrm{e}^{-} \longrightarrow \mathrm{Cu}$$

Using this technique, a 100 μm conductive layer (copper) is built on an insulation layer on Si wafer. A remark that can be done is that this process can be controlled by the current from the source and the time of the reaction.

5.2 Film adhesion

The layer is very thick therefore there is a low residual stress, meaning potentially a good adhesion.

Also Copper as a melting point of 1085°C and Chromium 1907°C it should therefore be possible to have a surface treatment by heating or reduce the residual stress by annealing.

6 Conclusion

Through this report, the techniques used in thin film deposition for MEMS were covered for 4 particular cases. Step by step, is proper fabrication techniques were used through clear justifications. Those are the following:

1. Silicon oxydation for 0.5 μm of oxide layer on silicon substrate
2. LPCVD for 0.1 μm of poly silicon on oxide layer
3. Vapor deposition for 0.1 μm Au layer on oxide
4. Electroplating with seed layer for 100 μm conductive layer (copper) + insulation layer on silicon wafer

References

[1] Miki Norihisa & Takahashi Hidetoshi's slides of "MEMS: design and fabrication" course. Course #4, slide #5.

[2] Miki Norihisa & Takahashi Hidetoshi's slides of "MEMS: design and fabrication" course. Course #4, slide #6.

[3] Miki Norihisa & Takahashi Hidetoshi's slides of "MEMS: design and fabrication" course. Course #4, slide #8.

[4] Miki Norihisa & Takahashi Hidetoshi's slides of "MEMS: design and fabrication" course. Course #4, slide #11.

[5] Miki Norihisa & Takahashi Hidetoshi's slides of "MEMS: design and fabrication" course. Course #4, slide #15.