Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical /Oral	Tutorial	Total
ITC405	Computer Organization and Architecture	03	--	--	03	--	--	03

Course Code	Course Name	Examination Scheme						
		Theory Marks				Term Work	Pract. /Oral	Total
		Internal assessment			End Sem. Exam			
		Test1	Test 2	Avg.				
ITC405	Computer Organization and Architecture	20	20	20	80	--	--	100

Course Objectives:

Sr. No.	Course Objectives
The course aims:	
1	Learn the fundamentals of Digital Logic Design.
2	Conceptualize the basics of organizational and features of a digital computer.
3	Study microprocessor architecture and assembly language programming.
4	Study processor organization and parameters influencing performance of a processor.
5	Analyse various algorithms used for arithmetic operations.
6	Study the function of each element of memory hierarchy and various data transfer techniques used in digital computer.

Course Outcomes:

Sr. No.	Course Outcomes	Cognitive levels of attainment as per Bloom's Taxonomy
On successful completion, of course, learner/student will be able to:		
1	Demonstrate the fundamentals of Digital Logic Design	L1, L2
2	Describe basic organization of computer, the architecture of 8086 microprocessor and implement assembly language programming for 8086 microprocessors.	L1
3	Demonstrate control unit operations and conceptualize instruction level parallelism.	L1, L2
4	List and Identify integers and real numbers and perform computer arithmetic operations on integers.	L1,L4
5	Categorize memory organization and explain the function of each element of a memory hierarchy.	L4
6	Examine different methods for computer I/O mechanism.	L3

Prerequisite: Basics of Electrical Engineering, Fundamentals of Computer.

DETAILED SYLLABUS:

Sr. No.	Module	Detailed Content	Hours	CO Mapping
0	**Prerequisite**	Basics of Electrical Engineering, Fundamentals of Computer	**02**	
I	**Fundamentals of Logic Design**	Number systems: Introduction to Number systems, Binary Number systems, Signed Binary Numbers, Binary, Octal, Decimal and Hexadecimal number and their conversions, 1's and 2's complement Combinational Circuits: NOT,AND,OR,NAND,NOR,EX-OR,EX-NOR Gates. Half & Full Adder and subtractor, Reduction of Boolean functions using K-map method (2,3,4 Variable), introduction to Multiplexers and Demultiplexers, Encoders & Decoders. Sequential Circuits: Introduction to Flip Flops: SR, JK, D, T, master slave flip flop, Truth Table. **Self-learning Topics:** Number System, Quine-McCluskey,Flip-Flop conversion, Counter Design.	**07**	CO1
II	**Overview of Computer Architecture & Organization**	Introduction of Computer Organization and Architecture. Basic organization of computer and block level description of the functional units. Evolution of Computers, Von Neumann model. Performance measure of Computer Architecture, Amdahl's Law Architecture of 8086 Family, Instruction Set, Addressing Modes, Assembler Directives, Mixed-Language Programming, Stack, Procedure, Macro. **Self-learning Topics:** Interfacing of I/O devices with 8086(8255,ADC,DAC).	**08**	CO2
III	**Processor Organization and Architecture**	CPU Architecture, Instruction formats, basic instruction cycle with Interrupt processing. Instruction interpretation and sequencing. Control Unit: Soft wired (Microprogrammed) and hardwired control unit design methods. Microinstruction sequencing and execution. Micro operations, concepts of nano programming. Introduction to parallel processing concepts, Flynn's classifications, instruction pipelining, pipeline hazards. **Self-learning Topics**: Study the examples on instruction pipelining for practice.	**07**	CO3
IV	**Data Representation and Arithmetic Algorithms**	Booth's algorithm. Division of integers: Restoring and non-restoring division, signed division, basics of floating-point representation IEEE 754 floating point (Single & double precision) number representation. **Self-learning Topics:** Implement Booth's Algorithm and Division methods.	**04**	CO4
V	**Memory Organization**	Introduction to Memory and Memory parameters. Classifications of primary and secondary memories. Types of RAM and ROM, Allocation policies, Memory hierarchy and characteristics. Cache memory: Concept, architecture (L1, L2, L3), mapping techniques. Cache Coherency, Interleaved and Associative memory	**07**	CO5

		Self-learning Topics: Case study on Memory Organization, Numerical on finding EAT, Address mapping.		
VI	**I/O Organization**	Input/output systems, I/O module-need & functions and Types of data transfer techniques: Programmed I/O, Interrupt driven I/O and DMA **Self-learning Topics:** Comparison of all I/O methods.	**04**	CO6

Text Books:

1. R. P. Jain,"Modern Digital Electronics", TMH
2. M. Morris Mano,"Digital Logic and Computer Design", PHI
3. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, Computer Organization, Fifth Edition, TataMcGraw-Hill.
4. William Stallings, Computer Organization and Architecture: Designing for Performance, EighthEdition,, Pearson
5. John Uffenbeck, 8086/8088 family: Design Programming and Interfacing, (Pearson Education

References:

1. A. Anand Kumar, "Fundamentals of Digital Circuits",. PHI
2. Donald P Leach, Albert Paul Malvino, "Digital Principals & Applications", TMH.
3. B. Govindarajulu,, Computer Architecture and Organization: Design Principles and Applications,Computer Architecture and Organization: Design Principles and Applications, Tata McGraw-Hill
4. Dr. M. Usha, T. S. Srikanth, Computer System Architecture and Organization, First Edition,Wiley-India.
5. John P. Hayes, Computer Architecture and Organization, Third Edition., McGraw-Hill
6. K Bhurchandi, Advanced Microprocessors & Peripherals, Tata McGraw-Hill Education

Online References:

Sr. No.	Website Name
1.	https://www.nptel.ac.in
2.	https://www.geeksforgeeks.org
3.	https://www.coursera.org/

Assessment:

Internal Assessment (IA) for 20 marks:

- IA will consist of Two Compulsory Internal Assessment Tests. Approximately 40% to 50%of syllabus content must be covered in First IA Test and remaining 40% to 50% of syllabuscontent must be covered in Second IA Test

➢ **Question paper format**

- Question Paper will comprise of a total of **six questions each carrying 20 marks Q.1** willbe **compulsory** and should **cover maximum contents of the syllabus**

- **Remaining questions** will be **mixed in nature** (part (a) and part (b) of each question mustbe from different modules. For example, if Q.2 has part (a) from Module 3 then part (b) must be from any other Module randomly selected from all the modules)

- A total of **four questions** need to be answered