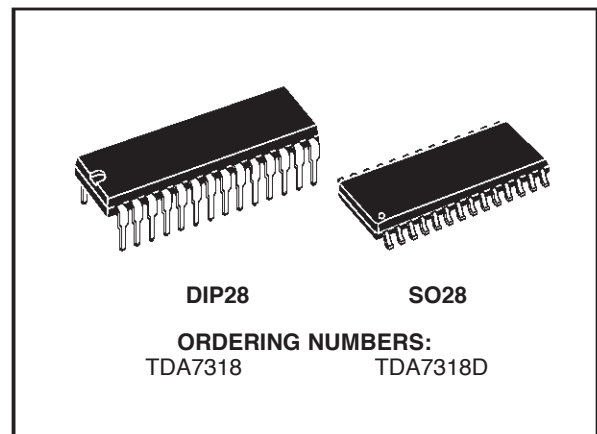


DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

- INPUT MULTIPLEXER:
 - 4 STEREO INPUTS
 - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTION TO DIFFERENT SOURCES
- INPUT AND OUTPUT FOR EXTERNAL EQUALIZER OR NOISE REDUCTION SYSTEM
- VOLUME CONTROL IN 1.25dB STEPS
- TREBLE AND BASS CONTROL
- FOUR SPEAKER ATTENUATORS:
 - 4 INDEPENDENT SPEAKERS CONTROL IN 1.25dB STEPS FOR BALANCE AND FADER FACILITIES
 - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL I²C BUS

DESCRIPTION

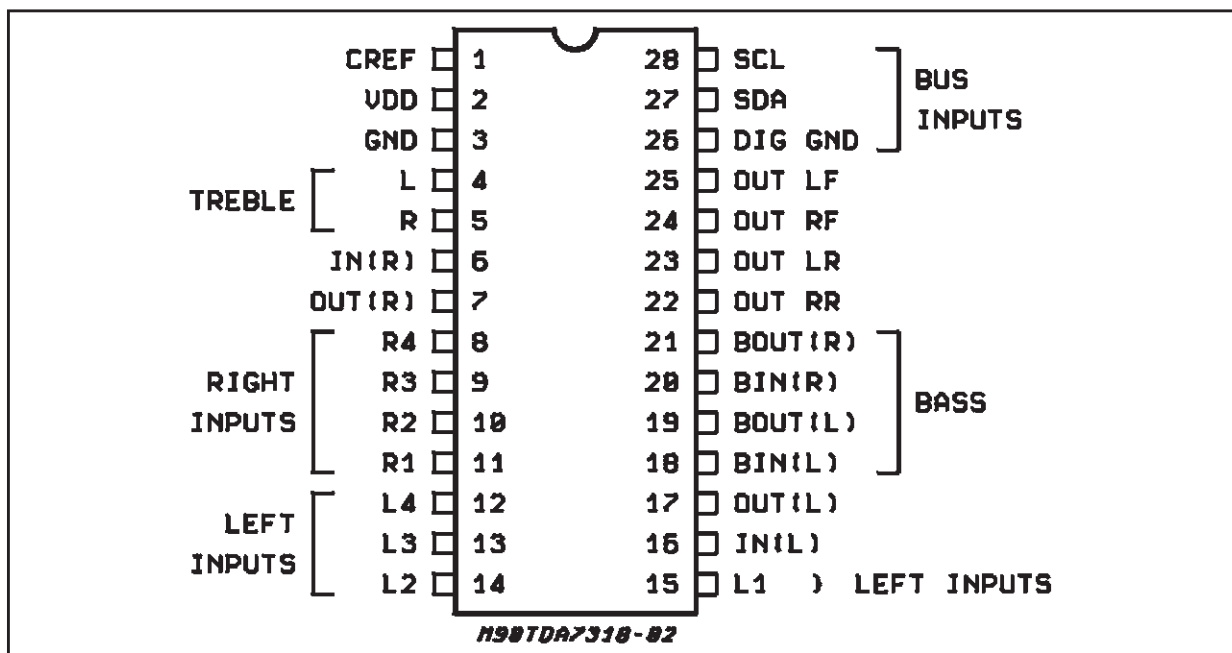
The TDA7318 is a volume, tone (bass and treble) balance (Left/Right) and fader (front/rear) processor for quality audio applications in car radio and Hi-Fi systems.



Selectable input gain is provided. Control is accomplished by serial I²C bus microprocessor interface. The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

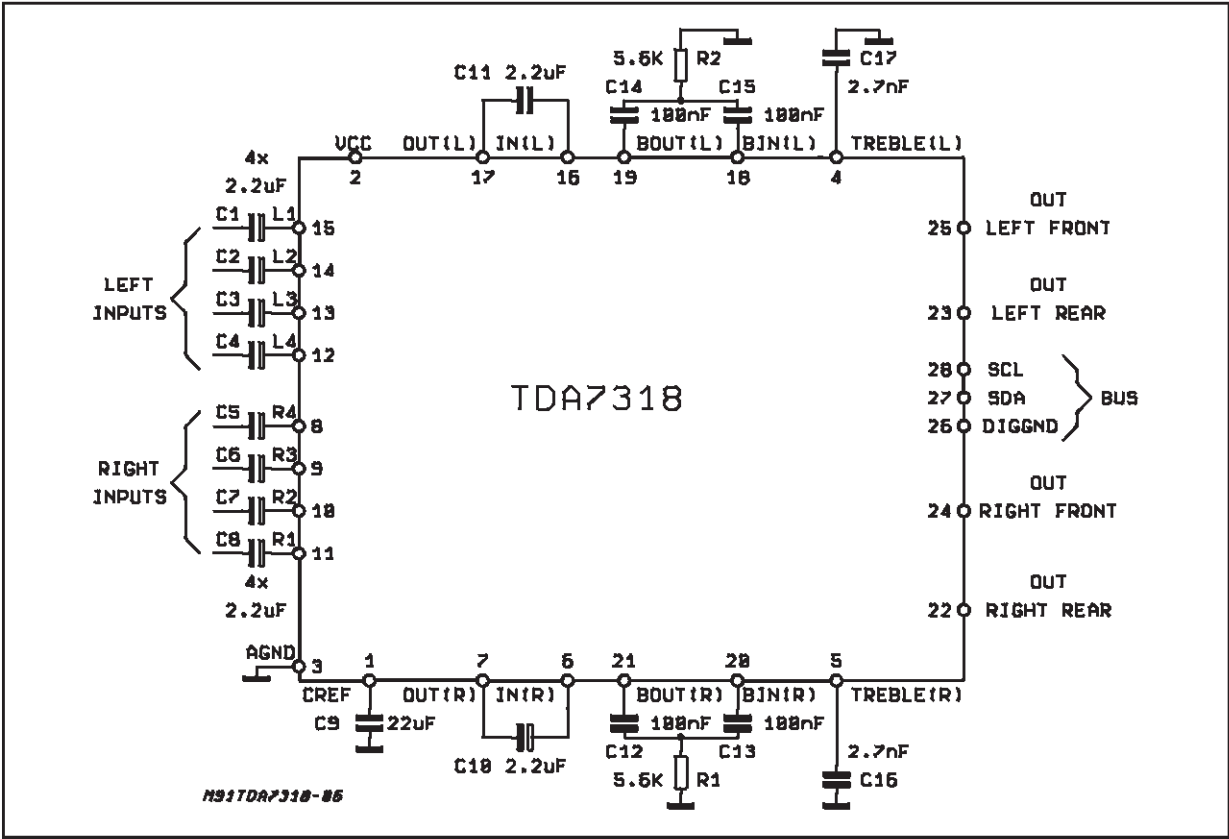
Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and Low DC stepping are obtained.

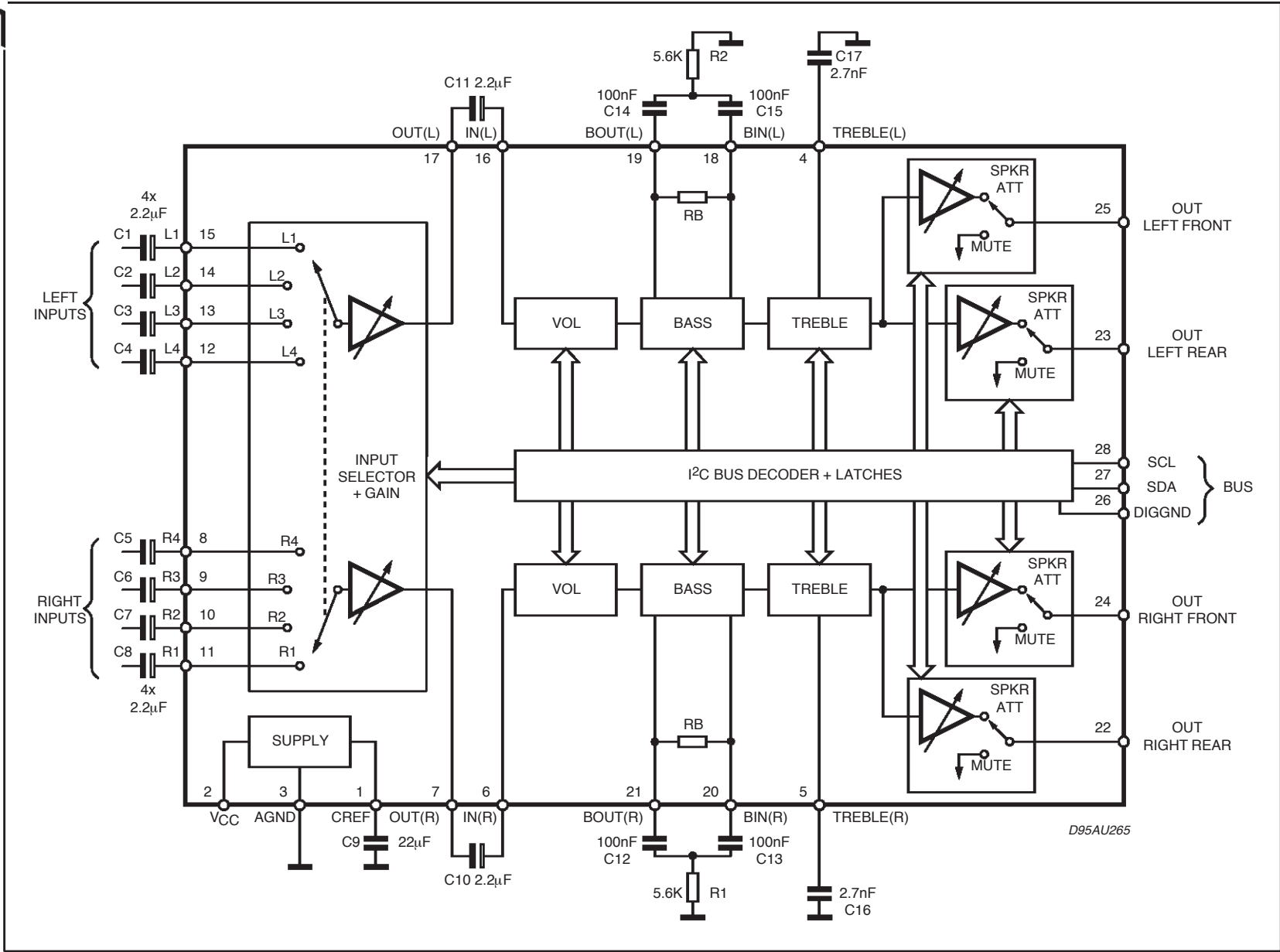
PIN CONNECTION (Top view)



TDA7318

TEST CIRCUIT





TDA7318

ELECTRICAL CHARACTERISTICS (refer to the test circuit $T_{amb} = 25^{\circ}\text{C}$, $V_S = 9\text{V}$, $R_L = 10\text{K}\Omega$, $R_G = 600\Omega$, all controls flat ($G = 0$), $f = 1\text{KHz}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

SUPPLY

V_S	Supply Voltage		6	9	10	V
I_S	Supply Current		4	8	11	mA
SVR	Ripple Rejection		60	85		dB

INPUT SELECTORS

R_{II}	Input Resistance	Input 1, 2, 3, 4	35	50	70	$\text{K}\Omega$
V_{CL}	Clipping Level		2	2.5		Vrms
S_{IN}	Input Separation (2)		80	100		dB
R_L	Output Load resistance	pin 7, 17	2			$\text{K}\Omega$
G_{INmin}	Min. Input Gain		-1	0	1	dB
G_{INmax}	Max. Input Gain		17	18.75	20	dB
G_{STEP}	Step Resolution		5	6.25	7.5	dB
e_{IN}	Input Noise	$G = 18.75\text{dB}$		2		μV
V_{DC}	DC Steps	adjacent gain steps		4	20	mV
		$G = 18.75$ to Mute		4		mV

VOLUME CONTROL

R_{IV}	Input Resistance		20	33	50	$\text{k}\Omega$
C_{RANGE}	Control Range		70	75	80	dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		70	75	80	dB
A_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation Set Error	$A_v = 0$ to -20dB	-1.25	0	1.25	dB
		$A_v = -20$ to -60dB	-3		2	dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	adjacent attenuation steps		0	3	mV
		From 0dB to A_v max		0.5	7.5	mV

SPEAKER ATTENUATORS

C_{range}	Control Range		35	37.5	40	dB
S_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation set error				1.5	dB
A_{MUTE}	Output Mute Attenuation		80	100		dB
V_{DC}	DC Steps	adjacent att. steps		0	3	mV
		from 0 to mute		1	10	mV

BASS CONTROL (1)

G_b	Control Range	Max. Boost/cut	± 12	± 14	± 16	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		34	44	58	$\text{K}\Omega$

TREBLE CONTROL (1)

G_t	Control Range	Max. Boost/cut	± 13	± 14	± 15	dB
T_{STEP}	Step Resolution		1	2	3	dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AUDIO OUTPUTS						
V_{OCL}	Clipping Level	$d = 0.3\%$	2	2.5		Vrms
R_L	Output Load Resistance		2			K Ω
C_L	Output Load Capacitance				10	nF
R_{OUT}	Output resistance		30	75	120	Ω
V_{OUT}	DC Voltage Level		4.2	4.5	4.8	V

GENERAL

e_{NO}	Output Noise	BW = 20-20KHz, flat output muted all gains = 0dB		2.5 5	15	μV μV
		A curve all gains = 0dB		3		μV
S/N	Signal to Noise Ratio	all gains = 0dB; $V_O = 1V_{rms}$		106		dB
d	Distortion	$A_V = 0, V_{IN} = 1V_{rms}$		0.01	0.1	%
		$A_V = -20dB, V_{IN} = 1V_{rms}$		0.09	0.3	%
		$V_{IN} = 0.3V_{rms}$		0.04		%
Sc	Channel Separation left/right		80	103		dB
	Total Tracking error	$A_V = 0$ to $-20dB$		0	1	dB
		-20 to -60 dB		0	2	dB

BUS INPUTS

V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	μA
V_O	Output Voltage SDA Acknowledge	$I_O = 1.6mA$			0.4	V

Notes:

- (1) Bass and Treble response see attached diagram (fig.19). The center frequency and quality of the resonance behaviour can be chosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network
- (2) The selected input is grounded thru the 2.2 μF capacitor.

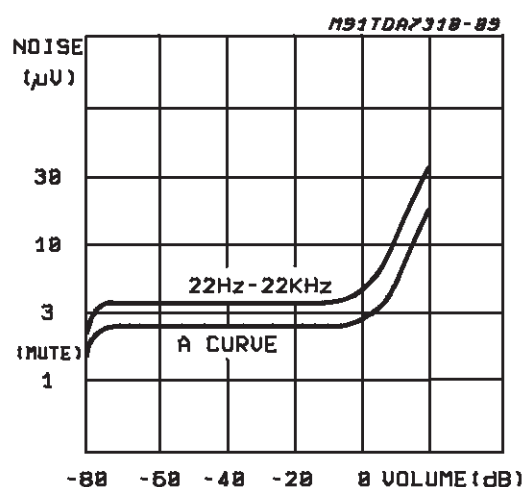
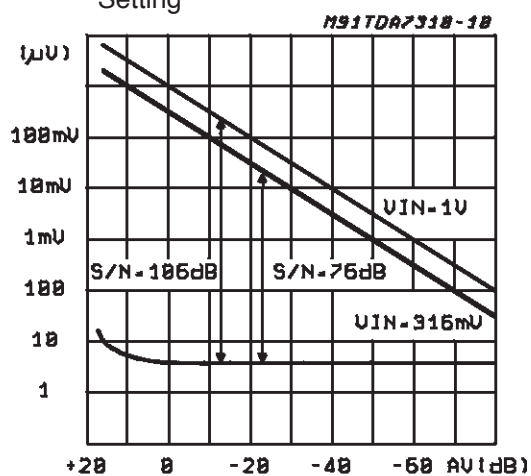
Figure 1: Noise vs. Volume/Gain Settings**Figure 2: Signal to Noise Ratio vs. Volume Setting**

Figure 3: Distortion & Noise vs. Frequency

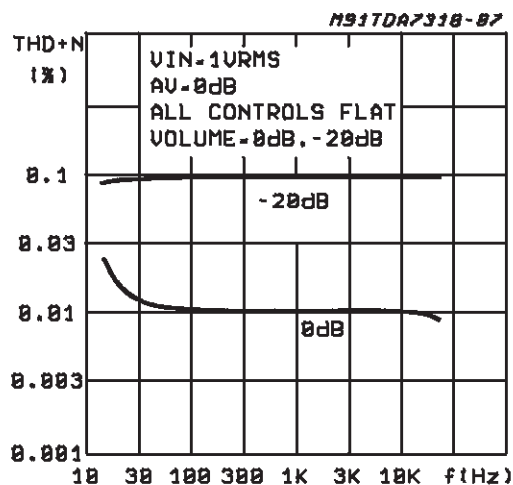


Figure 4: Distortion & Noise vs. Frequency

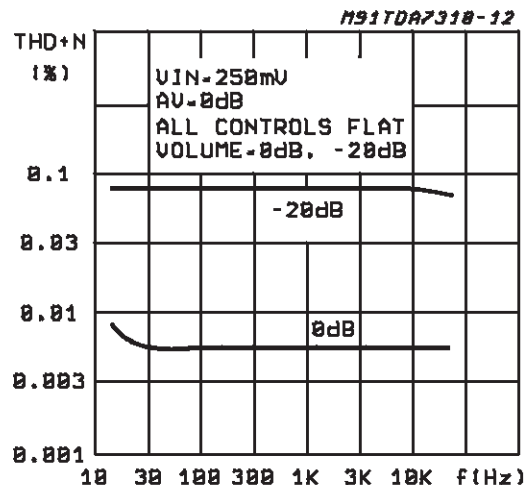


Figure 5: Distortion vs. Load Resistance

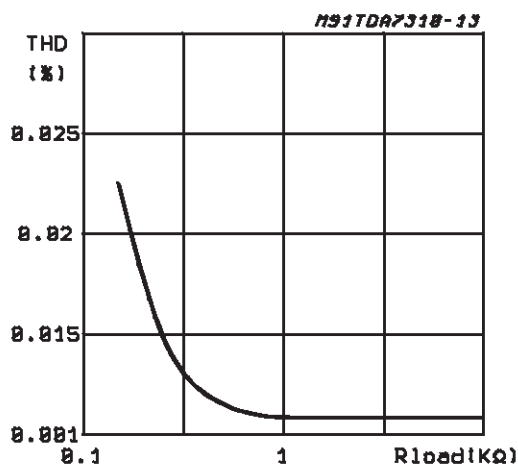


Figure 6: Channel Separation (L → R) vs. Frequency

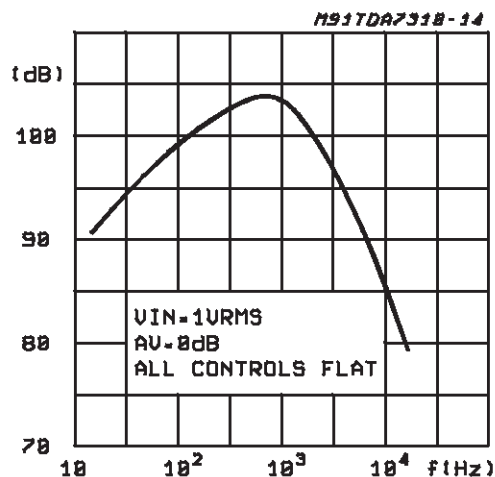


Figure 7: Input Separation (L1 → L2, L3, L4) vs. Frequency

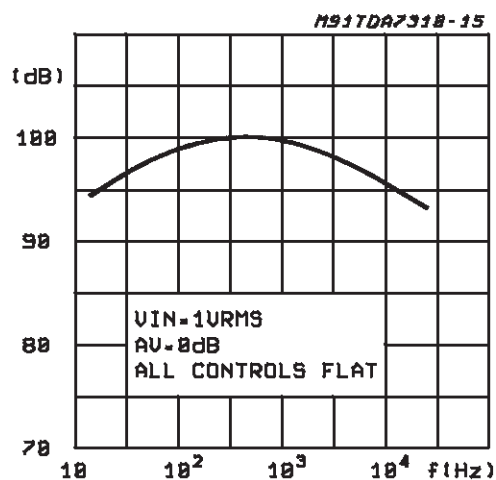


Figure 8: Supply Voltage Rejection vs. Frequency

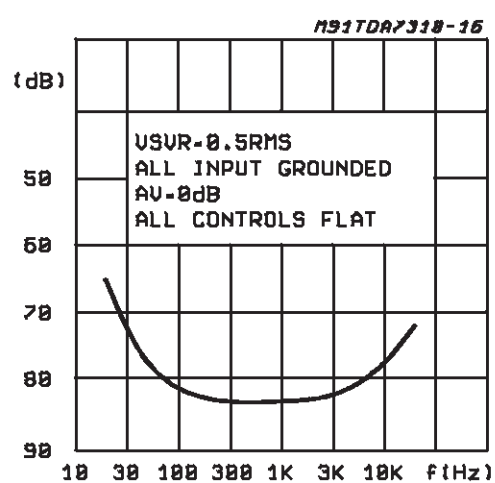


Figure 9: Output Clipping Level vs. Supply Voltage

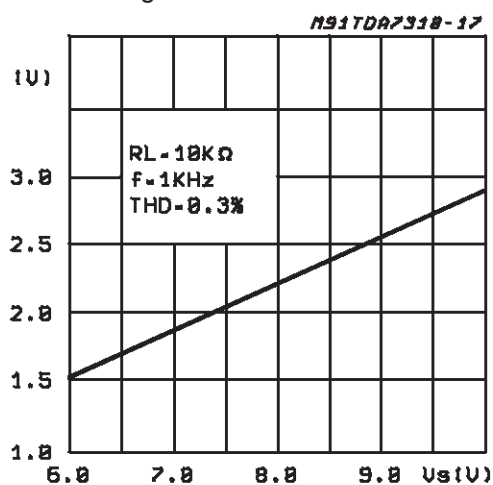


Figure 10: Quiescent Current vs. Supply Voltage

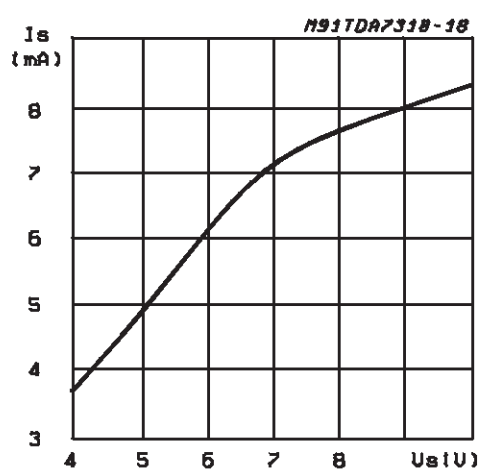


Figure 11: Supply Current vs. Temperature

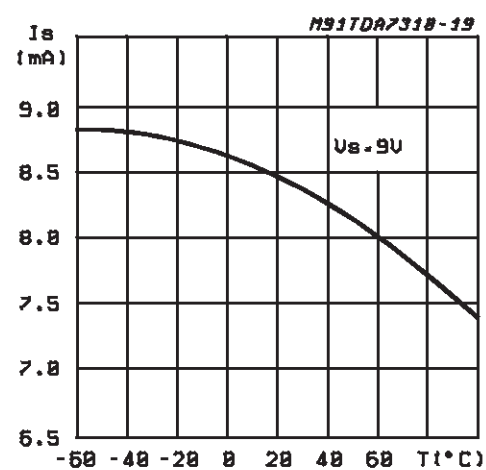


Figure 12: Bass Resistance vs. Temperature

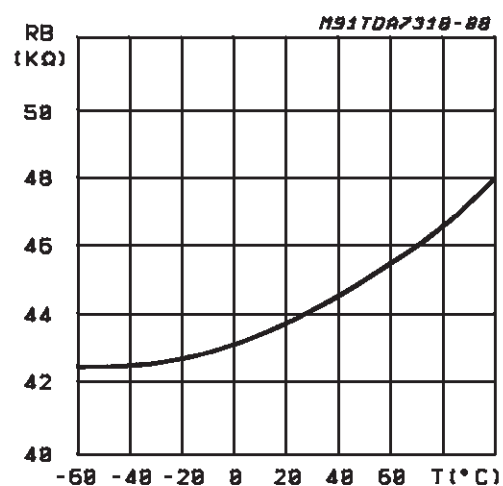
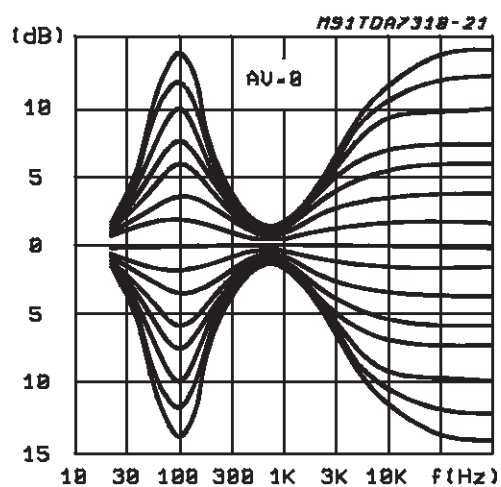


Figure 13: Typical Tone Response (with the ext. components indicated in the test circuit)



I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7318 and viceversa takes place thru the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown in fig. 14, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.15 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an ac-

knowledge bit. The MSB is transferred first.

Acknowledge

The master (μ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 16). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the μ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Figure 14: Data Validity on the I²C BUS

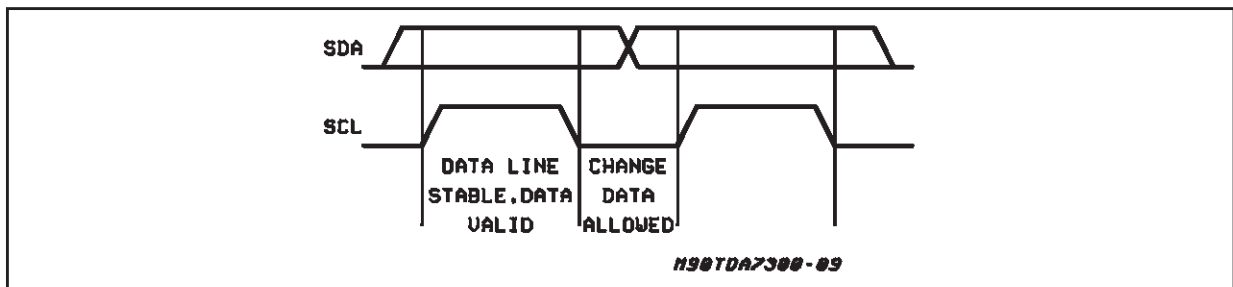


Figure 15: Timing Diagram of I²C BUS

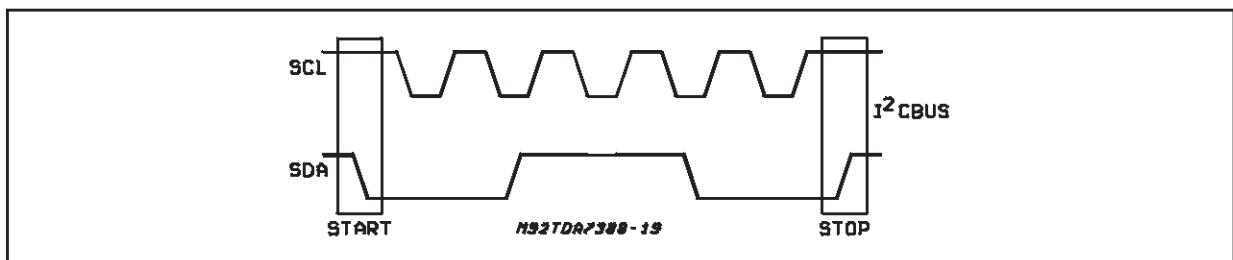
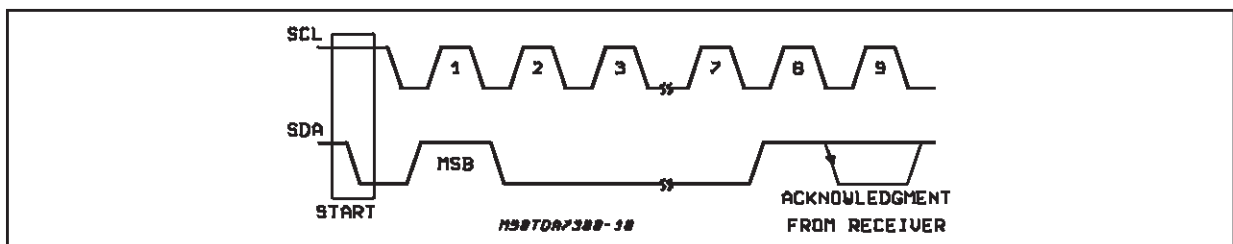


Figure 16: Acknowledge on the I²C BUS



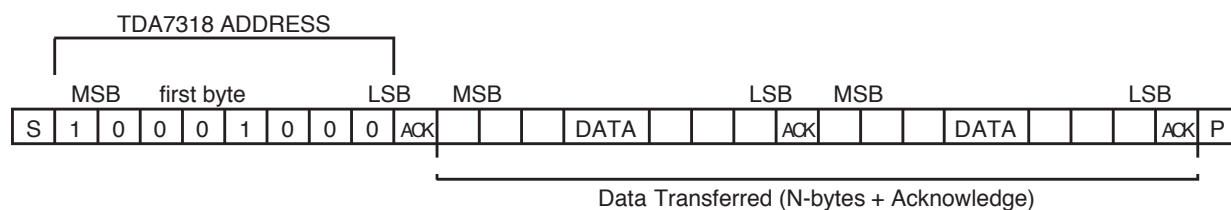
SOFTWARE SPECIFICATION**Interface Protocol**

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7318

address (the 8th bit of the byte must be 0). The TDA7318 must always acknowledge at the end of each transmitted byte.

- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

MAX CLOCK SPEED 100kb/s

SOFTWARE SPECIFICATION

Chip address

1	0	0	0	1	0	0	0
MSB							LSB

DATA BYTES

MSB								LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	A0	Volume control
1	1	0	B1	B0	A2	A1	A0	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	A0	Speaker ATT RF
0	1	0	G1	G0	S2	S1	S0	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	C0	Bass control
0	1	1	1	C3	C2	C1	C0	C0	Treble control

Ax = 1.25dB steps; Bx = 10dB steps; Cx = 2dB steps; Gx = 6.25dB steps

SOFTWARE SPECIFICATION (continued)

DATA BYTES (detailed description)

Volume

MSB			LSB			FUNCTION
0	0	B2 B1 B0	A2 A1 A0	Volume 1.25dB steps		
			0 0 0	0		
			0 0 1	-1.25		
			0 1 0	-2.5		
			0 1 1	-3.75		
			1 0 0	-5		
			1 0 1	-6.25		
			1 1 0	-7.5		
			1 1 1	-8.75		
0	0	B2 B1 B0	A2 A1 A0	Volume 10dB steps		
		0 0 0		0		
		0 0 1		-10		
		0 1 0		-20		
		0 1 1		-30		
		1 0 0		-40		
		1 0 1		-50		
		1 1 0		-60		
		1 1 1		-70		

For example a volume of -45dB is given by:

0 0 1 0 0 1 0 0

Speaker Attenuators

MSB							LSB		FUNCTION
1	0	0	B1	B0	A2	A1	A0	Speaker LF	
1	0	1	B1	B0	A2	A1	A0	Speaker RF	
1	1	0	B1	B0	A2	A1	A0	Speaker LR	
1	1	1	B1	B0	A2	A1	A0	Speaker RR	
					0	0	0	0	
					0	0	1	-1.25	
					0	1	0	-2.5	
					0	1	1	-3.75	
					1	0	0	-5	
					1	0	1	-6.25	
					1	1	0	-7.5	
					1	1	1	-8.75	
					0	0		0	
					0	1		-10	
					1	0		-20	
					1	1		-30	
			1	1	1	1	Mute		

For example attenuation of 25dB on speaker RF is given by:

1 0 1 1 0 1 0 0

Audio Switch

MSB			LSB					FUNCTION
0	1	0	G1	G0	S2	S1	S0	Audio Switch
					0	0	0	Stereo 1
					0	0	1	Stereo 2
					0	1	0	Stereo 3
					0	1	1	Stereo 4
					1	0	0	Not allowed
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				+18.75dB
			0	1				+12.5dB
			1	0				+6.25dB
			1	1				0dB

For example to select the stereo 2 input with a gain of +12.5dB the 8bit string is:

0 1 0 0 1 0 0 1

Bass and Treble

0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

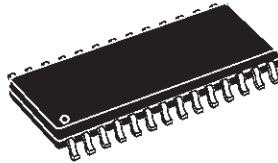
C3 = Sign

For example Bass at -10dB is obtained by the following 8 bit string:

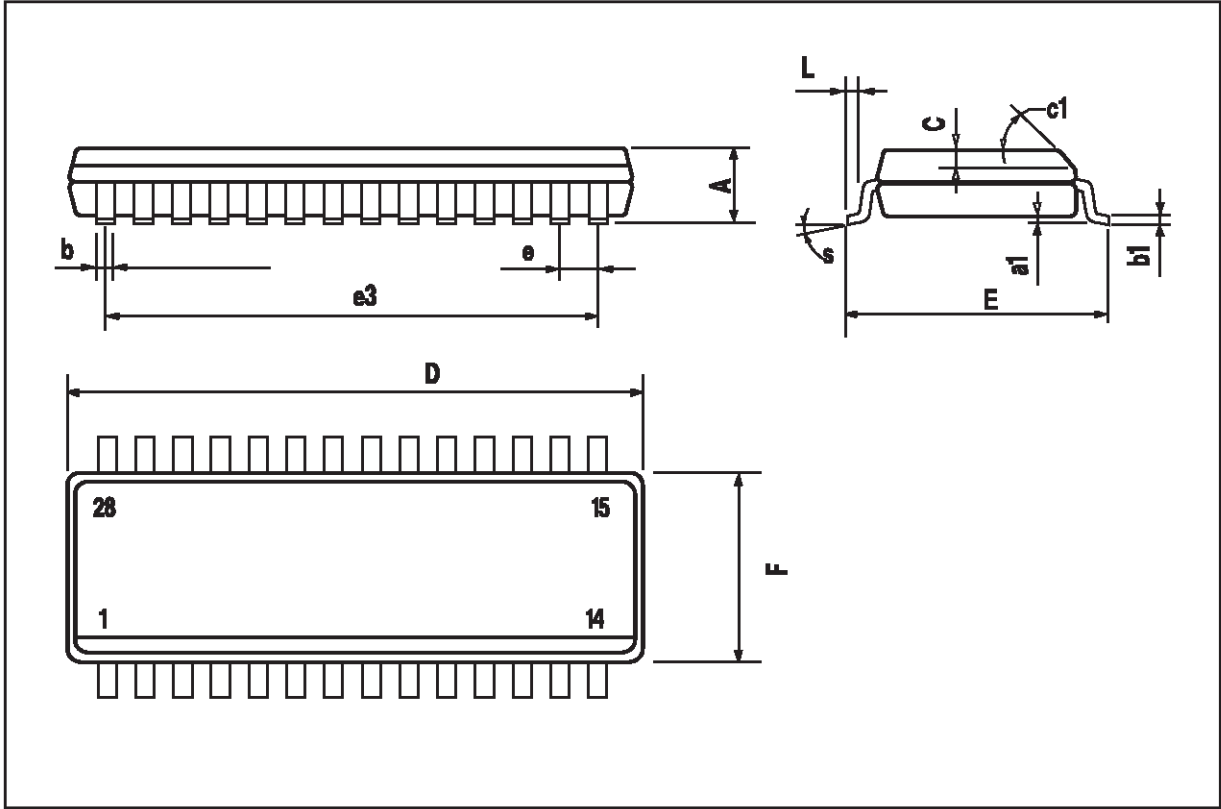
0 1 1 0 0 0 1 0

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

**OUTLINE AND
MECHANICAL DATA**

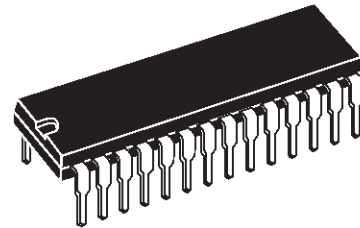


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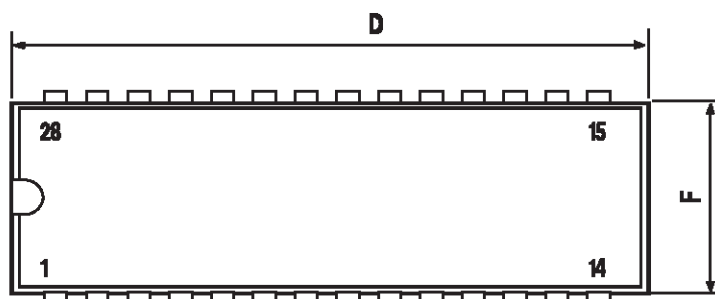
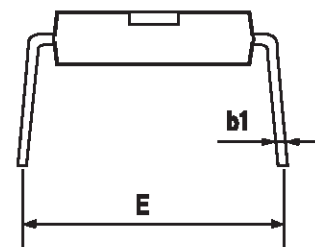
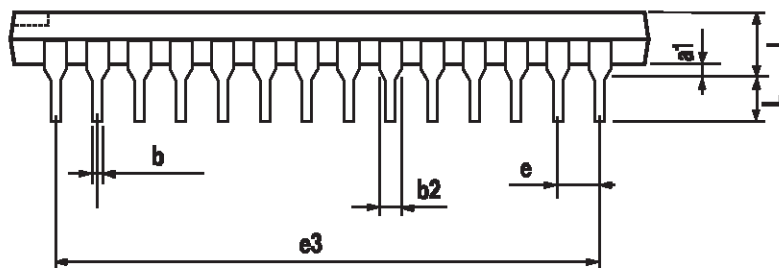


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

OUTLINE AND MECHANICAL DATA



DIP28



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