SW6106 Register List

1. History

V1.0: initial version for IC version 6;

2. Register

Note: reserved bits should not be modified

2.1. REG 0x01: BG Control

Bit	Description	R/W	Default
7:6	i2c register operation enable 0: register operation disable 1: first operation for register enable 2: second operation for register enable 3: nothing Other bits of this register can be writen after first operation and second operation.	W/R	0x0
5-4	reserved	R	0x0
3	PD PDO settings 0: configured according to power configure 1: configured according to mcu	R/W	0x0
2	BG force close 0: nothing 1:BG force close	W/R	0x0
1	BG force open 0: nothing 1: BG force open	W/R	0x0
0	reserved	/	/

2.2. REG 0x03: Key Event Ctrl

Bit	Description	R/W	Default

7:5	/	/	/
4	output power off event 0: nothing 1: output power off This function is valid when Reg0x49[3] is '1' This bit is automatically cleared by hardware	W/R	0x0
3-1	/	/	/
0	short key event 0: nothing 1: short key event This bit is automatically cleared by hardware	W/R	0x0

2.3. **REG 0x05: IRQ Pending1**

Bit	Description	R/W	Default
7	vbusC overvoltage pending bit 0: no irq 1: irq pending This bit is cleared by writing 1 Pending bit will be set to '1' when irq enable and vbusC overvoltage event happed	W/R	0x0
6	*vbusB overvoltage* pending bit 0: no irq 1: irq pending Note: this bit is cleared by writing 1 after vbusB exiting overvoltage	W/R	0x0
5	charger overtime pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
4	UVLO pending bit 0: no irq 1: irq pending Note: this bit is cleared by writing 1 after exiting UVLO	W/R	0x0
3	NTC over temperature pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
2	/	/	/
1	OTP (IC over temperature protect) pending bit 0: no irq 1: irq pending	W/R	0x0

	this bit is cleared by writing 1		
0	SCP/OLP pending bit 0: no irq 1: irq pending Note: this bit is cleared by writing 1 after exiting SCP/OLP	W/R	0x0

2.4. REG 0x06: IRQ Pending2

Bit	Description	R/W	Default
7	short key pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
6	port C plug out pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
5	port C plug in pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
4	port B plug out pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
3	Port B plug in pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
2	port A plug out pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
1	port A plug in pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
0	vbat overvoltage pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0

2.5. **REG 0x07: IRQ Pending3**

Bit	Description	R/W	Default
7	/	/	/
6	fuel gauge Below 5% pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
5	charger *close* pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
4	charger open pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
3	boost close pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
2	boost open pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
1	gauge percent change pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0
0	fast charge status change pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0

2.6. **REG 0x08: IRQ Pending4**

Bit	Description	R/W	Default
7:2	/	/	/
1	wled on/off pending bit 0: no irq	W/R	0x0

	1: irq pending this bit is cleared by writing 1		
0	charger full event pending bit 0: no irq 1: irq pending this bit is cleared by writing 1	W/R	0x0

2.7. REG 0x09: IRQ Enable

Bit	Description	R/W	Default
7:4	/	/	/
3	Reg0x07[1] /Reg0x07[6]/Reg0x8[1:0] irq enable 0: disable 1: enable	W/R	0x0
2	Reg0x07[0] /Reg0x07[5:2] irq enable 0: disable 1: enable	W/R	0x0
1	Reg0x06[7:1] irq enable 0: disable 1: enable	W/R	0x1
0	Reg0x05[7:0] /Reg0x06[0] irq enable 0: disable 1: enable	W/R	0x0

2.8. REG 0x0A: IRQ Maskbits1

Bit	Description	R/W	Default
7	vbusC overvoltage irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
6	vbusB overvoltage irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
5	charger overtime irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0

4	UVLO irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
3	NTC overtempt irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
2	/	/	/
1	OTP irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
0	SCP/OLP irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0

2.9. **REG 0x0B: IRQ Maskbits2**

Bit	Description	R/W	Default
7	short key irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x1
6	port C plug out irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
5	Port C plug in irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
4	port B plug out irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
3	port B plug in irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0

2	port A plug out irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
1	port A plug in irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0
0	vbat overvoltage irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low;	W/R	0x0

2.10. REG 0x0C: IRQ Maskbits3

Bit	Description	R/W	Default
7	/	/	/
6	fuel gauge below 5% irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0
5	charger close irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0
4	charge open irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0
3	boost close irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0
2	boost open irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0
1	gauge percent change irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0

0	fast charge status change irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0

2.11. REG 0x0D: IRQ Maskbits4

Bit	Description	R/W	Default
7:2	/	/	/
1	wled on/off irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0
0	charge full event irq mask bit 0: disable 1: enable Only when mask bit is 1 and irq pengding is 1, irq pin will be low	W/R	0x0

2.12. REG 0x10: Protocol Indication

Bit	Description	R/W	Default
7:6	/	/	/
5:4	sink protocols indication (SW6106 as sink) 1: PD 2: high voltage input/ FCP /AFC, refer to reg0x5F[7:5] 3: reserved	R	0x0
3	/	/	/
2:0	source protocols indication 0: nothing 1: PD 2: QC2.0 3: QC3.0 4: FCP 5: PE2.0/1.1 6: SFCP 7: AFC	R	0x0

2.13. REG 0x11: System Status

Bit	Description	R/W	Default
7:6	/	/	/
5	boost status 0: boost close 1: boost open	R	0x0
4	charger status 0: charger close 1: charger open	R	0x0
3	/	/	/
2	port C status 0: port C off 1: port C on	R	0x0
1	port B status 0: port B off 1: port B on	R	0x0
0	port A status 0: port A off 1: port A on	R	0x0

2.14. REG 0x13: Boost DAC Data

Bit	Description	R/W	Default
7	ADC data type 0: filtered data 1: raw data; note: only Vbat/Ichg/Idischg/Ts can select fiter data and raw data	W/R	0x0
6-0	boost output voltage value V_{Boost} = (5.0 + 0.1*Reg0x13[6:0]) V	R	0x0

2.15. REG 0x14: ADC Vbat Data

Bit	Description	R/W	Default
7-0	battery voltage Vbat[7:0] V_{BAT} = ((Reg0x15[3:0]<<8)+ Reg0x14[7:0]) *1.2 mV	R	0x0

2.16. REG 0x15: ADC Vbat/Vout Data

Bit	Description	R/W	Default
7-4	Vout voltage Vout[11:8] Vout= ((Reg0x15[7:4]<<8)+ Reg0x16[7:0]) *4 mV	R	0x0
3-0	battery voltage Vbat[11:8] V_{BAT} = ((Reg0x15[3:0]<<8)+ Reg0x14[7:0]) *1.2 mV	R	0x0

2.17. REG 0x16: ADC Vout Data

Bit	Description	R/W	Default
7-0	output voltage Vout[7:0] Vout = ((Reg0x15[7:4]<<8)+ Reg0x16[7:0]) *4 mV	R	0x0

2.18. REG 0x17: ADC Ichg Data

Bit	Description	R/W	Default
7-0	Charge current Icharge[7:0] I_{Charge} = ((Reg0x18[3:0]<<8)+ Reg0x17[7:0])*25/7 mA	R	0x0

2.19. REG 0x18: ADC Ichg/Idischg Data

Bit	Description	R/W	Default
7-4	Discharge current Idischarge[11:8] $I_{Discharge}$ = ((Reg0x18[7:4]<<8)+ Reg0x19[7:0])*25/7 mA	R	0x0
3-0	Charge current Icharge[11:8] I_{Charge} = ((Reg0x18[3:0]<<8)+ Reg0x17[7:0])*25/7 mA	R	0x0

2.20. REG 0x19: ADC Idischg Data

Bit	Description	R/W	Default
7-0	Discharge current Idischarge[7:0] $I_{Discharge}$ = ((Reg0x18[7:4]<<8)+ Reg0x19[7:0])*25/7 mA	R	0x0

2.21. REG 0x1A: ADC Die Temp Data

Bit	Description	R/W	Default
7-0	IC internal temperature Tdie[7:0] T_{Die}= ((Reg0x1B[3:0]<<8)+ Reg0x1A[7:0] - 1851)*1/6.82 ℃	R	0x0

2.22. REG 0x1B: ADC IC Temperature/NTC Data

Bit	Description	R/W	Default
7-4	NTC resistor voltage Vntc[11:8,] V_{NTC} = ((Reg0x1B[7:4]<<8)+ Reg0x1C[7:0])*1.1mV; Note NTC resistance is computed according to adc_NTC voltage and current. the current value is 80uA.	R	0x0
3-0	IC internal temperature Tdie[11:8] T_{Die}= ((Reg0x1B[3:0]<<8)+ Reg0x1A[7:0] - 1851)*1/6.82 ℃	R	0x0

2.23. REG 0x1C: ADC NTC Data

Bit	Description	R/W	Default
7-0	NTC resistor voltage Vntc[7:0] V_{NTC} = ((Reg0x1B[7:4]<<8)+ Reg0x1C[7:0])*1.1mV	R	0x0

2.24. REG 0x22: Control Power

Bit	Description	R/W	Default
7:6	control power operation bit 0: control disenable 1: first operation for control enable 2: second operation for control enable 3: nothing Other bits of this register can be writen after first operation and second operation.	/	/
5	Force open boost 0: nothing 1: force open boost Writing “1” to this bit will force open boost when BG force open(reg0x01[1])	R/W	0x0
4	Force close boost 0: nothing 1: force close boost	R/W	0x0
3:2	/	/	/
1	force open charger 0: nothing 1: force open charger	R/W	0x0
0	force close charger 0: nothing 1: force close charger	R/W	0x0

2.25. REG 0x23: PDO Config 1

Bit	Description	R/W	Default
7	/	/	/
6:5	in mcu configure mode(reg0x01[3]=1), 9V PDO current setting , Imax_9v[1:0] Vbus = 9V， I_{max} =((reg0x32[7:5]<<2)+reg0x23[6:5]) *0.1 A		
4-0	in mcu configure mode(reg0x01[3]=1), 5V PDO current setting , Imax_5v[4:0] Vbus = 5V， I_{max} = reg0x23[4:0]*0.1 A; Note, only setting 2A or 3A	R/W	0x0

2.26. REG 0x24: Fast Charge Config1

Bit	Description	R/W	Default
7	Port A source fast charge 0: disable	R/W	OTP

	1: enable		
6	Port C source fast charge 0: disable 1: enable	R/W	OTP
5:4	reserved	R/W	OTP
3	PD enable 0: disable 1: enable Note: PD source is enable only when reg0x24[3] and reg0x5D[0] are 1; reg0x5D[0] default is 1. PD sink is enable only when reg0x24[3] and reg0x5F[1] are 1;reg0x5F[1] default is 1.	R/W	OTP
2	PE source enable 0: disable 1: enable	R/W	OTP
1	FCP source enable 0: disable 1: enable Note: FCP sink enable is reg0x5E[7];	R/W	OTP
0	SFCP enable 0: disable 1: enable	R/W	OTP

2.27. REG 0x25: Fast Charge Config2

Bit	Description	R/W	Default
7-4	/	/	/
3	QC Source enable 0: disable 1: enable	R/W	OTP
2:0	reserved	R	OTP

2.28. REG 0x26: Version Info

Bit	Description	R/W	Default
7-3		/	/
2-0	IC version	R	0x6

2.29. REG 0x32: PDO Config2

Bit	Description	R/W	Default
7-5	in mcu configure mode(Regx01[3]=1), 9V PDO current setting , Imax_9v[4:2] Vbus = 9V， I_{max} = ((Reg0x32[7:5] << 2) + Reg0x23[6:5]) *0.1 A	R/W	0x0
4-0	in mcu configure mode(Reg0x01[3]=1), 12V PDO current setting , Imax_12v[4:0] Vbus = 12V， I_{max} = Reg0x32[4:0] *0.1 A	R/W	0x0

2.30. REG 0x37: Typec Indication

Bit	Description	R/W	Default
7-4	reserved	R/W	OTP
3-2	port C power role indication 1: Sink 2: Source 0/3: no attach	R	0x0
1-0	port C sink power level indication 0: default power 1.5A 2: 3.0A 3: reserved	R	0x0

2.31. REG 0x38: Plug Out Config

Bit	Description	R/W	Default
7-4	/	/	/
3-1	port A unloading detect current threshold (assuming power path MOS resistance is 30mohm) when VOUT<7.65V or VOUT>7.65V and reg0x38[0] = 0 000: 60mA 001: 10mA 010: 20mA 011: 40mA 100: 80mA 101: 6.66mA other: reserved when VOUT>7.65V and Regox38[0] = 1 000: 40mA 001: 10mA	R/W	OTP

	010: 10mA 011: 20mA 100: 40mA 101: 6.66mA other: reserved		
0	port A unloading detect current threshold change when vout > 7.65v 0: disable 1: enable	R/W	OTP

2.32. REG 0x3A: Charger Config1

Bit	Description	R/W	Default
7-6	battery charge current setting when high voltage input 0: 3.5A 1: 3.7A 2: 4.0A 3: 4.2A	R/W	OTP
5-3	battery charge current setting when 5V input 0: 0.5A 1: 1.0A 2: 1.5A 3: 2.0A 4: 2.5A 5: 3.0A 6: 3.2A 7: 3.5A	R/W	OTP
2-0	charger temperature loop setting 0: 100℃ 1: 105℃ 2: 110℃ 3: 115℃ 4: 80℃ 5: 85℃ 6: 90℃ 7: 95℃	R/W	OTP

2.33. REG 0x3B: Charger Config2

Bit	Description	R/W	Default

7	charger end current threshold 0: 300mA 1: 200mA	R/W	OTP
6-4	charger 5V input voltage threshold 0: 4.6V 1: 4.7V 2: 4.8V 3: 4.9V 4: 4.2V 5: 4.3V 6: 4.4V 7: 4.5V note: if input voltage lower than threshold, charger will stop.	R/W	OTP
3-2	battery type 0: 4.2V 1: 4.3V 2: 4.35V 3: 4.4V	R	OTP
1-0	reserved	/	/

2.34. REG 0x3C: Charger Config3

Bit	Description	R/W	Default
7-6	/	/	/
5-3	12V input voltage threshold 0: 11.538V 1: 11.650V 2: 11.765V 3: 11.881V 4: 11.215V 5: 11.215V 6: 11.321V 7: 11.429V note: if input voltage lower than threshold, charger will stop.	R/W	OTP
2-0	9V input voltage threshold 0: 8.490V 1: 8.612V 2: 8.738V 3: 8.867V 4: 8.072V 5: 8.182V	R/W	OTP

	6: 8.295V 7: 8.392V note: if input voltage lower than threshold, charger will stop.		

2.35. REG 0x3D: Boost Config

Bit	Description	R/W	Default
7-6	/	/	/
5-4	port A unloading detect time (current of port A lower than threshold) 0: 16s 1: 4s 2: 8s 3: 32s	R/W	OTP
3	cable compensation setting 0: enable 1: disable	W/R	OTP
2-0	boost temperature loop setting 0: 100℃ 1: 105℃ 2: 110℃ 3: 115℃ 4: 80℃ 5: 85℃ 6: 90℃ 7: 95℃	R/W	OTP

2.36. REG 0x3E: PDO Config3

Bit	Description	R/W	Default
7	PDO setting 0: 5V/3A, 9V/2A, 12V/1.5A 1: 5V/2A, 9V/2A, 12/1.5A This bit is valid when Reg0x01[3]=0;	R/W	OTP
6-0	/	/	/

2.37. REG 0x48: RDC Config

Bit	Description	R/W	Default
7	RDC calculation enable 0: disable 1: enable	R/W	OTP
6	RDC calculation status 0: not finish 1: finish	R	0x0
5-0	Resesrved	R/W	OTP

2.38. REG 0x49: Gauge Config

Bit	Description	R/W	Default
7	battery ovp enable 0: disable 1: enable	R/W	OTP
6	RDC automatically calculation enable 0: disable 1: enable	R/W	OTP
5	RDC calculation temperature compensation enable 0: disable 1: enable	R/W	OTP
4	reserved	R/W	0x 0
3	key control output power off enable 0: disable 1: enable output power off	R/W	OTP
2	charge prior to discharge enable 0: disable 1: enable If this bit is 1, port A and port C(as source) will close when port B or port C(as sink) open.	R/W	OTP
1	fuel gauge reaches 100% condition 1: charge done 0: wait 15 after reach 99%	R/W	OTP
0	AFC source support 12v 0: not support AFC 12v output 1: support AFC 12v output	R/W	OTP

2.39. REG 0x4A: Rdc Value by Compensation

Bit	Description	R/W	Default
7-0	RDC_comp[7:0] value including temperature compensation and ocv voltage compensation R_{DC_Comp} = ((Reg0x4C[5:3]<<8) + Reg0x4A[7:0])*0.336 mΩ	R	0x00

2.40. REG 0x4B: RDC Value Precompensation

Default: 0x9FH

Bit	Description	R/W	Default
7-0	RDC_org[7:0] R_{DC_Orig} = ((Reg0x4C[2:0]<<8) + Reg0x4B[7:0])*0.336 mΩ Note : this register can be written only when BG is opened	R/W	0x9F

2.41. REG 0x4C: RDC Value Compensation Hibit

Bit	Description	R/W	Default
7-6	/	/	/
5-3	RDC_comp[10:8] R_{DC_Comp} = ((Reg0x4C[5:3]<<8) + Reg0x4A[7:0])*0.336 mΩ	R	0x00
2-0	RDC_org[10:8] R_{DC_Orig} = ((Reg0x4C[2:0]<<8) + Reg0x4B[7:0])*0.336 mΩ Note : this register can be written only when BG is opened	R/W	0x00

2.42. REG 0x4D: OCV Current Percent

Bit	Description	R/W	Default
/	/	/	/
6-0	OCV current percent 1%/step	R	0x0

2.43. REG 0x4E: OCV Useful Percent

Bit	Description	R/W	Default
7	/	/	/

6-0	OCV useful percent 1%/step.	R	0x0

2.44. REG 0x4F: Final Percent

Bit	Description	R/W	Default
7	/	/	/
6-0	final percent 1%/step.	R	0x0

2.45. REG 0x50: LED Percent Config1

Bit	Description	R/W	Default
7-6	/	/	/
5-3	charger LED2 percent offset[2:0] 0: 0% 1: 3% 2: 6% 3: 9% 4: -3% 5: -6% 6: -9% 7: -12%	R/W	OTP
2-0	charger LED1 percent offset[2:0] 0: 0% 1: 3% 2: 6% 3: 9% 4: -3% 5: -6% 6: -9% 7: -12%	R/W	OTP

Note : LED default level refer to Appendix 1

2.46. REG 0x51: LED Percent Config2

Bit	Description	R/W	Default
7-6	/	/	/

5-3	charger LED4 percent offset[2:0] 0: 0% 1: 3% 2: 6% 3: 9% 4: -3% 5: -6% 6: -9% 7: -12%	R/W	OTP
2-0	charger LED3 percent offset[2:0] 0: 0% 1: 3% 2: 6% 3: 9% 4: -3% 5: -6% 6: -9% 7: -12%	R/W	OTP

2.47. REG 0x52: LED Percent Config3

Bit	Description	R/W	Default
7-6	/	/	/
5-3	boost LED2 percent offset[2:0] 0: 0% 1: 3% 2: 6% 3: 9% 4: -3% 5: -6% 6: -9% 7: -12%	R/W	OTP
2-0	boost LED1 percent offset[2:0] 0: 0% 1: 3% 2: 6% 3: 9% 4: -3% 5: -6% 6: -9% 7: -12%	R/W	OTP

2.48. REG 0x53: LED Percent Config4

Bit	Description	R/W	Default
7-6	/	/	/
5-3	boost LED4 percent offset[2:0] 0: 0% 1: 3% 2: 6% 3: 9% 4: -3% 5: -6% 6: -9% 7: -12%	R/W	OTP
2-0	boost LED3 percent offset[2:0] 0: 0% 1: 3% 2: 6% 3: 9% 4: -3% 5: -6% 6: -9% 7: -12%	R/W	OTP

2.49. REG 0x5D: Fast Charge Config3

Bit	Description	R/W	Default
7-1	/	/	/
0	PD src enable 0: disable 1: enable PD source is enable only when reg0x24[3] and reg0x5D[0] are 1	R/W	OTP

2.50. REG 0x5E: Fast Charge Config4

Bit	Description	R/W	Default
7	FCP sink enable 0: disable 1: enable	R/W	OTP

6	AFC sink enable 0: disable 1: enable	R/W	OTP
5	AFC source enable 0: disable 1: enable	R/W	OTP
4-2	reserved	R/W	OTP
1	Port C support unloading detect 0: not support 1: support	R/W	OTP
0	WLED pin function setting 0: mapping to Lightnning port Data pin 1: WLED mode	R/W	OTP

2.51. REG 0x5F: Fast Charge Config5

Bit	Description	R/W	Default
7	high voltage sink indication 0: nothing 1: input protocol is high voltage protocol	R	/
6	FCP sink indication 0: nothing 1: input protocol is FCP protocol	R	/
5	AFC sink indication 0: nothing 1: input protocol is AFC protocol	R	/
4	FCP source indication 0: nothing 1: output protocol is FCP protocol	R	/
3	AFC source indication 0: nothing 1: output protocol is AFC protocol	R	/
2	reserved	R/W	OTP
1	PD sink enable 0: disable 1: enable	R/W	OTP
0	Led display threshold configuration at 9V/12V input/output 0: same with 5v 1: differtent with 5v	R/W	OTP

2.52. REG 0x60~0x6F: OCV curve

Appendix 1. Led default level

Discharge:	3 LED	4 LED	5 LED
D_P1	30%	20%	16%
D_P2	63%	48%	38%
D_P3	/	73%	57%
D_P4	/	/	78%

Charge:	3 LED	4 LED	5 LED
C_P1	45%	35%	29%
C_P2	84%	64%	53%
C_P3	/	92%	76%
C_P4	/	/	95%