Digital Logic Design

Final Project

Due Date:

1- Implement the Boolean function below using transistor-level Verilog coding.

$$f(A,B,C,D) = AD + AB'C + BD' + A'C'D'$$

In your testbench, test the module for all different combinations of inputs. (80 points)

2- Implement an 4-bit signed adder using gate-level Verilog coding. The adder should have an overflow detector.
In your testbench, test it for different inputs (once with two positive numbers without overflow, once with two positive numbers with overflow, once with two negative numbers without overflow, and once with two negative numbers with overflow). (80 points)

3- Implement an ALU with two 6 bit signed inputs A and B and with 4 different operation modes mentioned below using dataflow coding.

0- $(A \lll 2) + (B \ggg 1)$
1- $A + 3B$
2- $-B$
3- $|2A - B|$

(Note: "<<<" and ">>>" mean arithmetic shift to left and arithmetic shift to right, respectively.) (140 extra points)

Good Luck!
Mosayebi
Do not hesitate to ask your question
Via eeXBee@gmail.com

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Note 1: For each of your codes you should provide two Verilog files: one for the module, and one for the testbench. There should be enough test cases in your testbenches to test the modules for different input values.

Note 2: This project should be done by each student individually; thus, in case of any similarities between the codes provided by the students, all of those with similarities in codes will receive a 0 for their projects.

Note 3: Upload your codes as one zip file.

Note 4: Please name your files as below:

For the modules:

Your_Last_Name.Your_First_Name.Student_Number.Problem_Number.Module.v

Example: Cruise.Tom.96777777.Problem1.Module.v

For the testbenches:

Your_Last_Name.Your_First_Name.Student_Number.Problem_Number.Testbench.v

Example: Cruise.Tom.95777777.Problem1.Testbench.v

Good Luck!

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