

RS 485 PCI

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RS 485 PCI: Interface card

RS 485 Interface extension card for personal computers

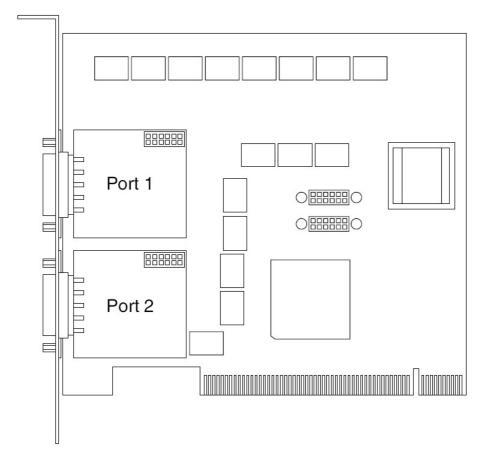


Figure 1: Side view

Weight

The card contains two independent RS 485 interfaces as an extension for a PC (PADT). The interfaces are electrically isolated (also among themselves) and suitable to connect HIBUS-2 directly to programmer units and visualization stations.

approx. 110 g

Baud rate 9.6 to 57.6 kBaud Data format any Basis addresses automatic configuration automatic configuration Interrupts Isolation (electric isolation) > 1 kV Connections 2 Sub-D plugs 9-pole Operating data 5 V / 0.2 A **Dimensions** 120 x 106 mm



After installation of the following HIMA programs the FIFO for the corresponding interface must be deactivated in the device manager of the windows operating system (communication ports):

- ELOP II
- OPC A&E
- Axeda Supervisor (Wizcon)

Operation with ELOP II

If short-time disturbances or failures in communication should still occur despite of a deactivated FIFO, the following measures can solve the problems:

from ELOP II Version 4.1: reduce value for message length

Open in the context menu of the resource *Properties* and reduce the value for the message length in the register *PADT (PC)*.

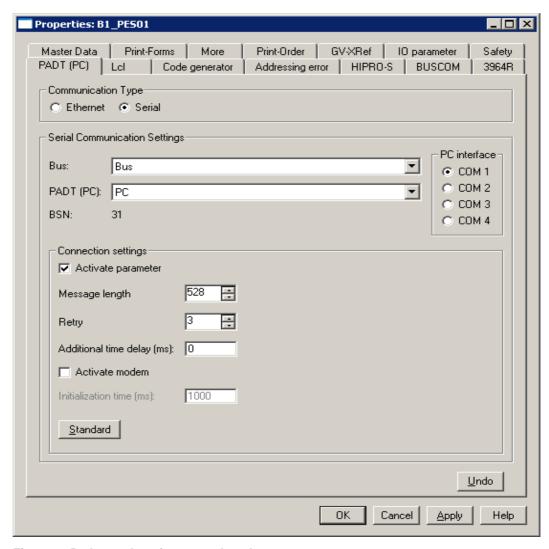


Figure 2: Reduce value of message length

The check box "Activate parameter" must be set that a change of the message length becomes active.

up to ELOP II Version 3.5: Setting the time delay

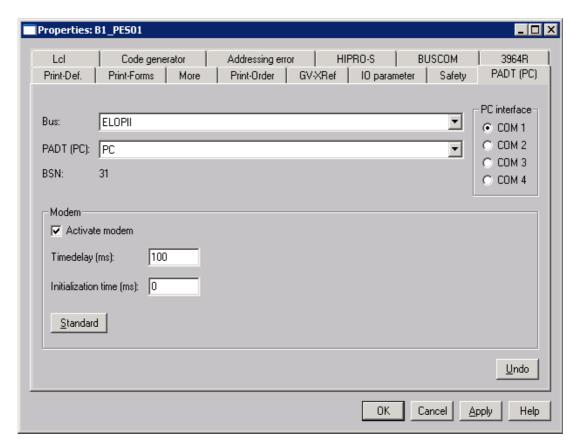


Figure 3: Setting the time delay at modem

The check box "Activate modem" must be set that a change of the time delay becomes active for the communication.

After initialization of the "Modem Connection" after each start from the control panel or at online tests an annunciation results about the initialization of the time.

Bus system with ELOP II and HIPRO data exchange (several masters)

If the bus system is used in common for ELOP II and HIPRO, several bus masters share the communication. If in this case the time delay was activated as described above, the time delays must be set for <u>all</u> masters to the same value. This time delay must be the same as the time delay of the modem otherwise the following error message will appear:

" If the PADT and the PES Master are used together on the same bus the same time delay setting must be used. Please check your time settings."

Therefore in the configuration of the project

- select Properties,
- select the bus and mark it to open the dialog Edit HIBUS,
- select bus station PES master and process it in the dialog HIBUS station. There the time delay is set (example ELOP II up to version 4.1):

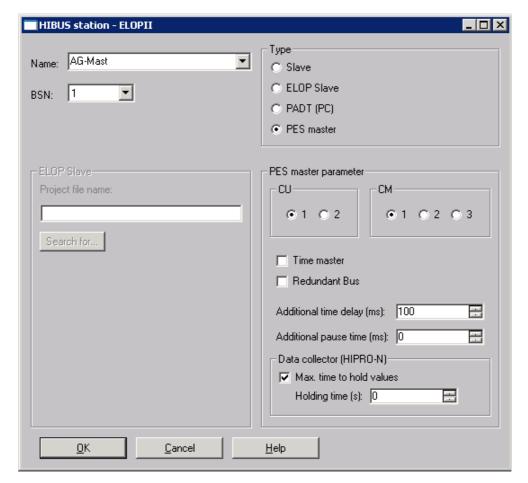


Figure 4: Setting the time delay at PES master

Note

With a loss of the communication connection an increased time delay triggers an increased bus cycle time. The concerning master waits during the defined time delay for an answer and so delays the data exchange.

This performance has to be considered.

Pin	RS 485	Signal	Meaning
1	-	-	not used
2	-	RP	5 V, decoupled by diodes
3	A/A'	RxD/TxD-A	Receive/Transmit Data A
4	-	CNTR-A	Control signal A
5	C/C'	DGND	Data Ground
6	-	VP	5 V, positive pole of power supply
7	-	-	not used
8	B/B'	RxD/TxD-B	Receive/Transmit Data B
9	-	CNTR-B	Control signal B

Table 1: Pin assignment of the interfaces RS 485, 9-pole