HIMA

F 8652E

F 8652E: Central module

Use in the PES H41q-MS, -HS, -HRS,
Safety-related, applicable up to SIL 3 according to IEC 61508

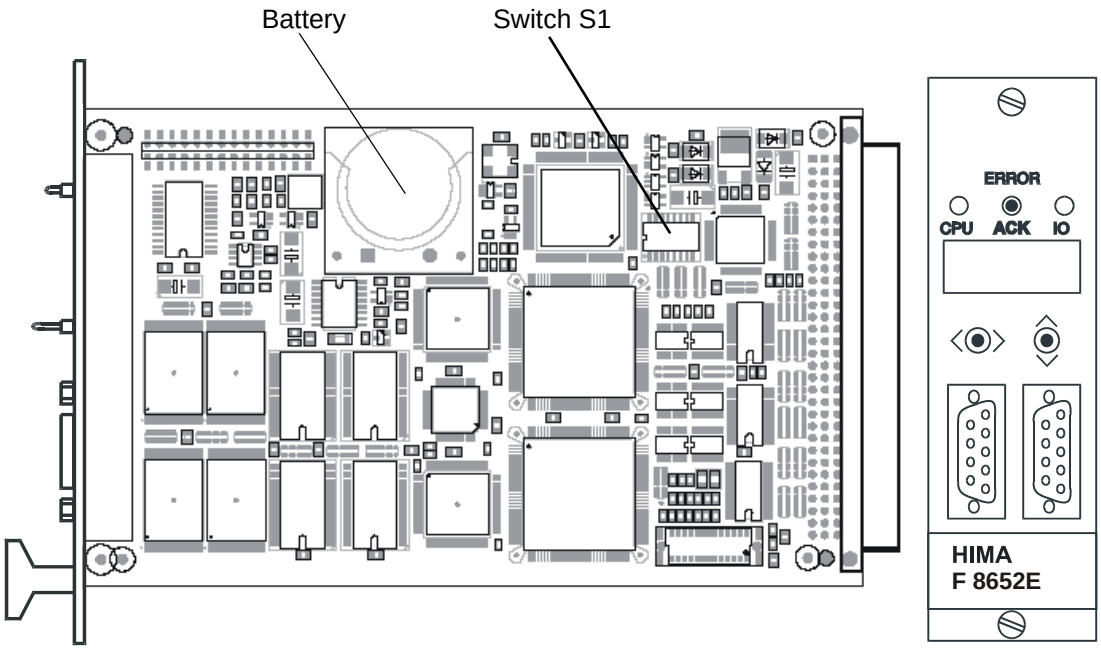
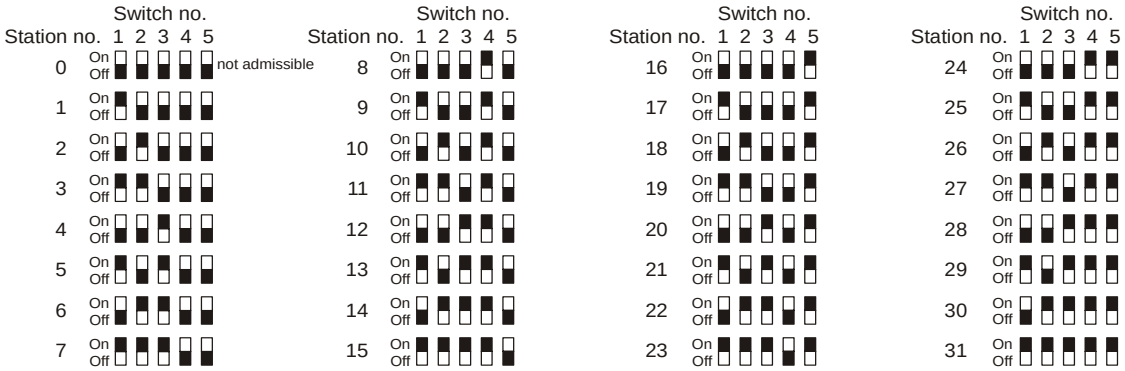


Figure 1: Layout version 02 and front view (Layout version 00 and 01 see figure 3)

Central module with two clock-synchronized microprocessors

Microprocessors	INTEL 386EX, 32 bits
Clock frequency	25 MHz
Memory per microprocessor	
Operating System	Flash-EPROM 1 MB
User program	Flash-EPROM 1 MB *
Data	SRAM 1 MB *
	* Degree of utilization depending on operating system version
Interfaces	Two serial interfaces RS 485 with electric isolation
Diagnostic display	Four digit matrix display with selectable information
Shutdown on fault	Safety-related watchdog with output 24 V, loadable up to 500 mA, short-circuit proof
Construction	Two European standard PCBs, one PCB for the the diagnostic display
Space requirement	8 SU
Operating data	5 V / 2 A

Setting of the bus station no. via switches S1-1/2/3/4/5:



Legend:

Positions white switch:

Bit is set White switch in position OFF	Bit is not set White switch in position ON

Setting of the transmission rate with switch S1-8:

Pin	RS 485	Signal	Meaning
1	-	-	not used
2	-	RP	5 V, decoupled by diodes
3	A/A'	RxD/TxD-A	Receive/Transmit Data A
4	-	CNTR-A	Control signal A
5	C/C'	DGND	Data Ground
6	-	VP	5 V, positive pole of power supply
7	-	-	not used
8	B/B'	RxD/TxD-B	Receive/Transmit Data B
9	-	CNTR-B	Control signal B

Table 1: Pin assignment of the interface RS 485, 9-pole

Before withdrawing a central module its fixing screws must be loosened completely and freely movable. Separate the module from the bus board by pushing the ejection lever (front label) top down and withdraw uninterruptedly the module to prevent faulty signals in the system which can trigger a shutdown!
For insertion set the module onto its connector and then insert it uninterruptedly until to the stop to prevent faulty signals in the system!

Function of the ejection lever with front label

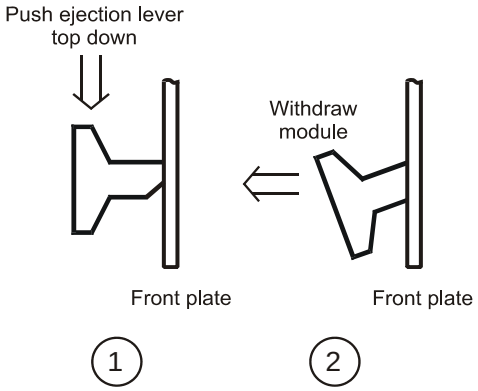


Figure 2: Function of the ejection lever

Diagnostic display of the central module

– Four digit alphanumerical display,
– two LEDs for the general display of errors (CPU for the central modules, IO for the testable input/output modules),
– two toggle switches to request detailed error information,
– push-button ACK resets the error indication;
in failure stop ACK behaves like restarting the system.

For further information on the diagnostic display and lists of error codes, refer to the documentation "Functions of the operational system BS 41q/51q" (also on ELOP II CD).

Notes for start-up and maintenance

– Lifetime of the buffer battery (*without* voltage feeding):
1000 days at T_A = 25 °C
200 days at T_A = 60 °C
– It is recommended to change the buffer battery (CPU in operation) at the latest after 6 years, or with display BATI within three months
(Lithium battery, e. g. type CR 2477N, HIMA part no. 44 0000018)
– Check the bus station no. and transmission rate at switch S1 for correct settings
– **Important:** When upgrading an F 8652 to an F 8652E module the fan concept has also to be changed!

Layout versions 00, 01 and 02
There are no functional differences between the layout versions 00, 01 and 02.

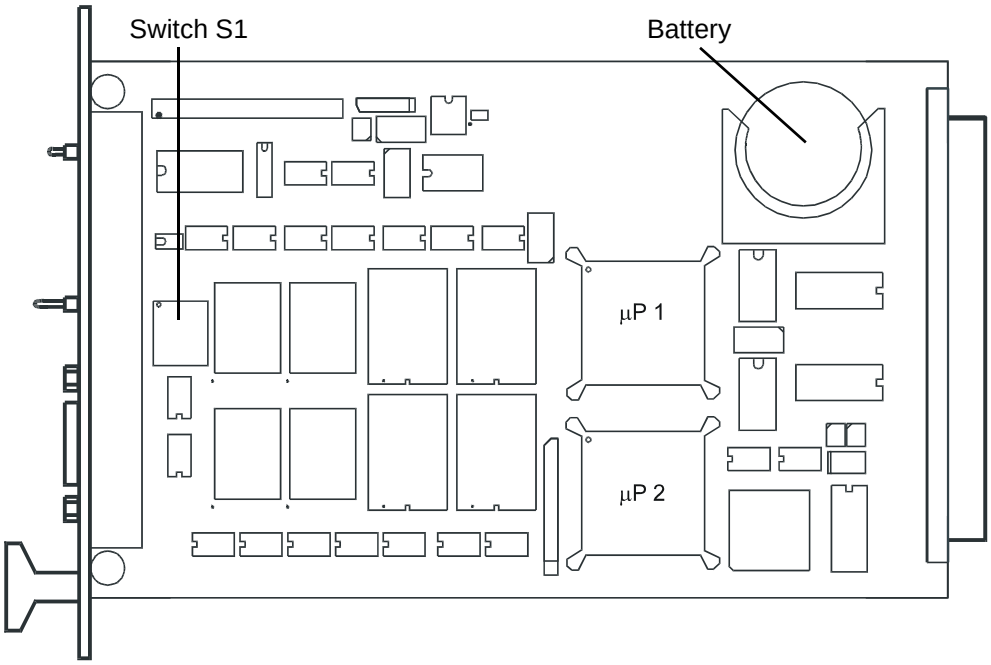


Figure 3: Layout versions 00 and 01