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ℹ This table shows all results in the report. Use the column headers to sort the results in this report. Double-click a result to see detailed metrics. Double-click on demangled names to rename it.

| ID | Estimated Speedup | Function Name | Demangled Name | Duration (8.19768e+07) | Runtime Improvement (4.25839e+07) | Compute Throughput | Memory Throughput | # Registers | Grid Size |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 51.83 | checkSortedRowWi... | checkSortedRowWi... | 0.05 | 0.02 | 5.04 | 8.20 | 16 | 16, 51 |
| 1 | 65.67 | checkSortedColum... | checkSortedColum... | 0.03 | 0.02 | 6.11 | 6.11 | 16 | 16, 51 |
| 2 | 23.28 | sortRowsKernelInt | sortRowsKernelInt.. | 22.63 | 5.27 | 89.48 | 89.48 | 18 | 512, |
| 3 | 35.42 | transposeKernelInt | transposeKernelInt.. | 0.03 | 0.01 | 23.49 | 64.58 | 16 | 16, |
| 4 | 51.56 | checkSortedRowWi... | checkSortedRowWi... | 0.08 | 0.04 | 7.16 | 8.16 | 16 | 16, 51 |
| 5 | 65.57 | checkSortedColum... | checkSortedColum... | 0.03 | 0.02 | 6.12 | 6.12 | 16 | 16, 51 |
| 6 | 28.38 | sortRowsKernelInt | sortRowsKernelInt.. | 22.24 | 6.31 | 91.05 | 91.05 | 18 | 512, |
| 7 | 34.20 | transposeKernelInt | transposeKernelInt.. | 0.03 | 0.01 | 24.39 | 65.80 | 16 | 16, |
| 8 | 87.21 | checkSortedRowWi... | checkSortedRowWi... | 32.42 | 28.28 | 3.12 | 49.85 | 16 | 16, 51 |
| 9 | 58.63 | checkSortedColum... | checkSortedColum... | 4.44 | 2.60 | 22.94 | 41.37 | 16 | 16, 51 |

The following performance optimization opportunities were discovered for this result. Follow the rule links to see more context on the Details page.
Note: *Speedup estimates provide upper bounds for the optimization potential of a kernel assuming its overall algorithmic structure is kept unchanged.*

**Long Scoreboard Stalls**
**Est. Speedup: 35.42%**

On average, each warp of this kernel spends 20.0 cycles being stalled waiting for a scoreboard dependency on a L1TEX (local, global, surface, texture) operation. Find the instruction producing the data being waited upon to identify the culprit. To reduce the number of cycles waiting on L1TEX data accesses verify the memory access patterns are optimal for the target architecture, attempt to increase cache hit rates by increasing data locality (coalescing), or by changing the cache configuration. Consider moving frequently used data to shared memory. This stall type represents about 49.9% of the total average of 40.0 cycles between issuing two instructions.

The following table lists the metrics that are key performance indicators:

| Metric Name | Value | Guidance |
|---|---|---|