

Digital Design Lab

Fall 2024 - Intro

<https://web.cs.hacettepe.edu.tr/~bbm231/>

<https://piazza.com/hacettepe.edu.tr/fall2024/bbm233>

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Student Assistants: M. Mustafa Karataş and İlter Doğaç Dönmez

Any Questions:

Please ask on Piazza publicly

(not via Emails*)

- Only types of questions that require you to share parts of assignment solutions may be asked in private.
- Contribution to answering your classmates' questions may earn you extra credit.

* Emails end up in spam sometimes, so please stick to the Piazza for communication.

Lab Sessions

Tuesdays

Attendance will be taken.

You must attend at least 80% of lab session to pass. You must attend board experiments sessions face-to-face to get a grade!

**Attendance
is
mandatory!**

Section 1



Section 2

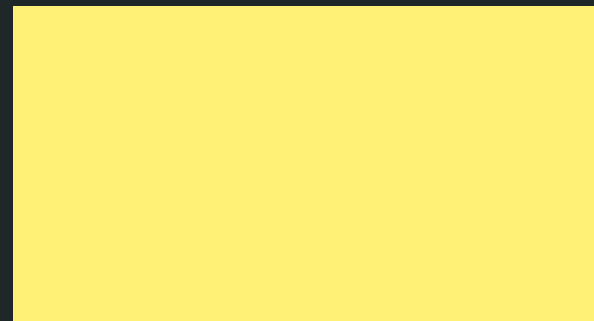


13:40



15:00

15:10



16:30

Lab Plan and Program (Tentative)

Lab session with graded tasks

No Lab Session

Lab session without graded tasks

1) Board Experiments - digital logic design using logic gates and other electronic components (**Digital Systems Lab**).

2) Verilog Assignments - digital logic design using HW description languages and an FPGA simulator (**Comp. Lab**).



Icarus Verilog Icarus Verilog - <http://iverilog.icarus.com/>

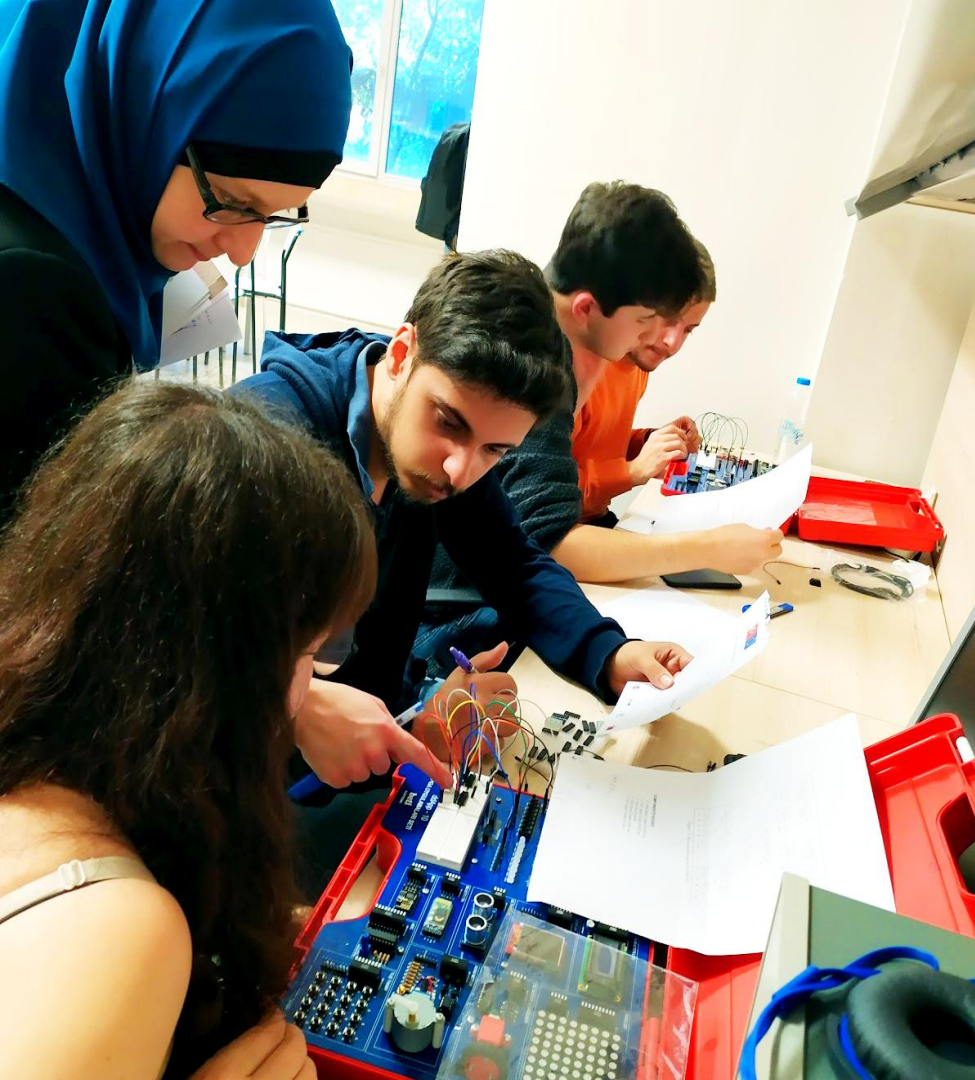


Vivado Design Suite - <https://www.xilinx.com/support/download.html>

Grading policy:

- 3 board experiments 30% (10% each)
- 2 Verilog Quizzes 5%
- 2 Verilog assignments 40% (20% each)
- Final Project (Verilog) 25%

Week	Date	Lab
3	08/10	Introduction, Logistics
4	15/10	Board Experiment 1
5	22/10	Board Experiment 1
6	29/10	Republic Day of Türkiye
7	05/11	Board Experiment 2&3
8	12/11	Board Experiment 2&3
9	19/11	Verilog Combinational Circuits + Quiz 1
10	26/11	Verilog Assignment 1
11	03/12	Verilog Sequential Circuits
12	10/12	Verilog Sequential Circuits + Quiz 2
13	17/12	Verilog Assignment 2
14	24/01	Final Project (Verilog)



A short introduction to board experiments prepared during pandemic:

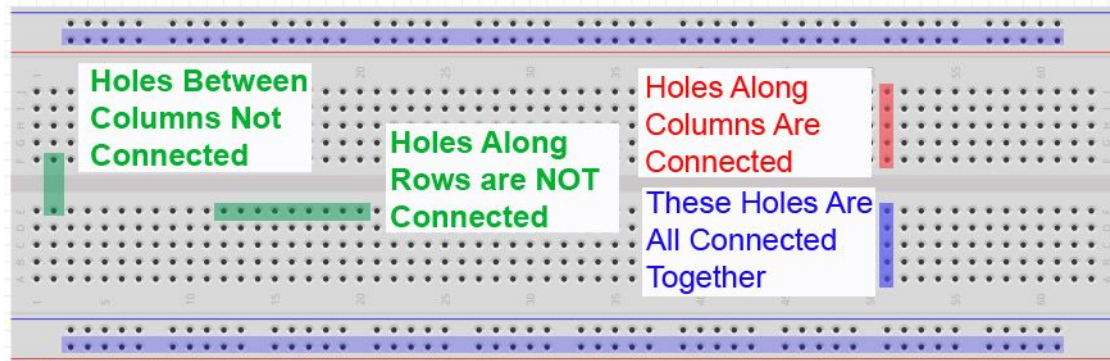
<https://youtu.be/ISpNhScERJY>

Board Experiments - Important Notes

We will implement the circuits on the breadboards. For more info about breadboards and how the experiments will be conducted, watch the following videos before the first graded lab:

- [Introduction to Breadboard \(Protoboard\) Part 1](#)
- [Introduction to Breadboard \(Protoboard\) Part 2](#)
- [How our board experiments will look like \(recorded during pandemics\)](#)
- [Do the practice exercises](#)

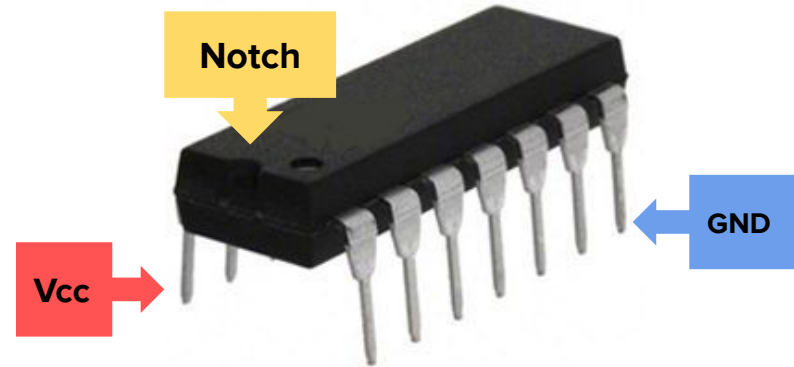
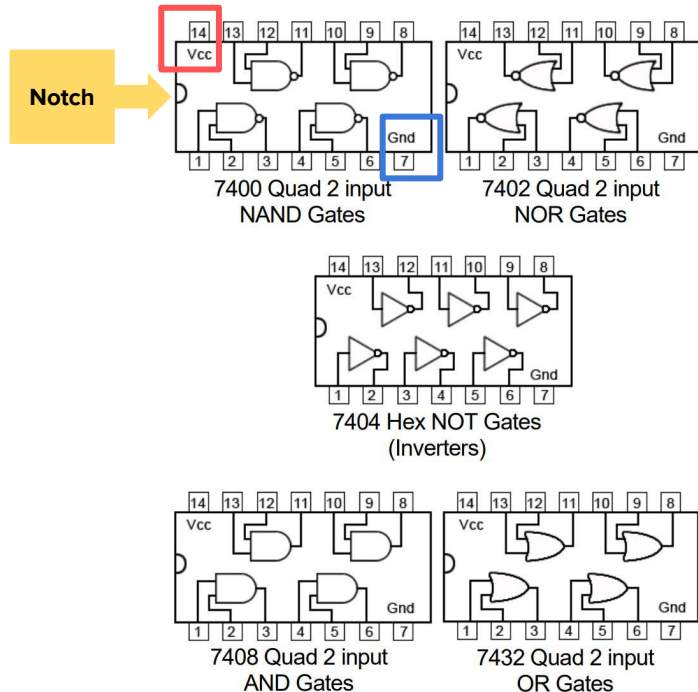
You are responsible for learning this before the first graded lab!



For detailed instructions and a basic example of how to use a breadboard, click [here](#).

7400 Series Quad 2-input gate Integrated Circuits

- Use the given figures as a reference to discern the pin numbers.



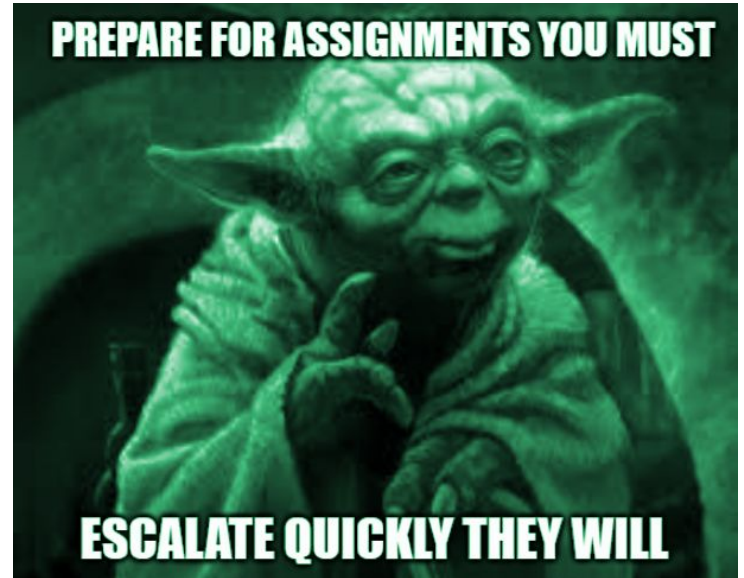
How to prepare for the lab

1. Read the lab instructions

Cannot stress this enough!

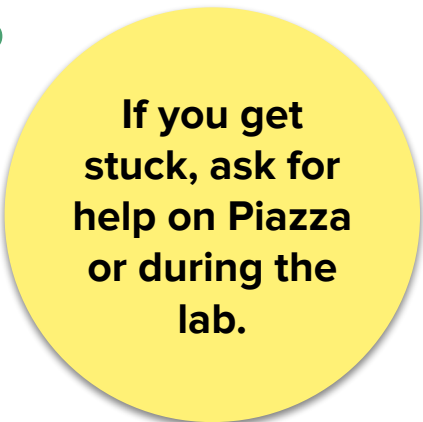
carefully as soon as they are announced (you will be given enough time to prepare).

2. Do a preliminary topic research if instructed, **write a report answering the questions, design circuits as instructed.**



How to prepare for the lab (cont.)

3. Submit the report before the lab. Use your report during the lab session to complete the experiment. Do the experiment on the breadboard:
 - a. **Implement the circuit you designed in your report or the one given by the TAs,**
 - b. **Test for all test cases and verify its correctness!**
4. Show your work to a TA before the end of your lab session. For Verilog assignments, submit before the deadline.



If you get stuck, ask for help on Piazza or during the lab.

How to prepare for the lab (optional practice)

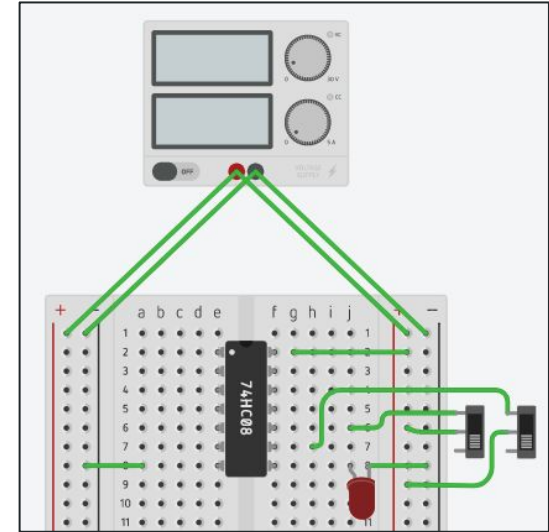
You may get familiar with the breadboard by following this [link](#).

1. Investigate the connections and the layout of the breadboard. Start the simulation and observe the behavior of the **74HC08 AND** gate.
2. Experiment with logic gates. Try to replace the given **AND** gate with **NAND**, **NOR**, **NOT** and **OR** gates.

Practice implementing and draw neat logic circuits for your reports:



<https://circuitverse.org/>



Submissions - What To Turn In

1) Board Experiments

- Preliminary lab reports to be **presented during the lab hour** (hard copy or show electronic version) + board experiment + defense and quiz about the work.
Report submissions via <https://submit.cs.hacettepe.edu.tr/>

- **Groups of two will be formed for board experiments. Teammates must be from the same section.**

2) Verilog Assignments

- Verilog code + report submissions via <https://submit.cs.hacettepe.edu.tr/>


- **Groups will NOT be formed for Verilog assignments. Only individual work will be accepted throughout the semester.**


In case of any changes, please read the assignment instructions carefully!

Grading Platform

<https://test-grader.cs.hacettepe.edu.tr/>



 Calendar

 Given Courses

 Taken Courses

What is TurBograder?

FAQs

Connect

Calendar







Courses 1 - 1 of 1

Normal



Active

Course Name	Code	Year	Semester			
 Digital Design Lab	233	2024	Fall			 View

Add Course

< Previous

Next >

*** You will be able to test your code before submission.**

Involvement on Piazza

(or any other kind of helpful contribution to this course)

May earn you extra credit!



Lab Experiments/ Assignments Grading

Lab grade will include:

- Written report grade
- Assignment implementation grade

Writing a Report (PDF format expected)

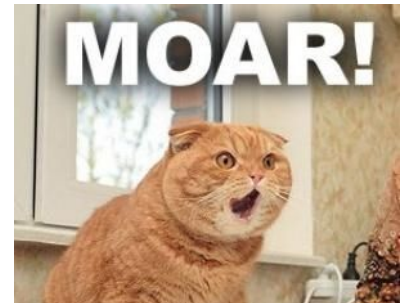
Cover Page: Student name and surname, student ID, name of the Experiment/Assignment, date of submission.

Answer the questions, explain the code, show the experiment steps, note any issues you may have faced.

Brevity, clarity and report structure are important!

We suggest using the LaTeX template we'll provide.

You may use Overleaf online - very convenient.

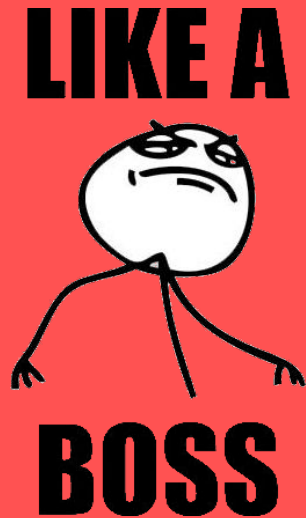


When we see students
who are getting creative

Objectives of this course:

- Learn how to “code” hardware like a boss.
- Have fun

“Learning
anything is **10%**
material and
90% being excited
to learn.”
- Daniel Bourke



Final Verilog Project

Should be something fun if you show us you are motivated by being involved in labs and on Piazza.

Five years ago, students designed an underground road intersection controller for future Martian settlements. :P



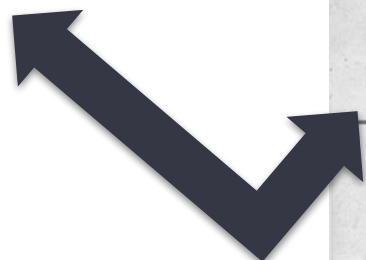
HACETTEPE UNIVERSITY
Computer Engineering Department
BBM233 Logic Design Laboratory
Fall 2019

Martian Underground Road Intersection Controller



Final Verilog Project

Four years ago, students helped an evil AI entity destroy the human race. :P



Verilog Project



ACCESS BY UNAUTHORIZED PERSONNEL IS STRICTLY PROHIBITED
PERPETRATORS WILL BE TRACKED, LOCATED, AND DETAINED



Clearance Level	2
Item #	SCP-079
Object Class	Euclid

Special Containment Procedures:

SCP-079 is packed away in a double-locked room in the secured general holding area at Site-15, connected by a 120VAC power cord to a small array of batteries and solar panels.

Staff with Level 2 or higher clearance may have access to SCP-079. Under no circumstances will SCP-079 be plugged into a phone line, network, or wall outlet. No peripherals or media will be connected or inserted into SCP-079.

Final Verilog Project

Three years ago, students helped design a special machine gun controller chip for the SIGANFU sci-fi battle suit.



<<stay calm, trust the plan.

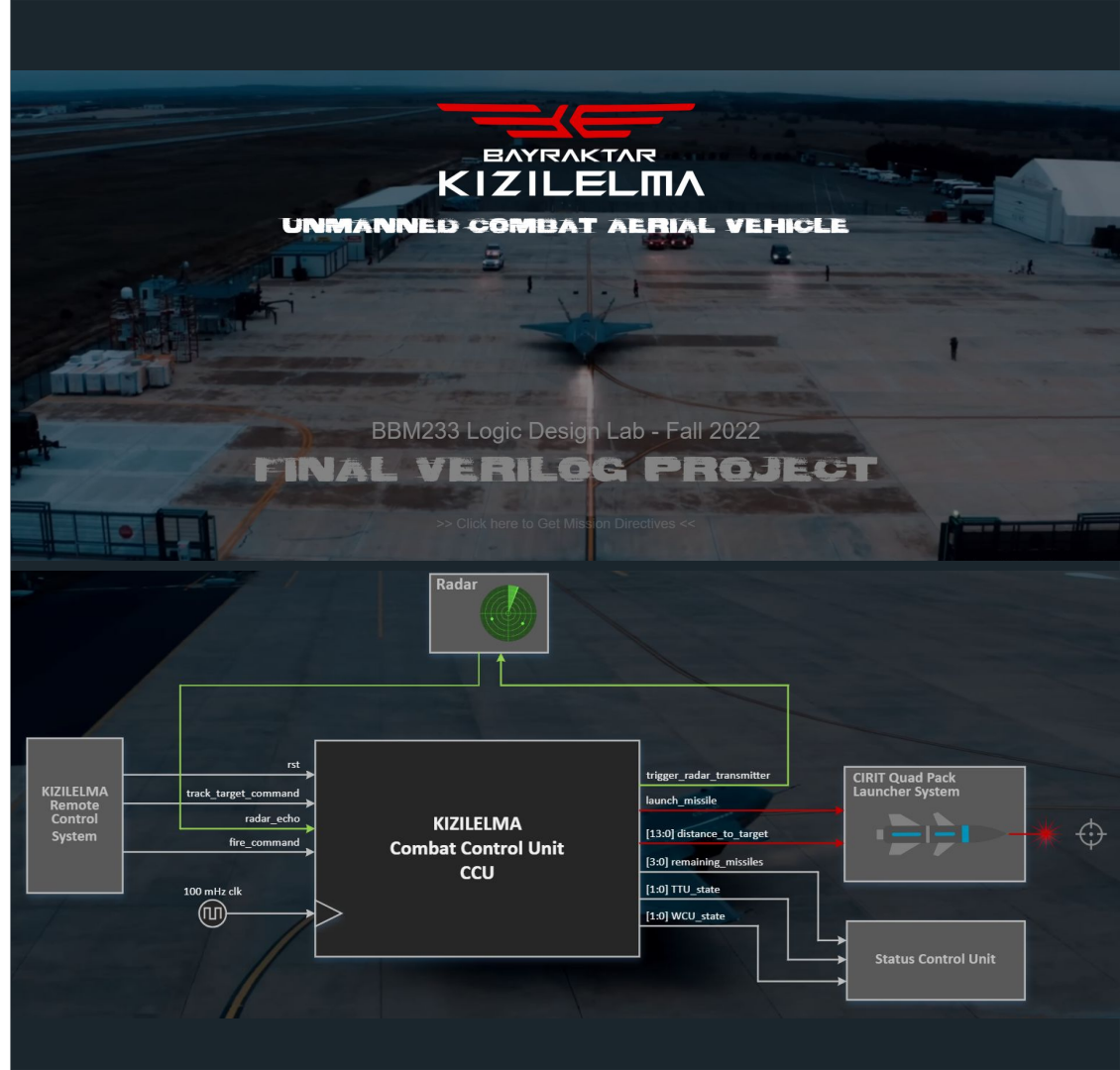
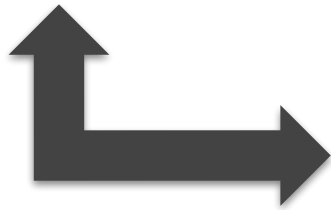
BBM233 Logic Design Lab - Fall 2021

Final Verilog Project

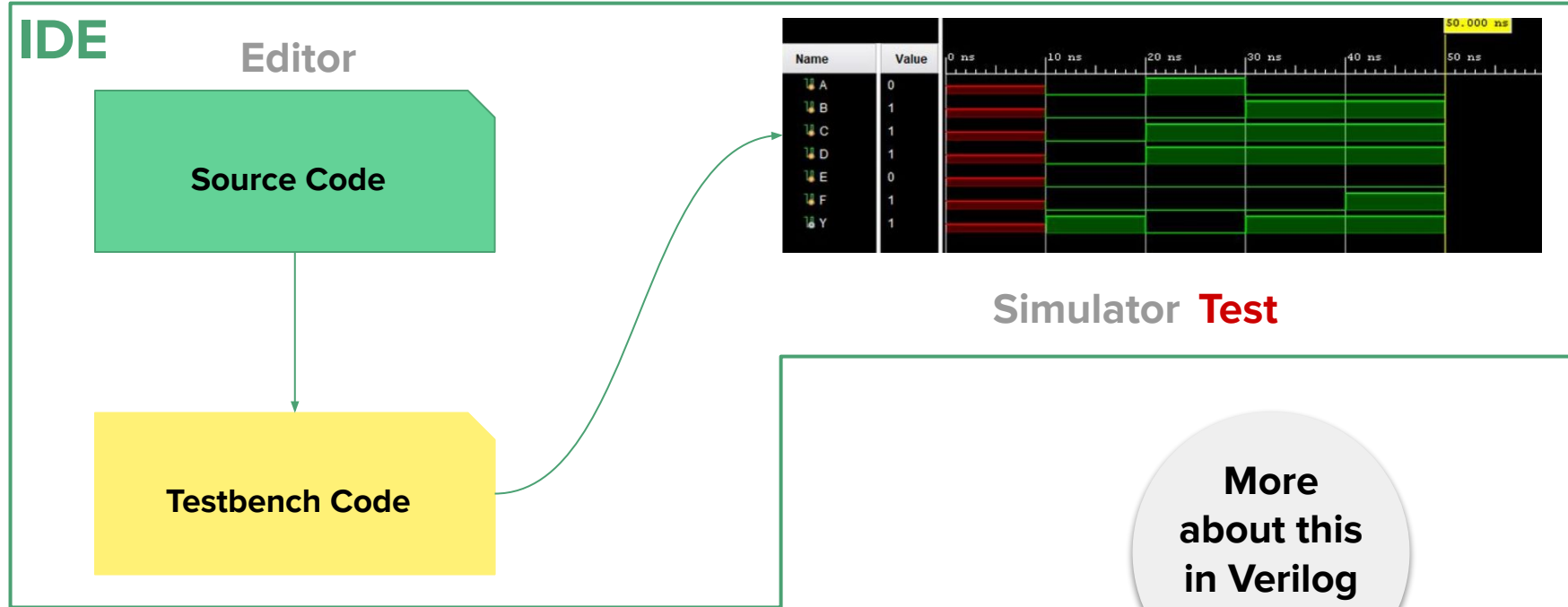
>> [Click here to Get Mission Directives](#) <<

Final Verilog Project

Two years ago, students helped design a Combat Control Unit chip for KIZILELMA Unmanned Combat Aerial Vehicle.



Verilog Designs Development Process



More
about this
in Verilog
Tutorial

Questions?