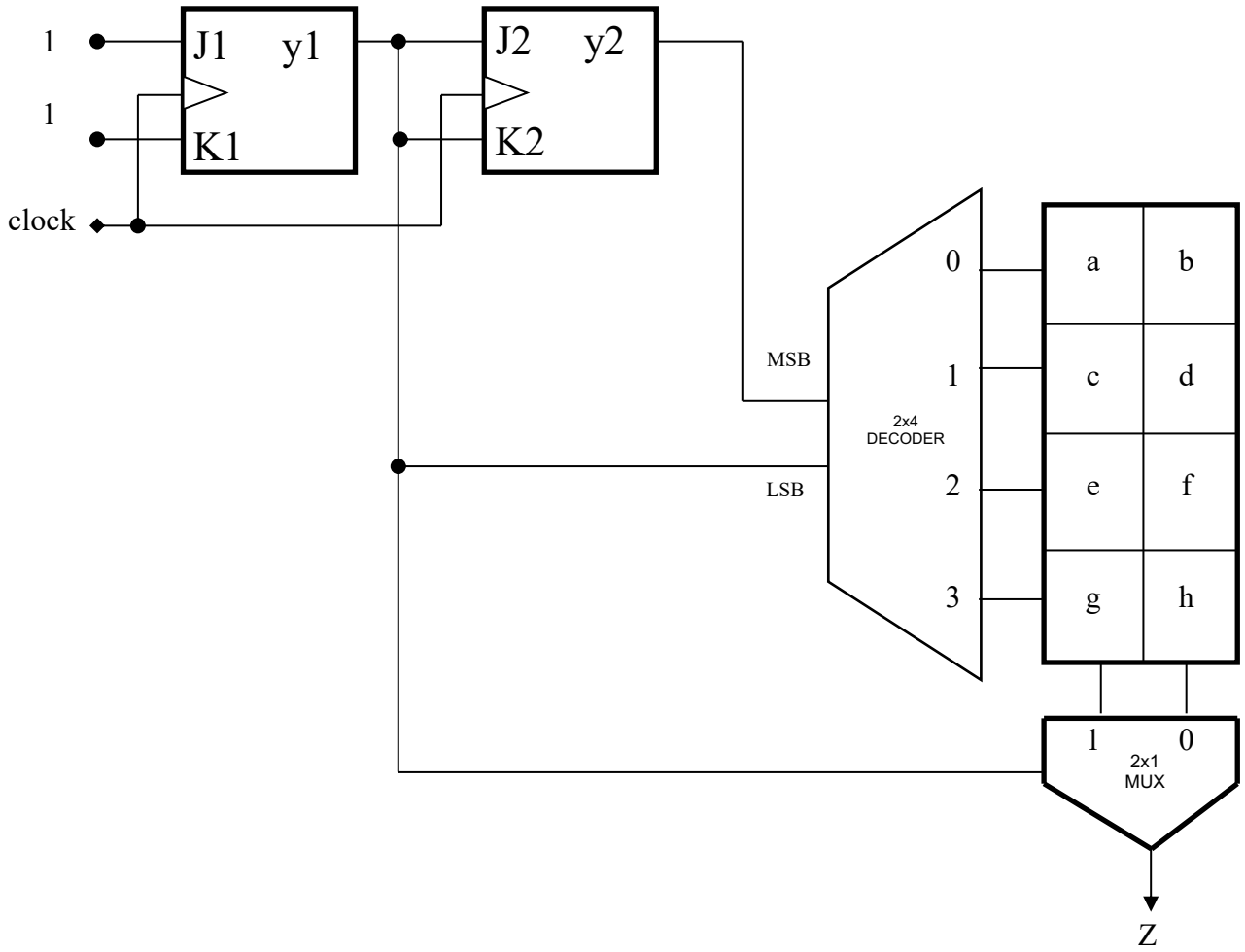
Final Review

Logic Design – BBM231

QUESTION

For the circuit given below, at the beginning the clock signal is at 0 level and y_1=0, y_2=0. MSB: most significant bit. LSB: least significant bit. A rise of the clock signal to 1 level and a subsequent fall back to 0 level together constitute a **pulse**. Fill the rest of the table below for y_1, y_2 (which can be 0 or 1) and Z output (which can be one of the given 8 letters).

	y_1	y_2	Z
At the beginning	0	0	
After the 1st pulse			
After the 2nd pulse			
After the 3rd pulse			
After the 4th pulse			



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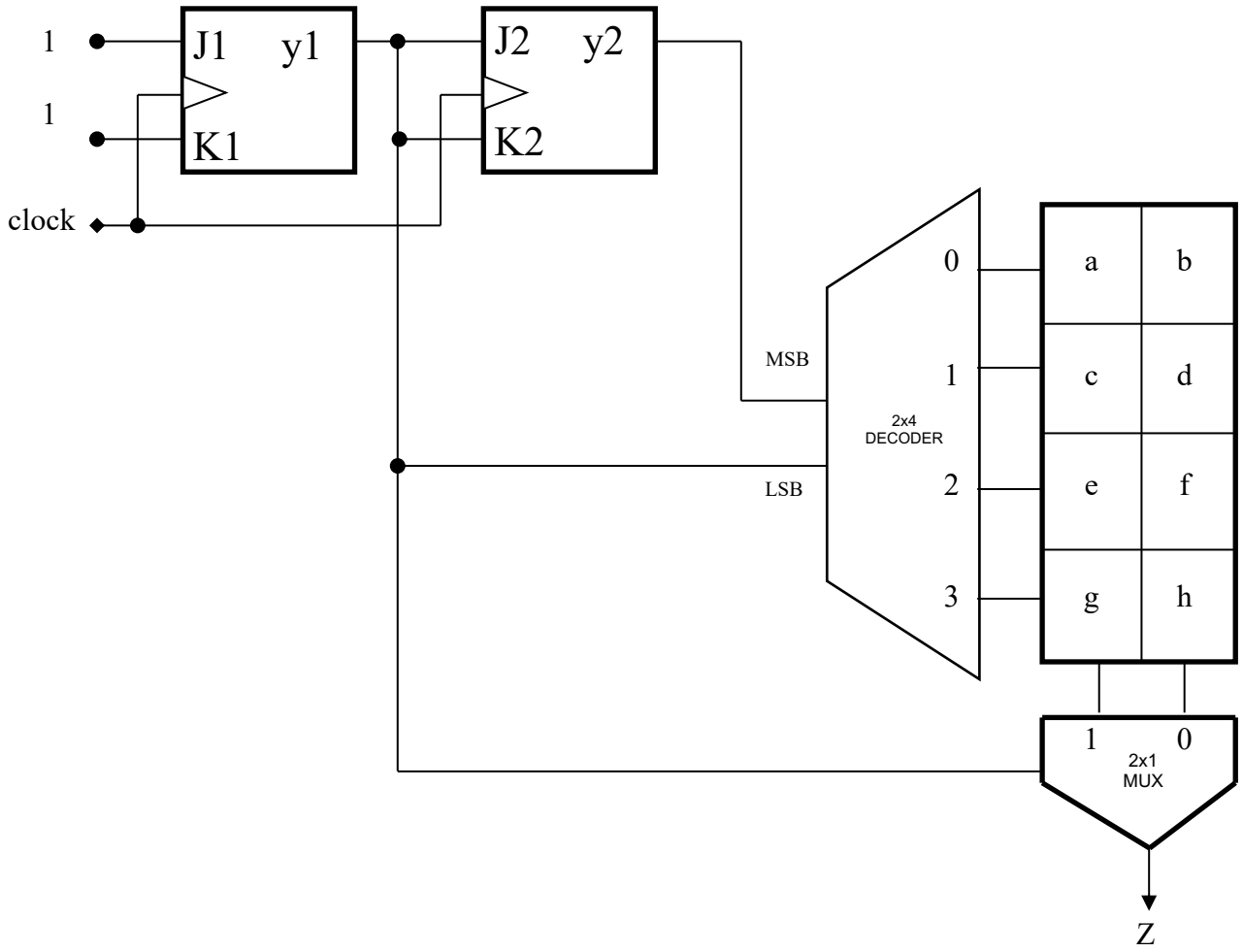
	y_1	y_2	Z
At the beginning	0	0	b
After the 1st pulse	1	0	c
After the 2nd pulse	0	1	f
After the 3rd pulse	1	1	g
After the 4th pulse	0	0	b



QUESTION

Design a one input one output circuit such that as the input is evaluated at every clock, when the input 0101 is detected, output becomes 1, otherwise it is 0. An example input-output sequence is given below.

Input (x)	0	0	1	0	1	0	1	1	1
Output (z)	0	0	0	0	1	0	1	0	0

In other words, design a Mealy type sequential circuit that detects the sequence 0101 using D-type flip flops and logic gates. Your circuit can have a maximum of 2 D-type flip flops.

- Draw the state diagram of the circuit
- Derive the complete state table from the state diagram
- Using Karnaugh-maps, find the most simplified Boolean expressions for flip-flop outputs and the circuit output
- Draw the complete circuit

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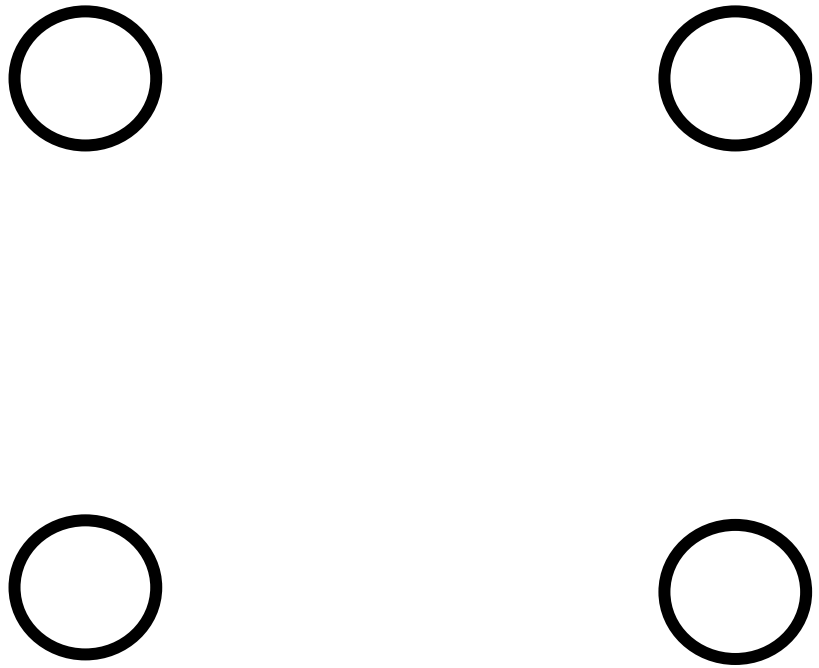

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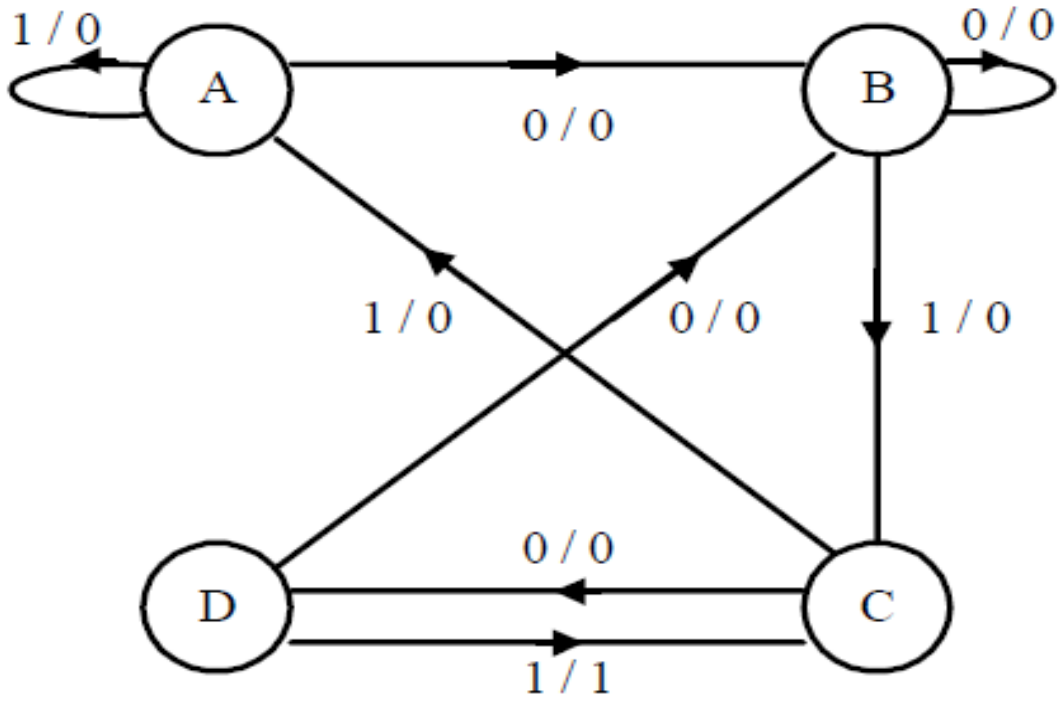


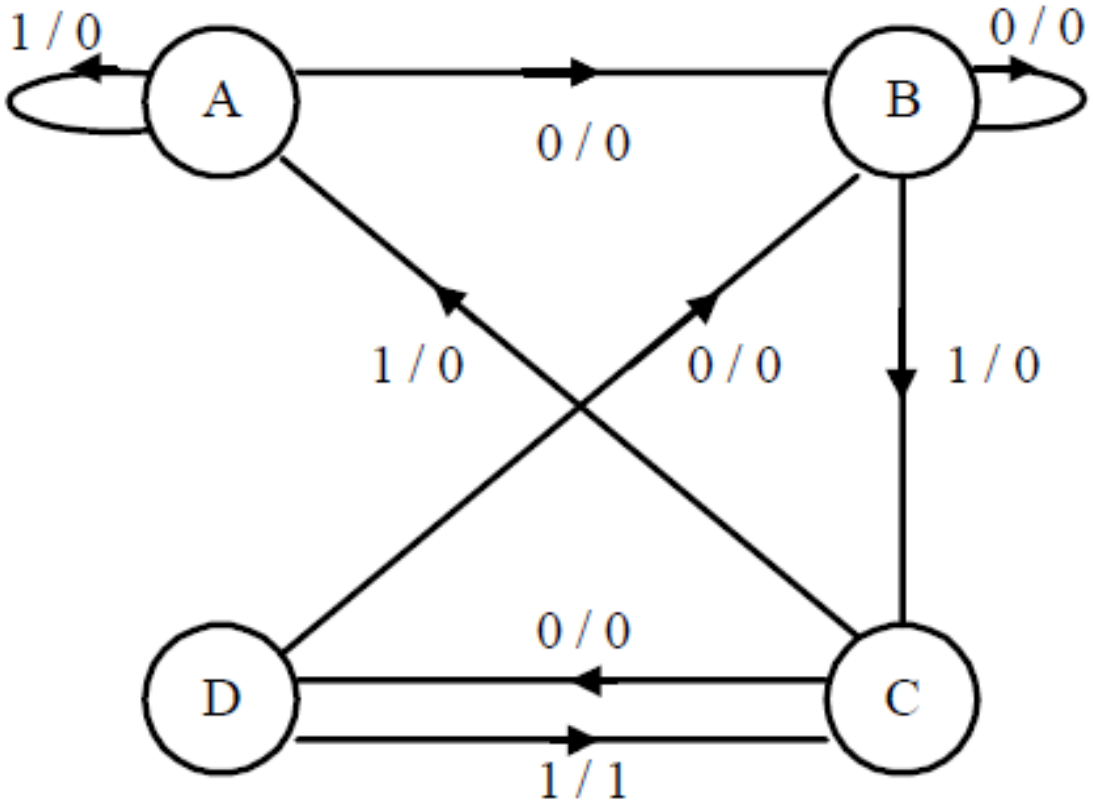
A: Başlangıç durumu
B: 0 gelmiş durumu
C: 01 gelmiş durumu
D: 010 gelmiş durumu

- 4 different states requires 2 D-type FFs using
  - either Binary Encoding
  - or Gray Encoding of states

- One-hot Encoding requires 4 FFs

Using Binary Encoding:

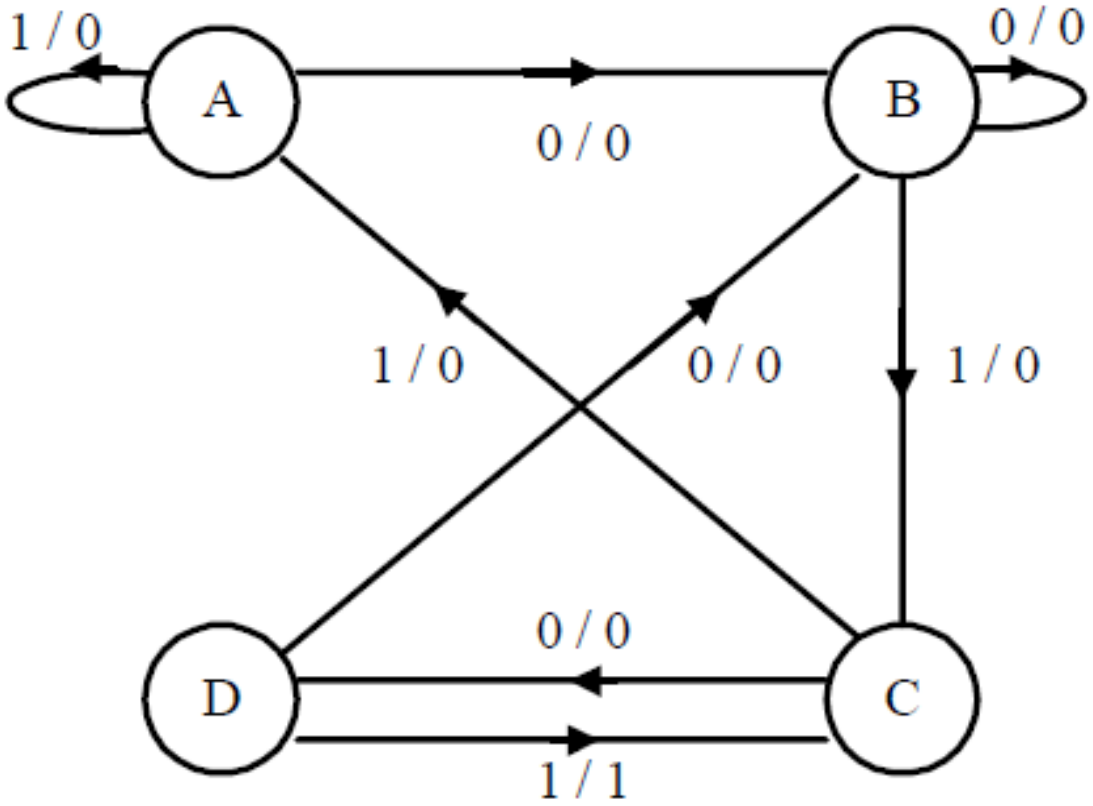
- A=00, B=01, C=10, and D=11.



x	y1	y2	Y1	Y2	z

Using Binary Encoding:

- A=00, B=01, C=10, and D=11.



x	y1	y2	Y1	Y2	z
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	1	0	1

- Binary Encoding:
- A=00, B=01, C=10, and D=11.

x	y1	y2	Y1	Y2	z
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	1	0	1

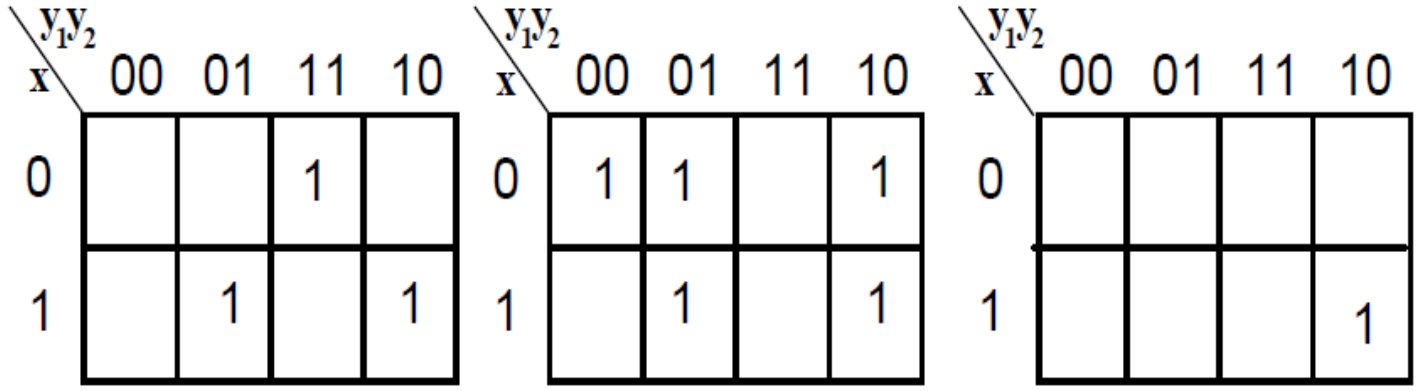
$$Z = xy1y2$$
$$Y1 = xy2 + x'y1y2'$$
$$Y2 = x'$$

- Gray Encoding:
- A=00, B=01, C=11, and D=10

x	y1	y2	Y1	Y2	z
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	0

- Gray Encoding:
- A=00, B=01, C=11, and D=10

x	y1	y2	Y1	Y2	z
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	0



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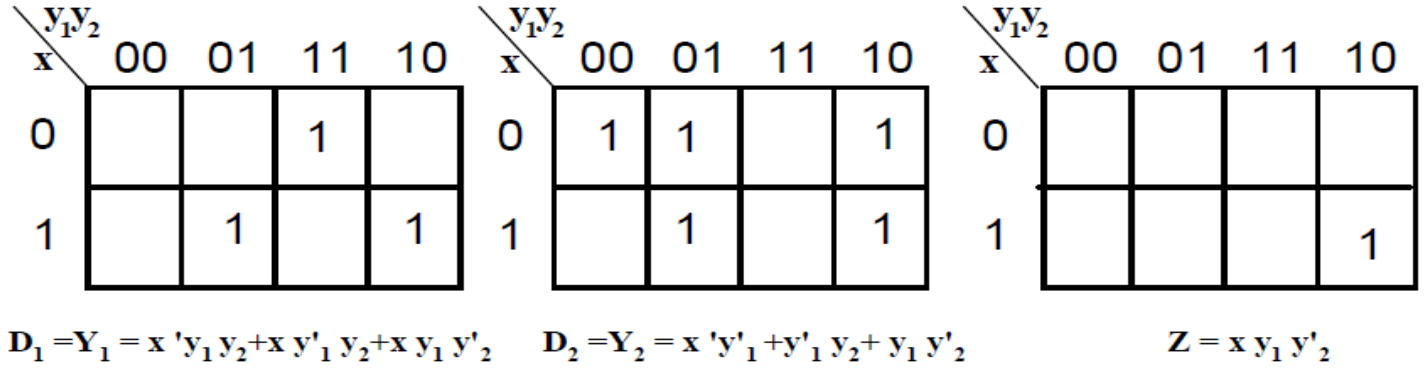
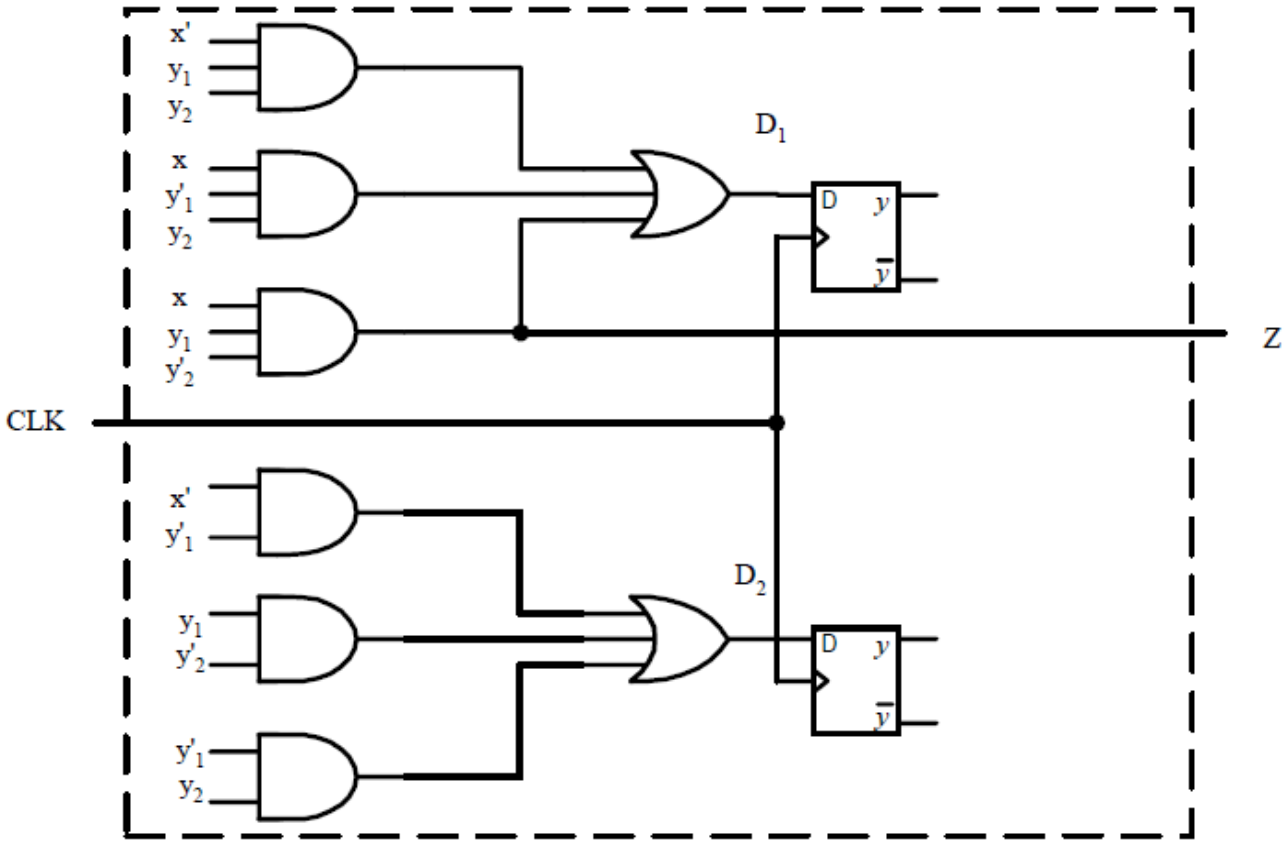


x	y1	y2	Y1	Y2	z
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	0



5.2 Construct a *JK* flip-flop using a *D* flip-flop, a two-to-one-line multiplexer, and an inverter.

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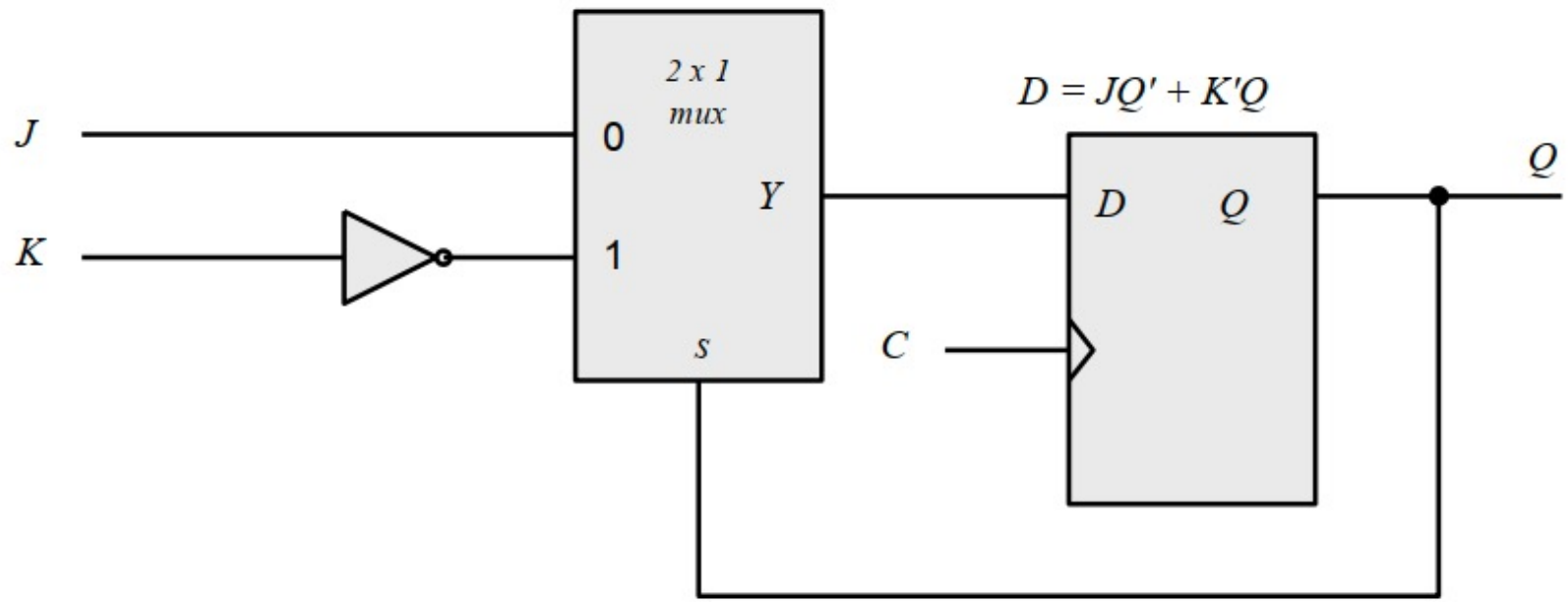

5.5 Explain the differences among a truth table, a state table, a characteristic table, and an excitation table. Also, explain the difference among a Boolean equation, a state equation, a characteristic equation, and a flip-flop input equation.

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The truth table describes a combinational circuit.
The state table describes a sequential circuit.
The characteristic table describes the operation of a flip-flop.
The excitation table gives the values of flip-flop inputs for a given state transition.
The four equations correspond to the algebraic expression of the four tables.

5.6 A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is specified by the following next-state and output equations

$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

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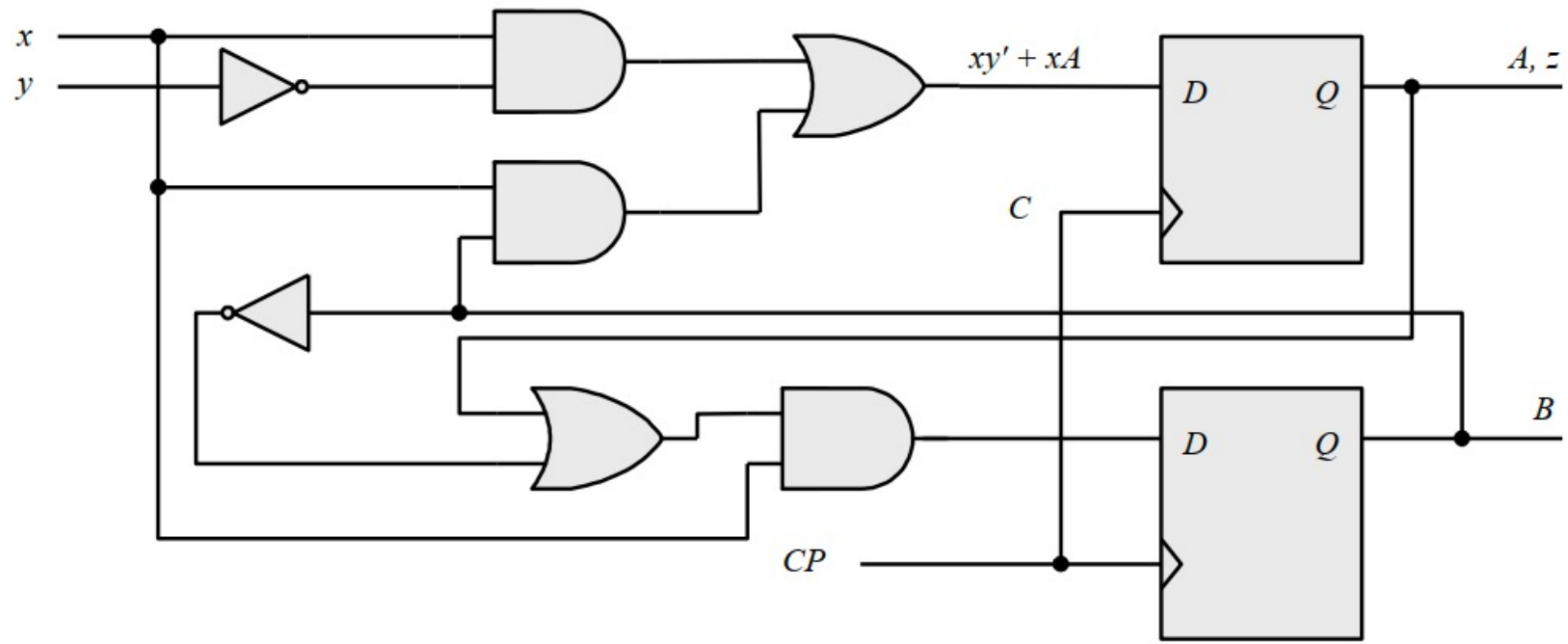

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(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

(b)

Present state		*Inputs*		*Next state*		*Output*
A	*B*	*x*	*y*	*A*	*B*	*z*
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
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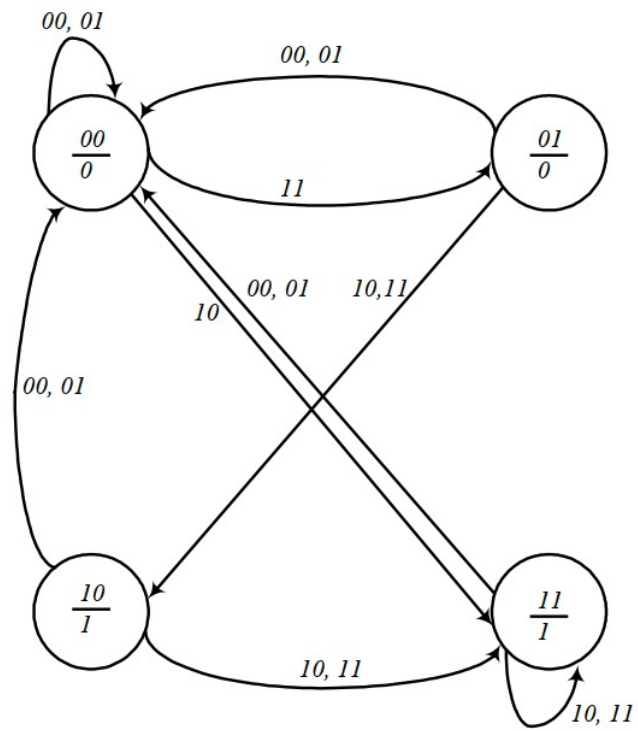
(b)

Present state		Inputs		Next state		Output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

(c)



5.7* A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in Fig. P5.7. Derive the state table and state diagram of the sequential circuit.

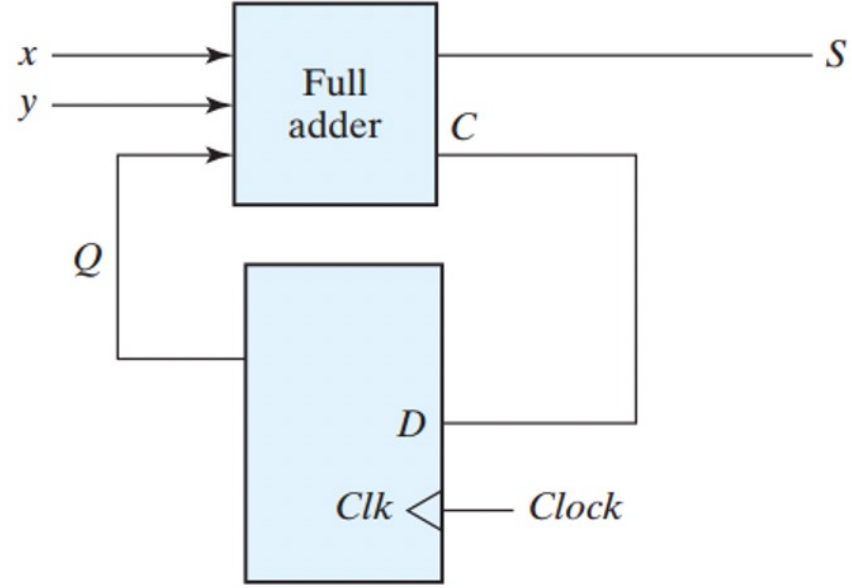


FIGURE P5.7

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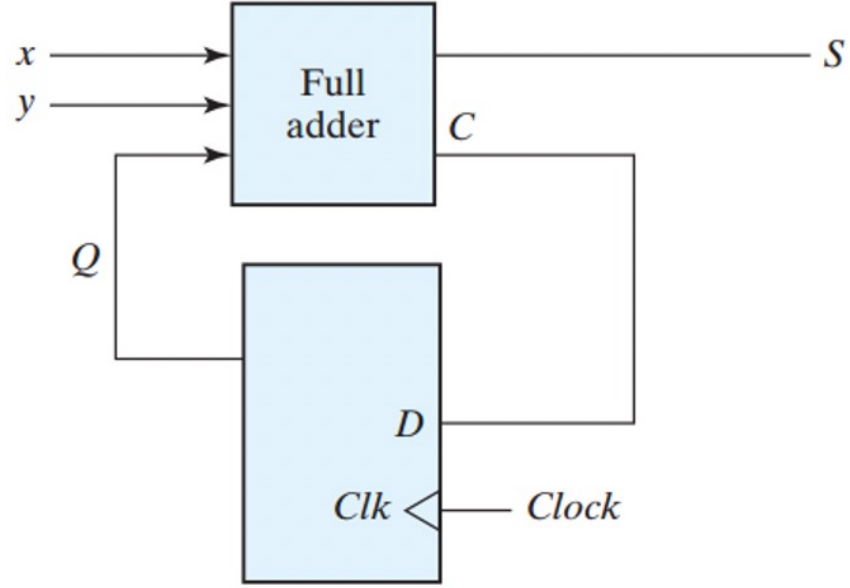
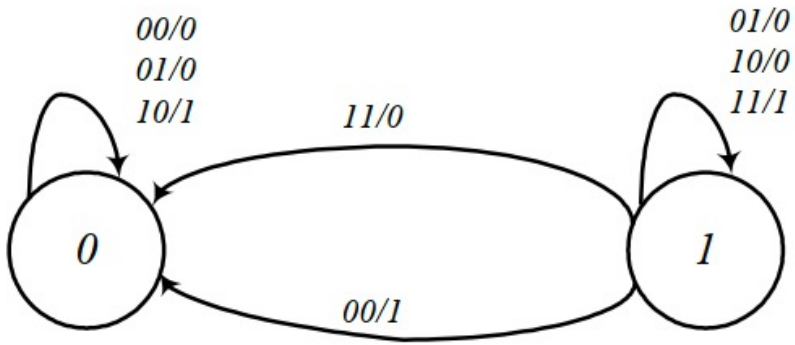


FIGURE P5.7

Present state	Inputs		Next state	Output
Q	x	y	Q	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$$S = x \oplus y \oplus Q$$
$$Q(t+1) = xy + xQ + yQ$$

5.8* Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8. Explain the function that the circuit performs. (HDL—see Problem 5.36.)

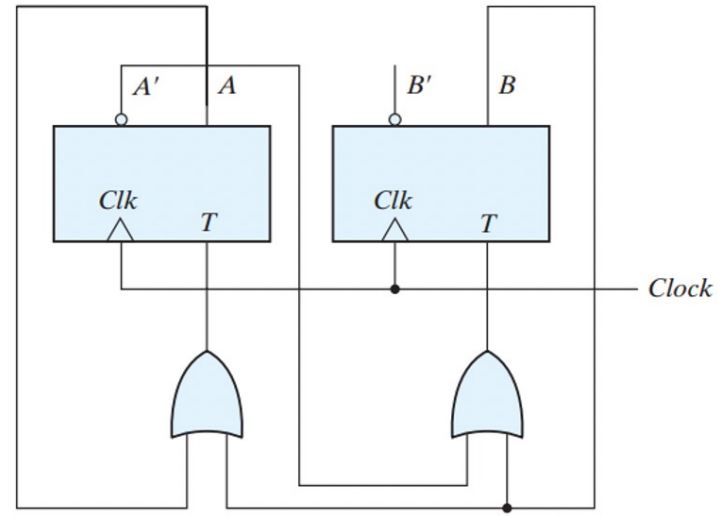


FIGURE P5.8

5.8* Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8. Explain the function that the circuit performs. (HDL—see Problem 5.36.)

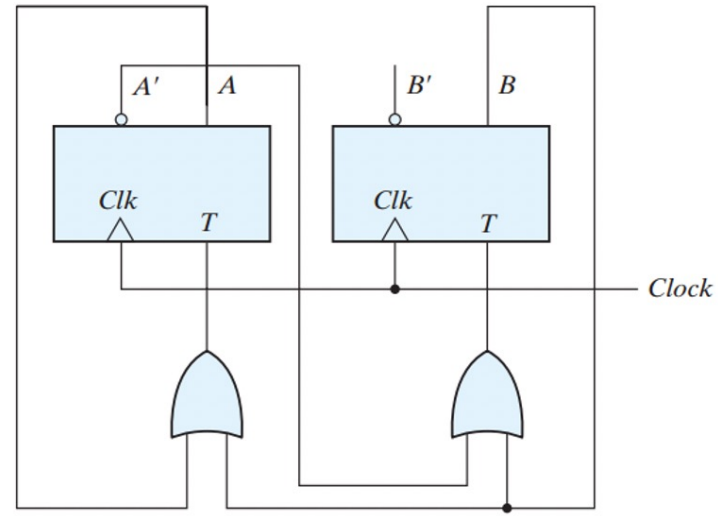


FIGURE P5.8

Present state		Next state		FF Inputs	
A	B	A	B	T_A	T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1

$$T_A = A + B$$
$$T_B = A' + B$$

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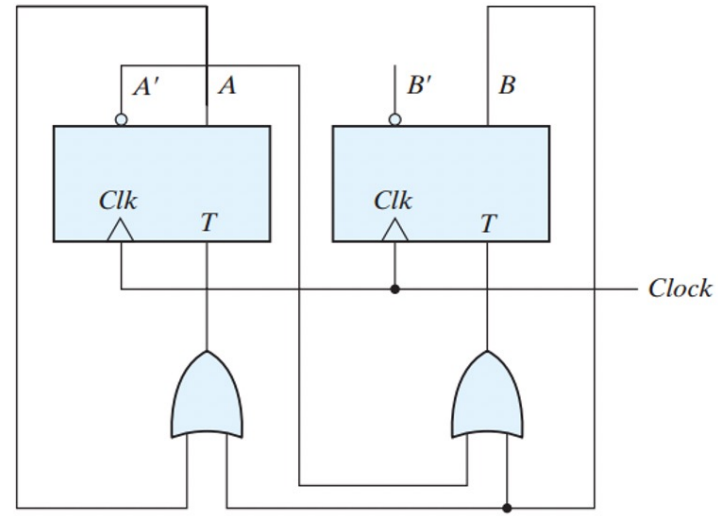


FIGURE P5.8

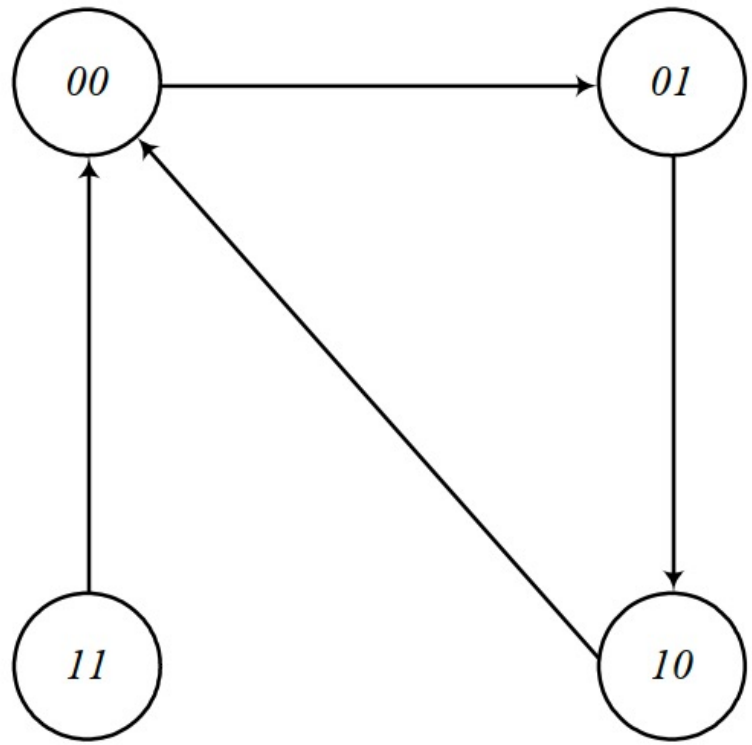
A counter with a repeated sequence of 00, 01, 10.

Present state A	Present state B	Next state A	Next state B	FF Inputs T_A	FF Inputs T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1

$$T_A = A + B$$
$$T_B = A' + B$$

Repeated sequence:

00 → 01 → 10 →



5.9 A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

$$J_A = x \quad K_A = B$$
$$J_B = x \quad K_B = A'$$

(a) Derive the state equations $A(t + 1)$ and $B(t + 1)$ by substituting the input equations for the J and K variables.
(b) Draw the state diagram of the circuit.

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$$J_A = x \qquad K_A = B$$
$$J_B = x \qquad K_B = A'$$

$$A(t+1) = J_A A' + K_A' A = xA' + B'A$$
$$B(t+1) = J_B B' + K_B' B = xB' + AB$$

x	A	B	$xA' + B'A$	$xB' + AB$
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

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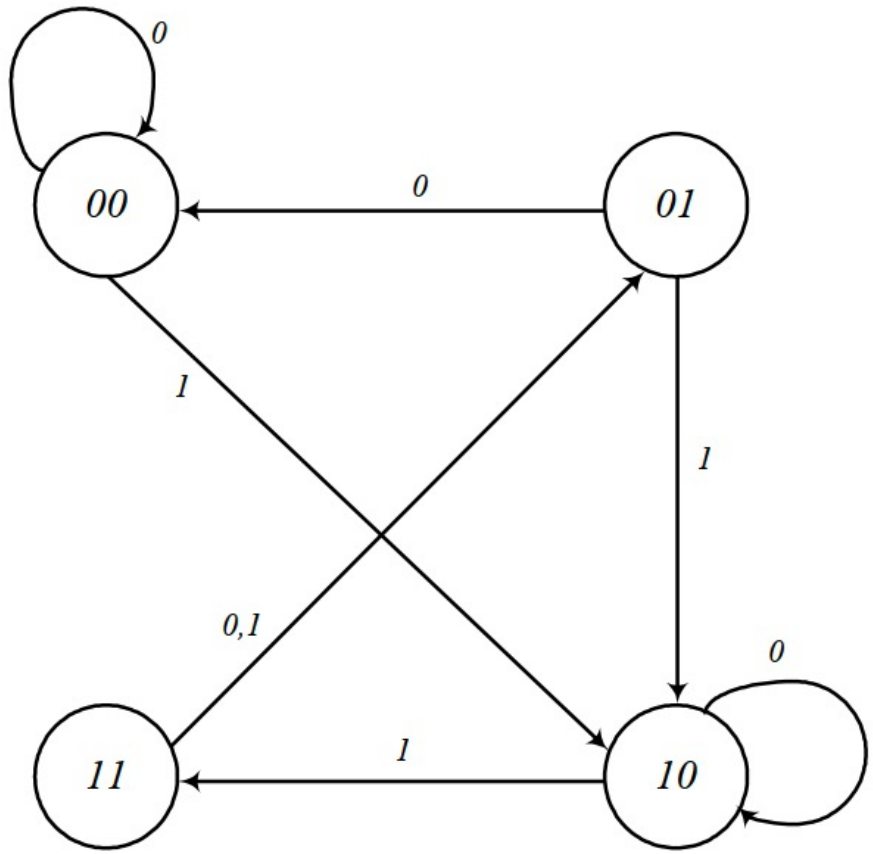
$$J_A = x \qquad K_A = B$$
$$J_B = x \qquad K_B = A'$$

$$A(t+1) = J_A A' + K_A' A = xA' + B'A$$
$$B(t+1) = J_B B' + K_B' B = xB' + AB$$

x	A	B	$xA' + B'A$	$xB' + AB$
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1



5.10 A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c) Derive the state equations for A and B.

5.10 A sequential circuit has two *JK* flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c) Derive the state equations for A and B.

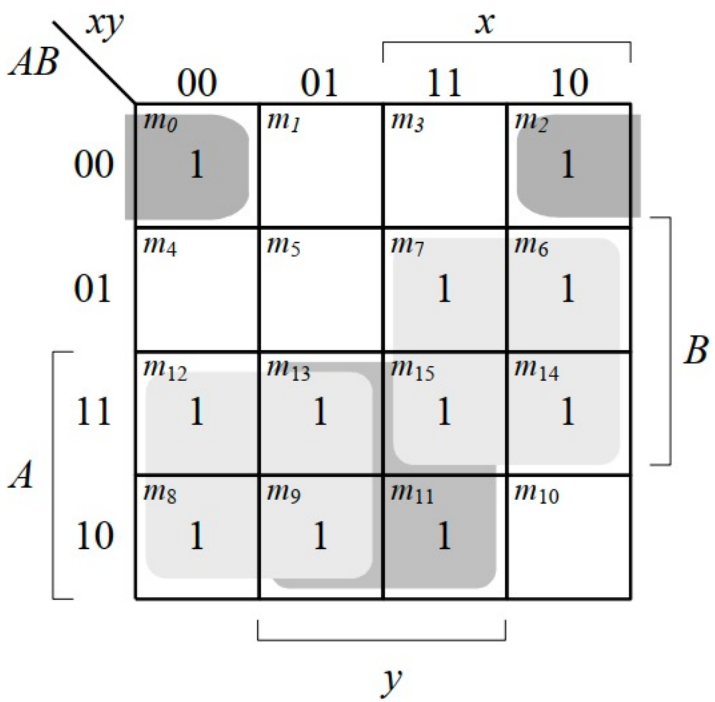
(b)

Present state		*Inputs*		*Next state*		*Output*	*FF Inputs*			
A	B	x	y	A	B	z	J_A	K_A	J_A	J_B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	1	0	1	0
0	1	1	1	1	1	0	1	0	1	0
1	0	0	0	1	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1
1	1	1	1	1	0	1	1	0	0	1

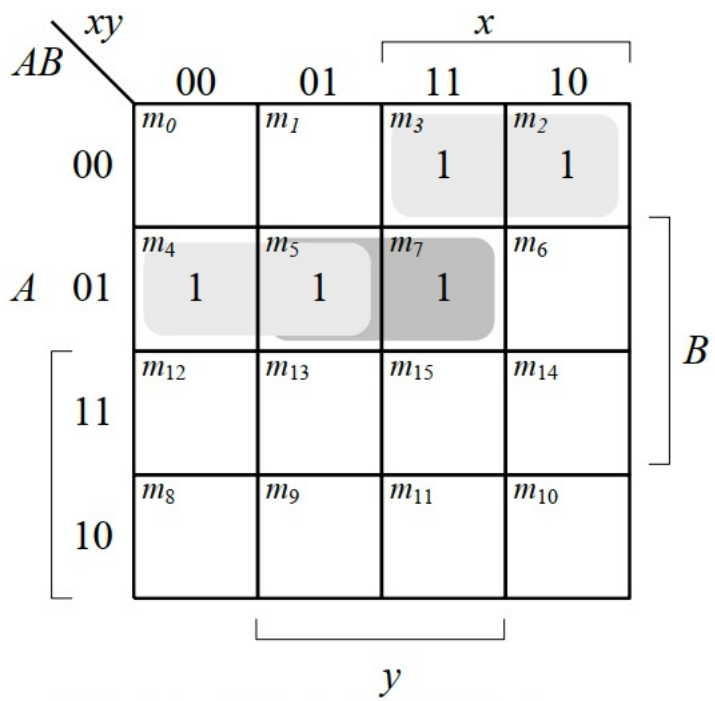
5.10 A sequential circuit has two *JK* flip-flops *A* and *B*, two inputs *x* and *y*, and one output *z*. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c) Derive the state equations for *A* and *B*.



$A(t+1) = Ax' + Bx + Ay + A'B'y'$



$B(t+1) = A'B'x + A'B'(x' + y)$

(b)

Present state		Inputs		Next state		Output	FF Inputs			
A	*B*	*x*	*y*	*A*	*B*	*z*	J_A	K_A	J_A	J_B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	1	0	1	0
0	1	1	1	1	1	0	1	0	1	0
1	0	0	0	1	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1
1	1	1	1	1	0	1	1	0	0	1

5.11 For the circuit described by the state diagram of Fig. 5.16,

(a)* Determine the state transitions and output sequence that will be generated when an input sequence of 010110111011110 is applied to the circuit and it is initially in the state 00.

(b) Find all of the equivalent states in Fig. 5.16 and draw a simpler, but equivalent, state diagram.

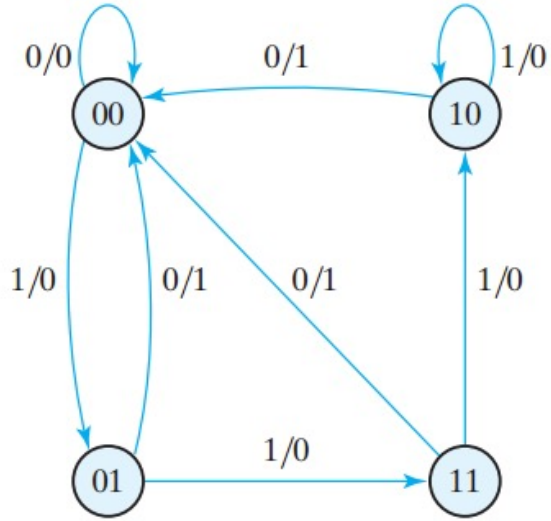


FIGURE 5.16

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(a)* Determine the state transitions and output sequence that will be generated when an input sequence of 010110111011110 is applied to the circuit and it is initially in the state 00.

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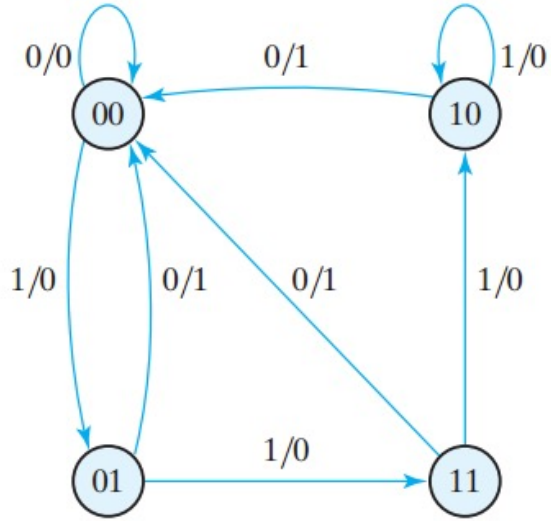


FIGURE 5.16

(a)

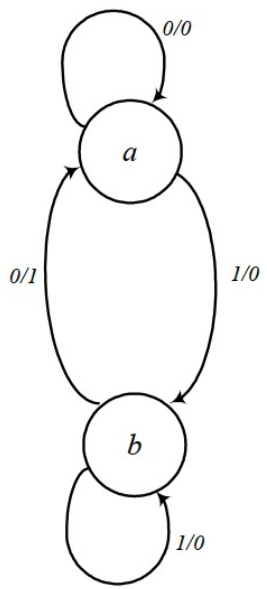
Present state:	00	00	01	00	01	11	00	01	11	10	00	01	11	10	10
Input:	0	1	0	1	1	0	1	1	1	0	1	1	1	1	0
Output:	0	0	1	0	0	1	0	0	0	1	0	0	0	0	1
Next state:	00	01	00	01	11	00	01	11	10	00	01	11	10	10	00

(b)

State labels: a: 00, b: 10, c: 11, d: 01

c is equivalent to b

d is equivalent to c



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(c) Using *D* flip-flops, design the equivalent machine (including its logic diagram) described by the state diagram in (b).

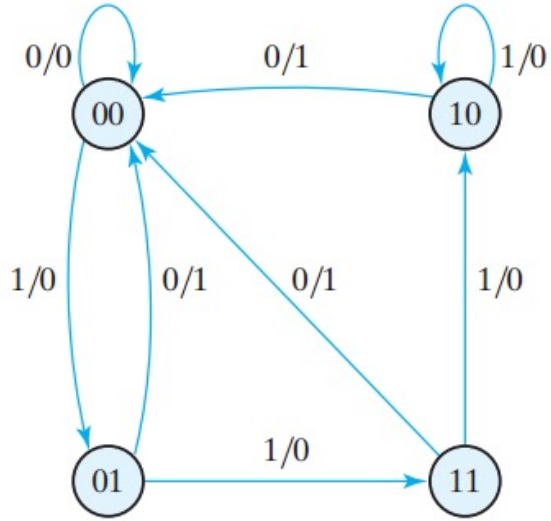

FIGURE 5.16

5.11 For the circuit described by the state diagram of Fig. 5.16,

(a)* Determine the state transitions and output sequence that will be generated when an input sequence of 010110111011110 is applied to the circuit and it is initially in the state 00.

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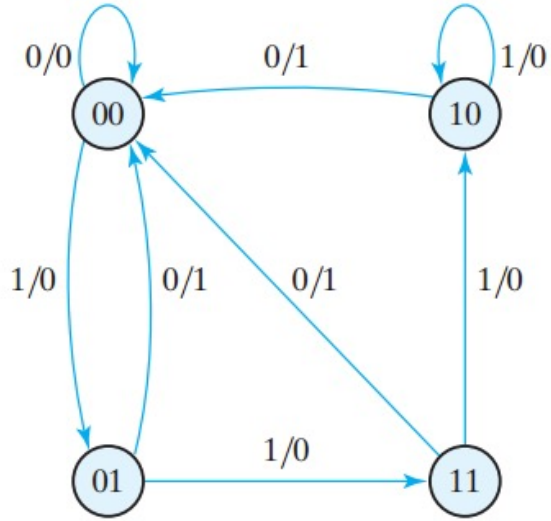

FIGURE 5.16

(c)

input	state	next st	output
0	0	0	0
1	0	1	0
0	1	0	0
1	1	1	1

State machine: D-flop with direct input of the input to the original machine;
output logic: y = (!input) && (state == b)

5.12 For the following state table

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(a) Draw the corresponding state diagram.
(b)* Tabulate the reduced state table.
(c) Draw the state diagram corresponding to the reduced state table.

5.12 For the following state table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(a) Draw the corresponding state diagram.
(b)* Tabulate the reduced state table.
(c) Draw the state diagram corresponding to the reduced state table.

Present state	Next state 0	Next state 1	Output 0	Output 1
a	f	b	0	0
b	d	a	0	0
d	g	a	1	0
f	f	b	1	1
g	g	d	0	1

5.18* Design a sequential circuit with two *JK* flip-flops A and B and two inputs E and F. If $E = 0$, the circuit remains in the same state regardless of the value of F. When $E = 1$ and $F = 1$, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When $E = 1$ and $F = 0$, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.

5.18* Design a sequential circuit with two *JK* flip-flops *A* and *B* and two inputs *E* and *F*. If $E = 0$, the circuit remains in the same state regardless of the value of *F*. When $E = 1$ and $F = 1$, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When $E = 1$ and $F = 0$, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.

Q(t)Q(t+1)	00	01	11	10
J,K	0,X	1,X	X,0	X,1

Present state $A\ B$	*Input* x	*Next state* $A\ B$	*Flip-flop inputs* $J_A\ K_A\ J_B\ K_B$
0 0	0 1	0 0	
0 0	0 1	0 0	
0 0	1 0	1 1	
0 0	1 1	0 1	
0 1	0 0	0 1	
0 1	0 1	0 1	
0 1	1 0	0 1	
0 1	1 1	1 0	
1 0	0 0	1 0	
1 0	0 1	1 0	
1 0	1 0	0 1	
1 0	1 1	1 1	
1 1	0 0	1 1	
1 1	0 1	1 1	
1 1	1 0	1 1	
1 1	1 1	1 1	

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Q(t)Q(t+1)	00	01	11	10
J,K	0,X	1,X	X,0	X,1

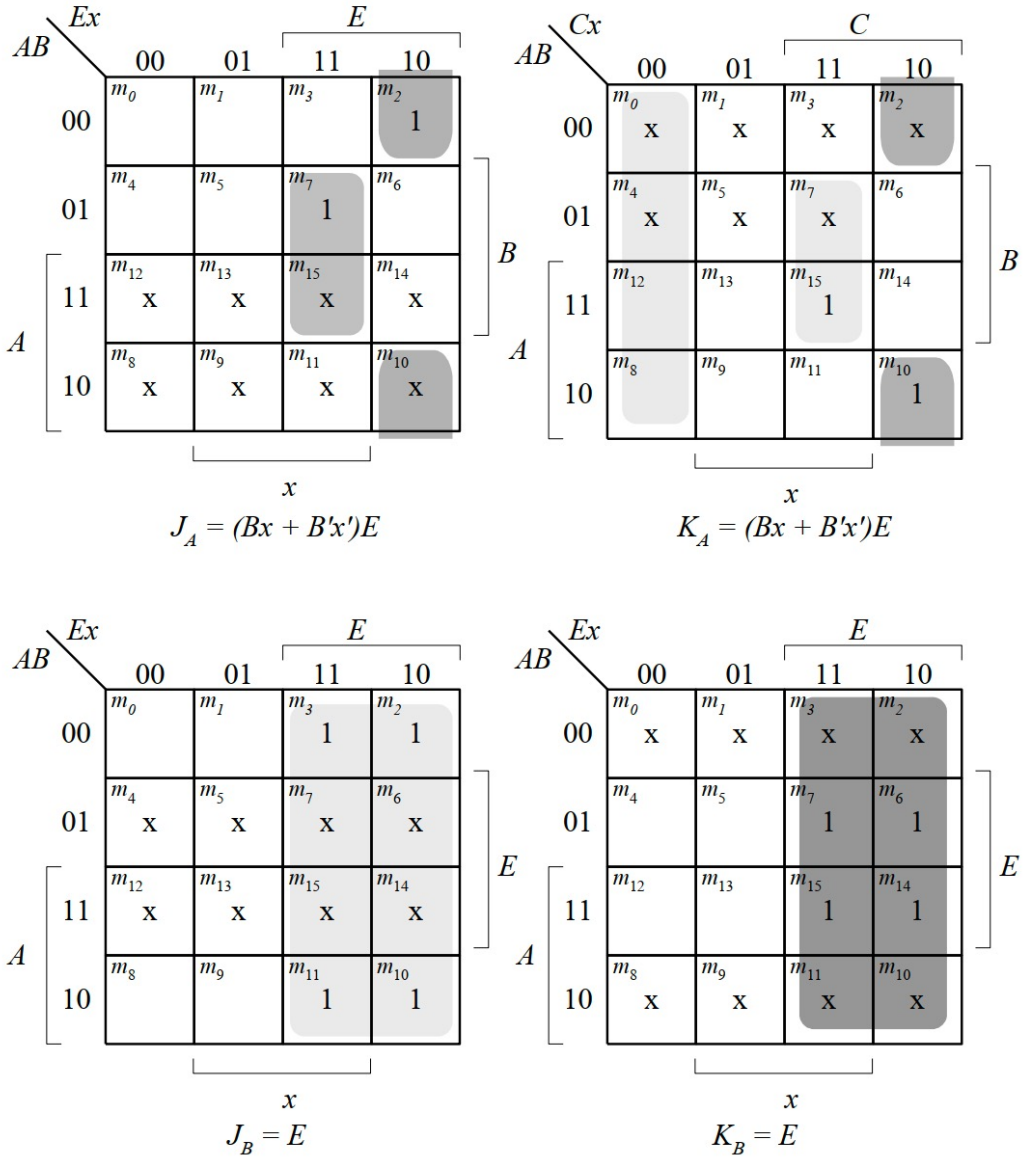
Present state A B	*Input* x	*Next state* A B	*Flip-flop inputs* J_A K_A	J_B K_B
0 0	0 1	0 0	0 x	0 x
0 0	0 1	0 0	0 x	0 x
0 0	1 0	1 1	1 x	1 x
0 0	1 1	0 1	0 x	1 x
0 1	0 0	0 1	0 x	x 0
0 1	0 1	0 1	0 x	x 0
0 1	1 0	0 1	0 x	x 1
0 1	1 1	1 0	1 x	x 1
1 0	0 0	1 0	x 0	1 0
1 0	0 1	1 0	x 0	1 0
1 0	1 0	0 1	x 1	x 1
1 0	1 1	1 1	x 0	x 1
1 1	0 0	1 1	x 0	x 0
1 1	0 1	1 1	x 0	x 0
1 1	1 0	1 1	1 0	x 1
1 1	1 1	1 1	x 1	x 1

5.18* Design a sequential circuit with two *JK* flip-flops *A* and *B* and two inputs *E* and *F*. If $E = 0$, the circuit remains in the same state regardless of the value of *F*. When $E = 1$ and $F = 1$, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When $E = 1$ and $F = 0$, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.

Binary up-down counter with enable *E*.

Present state *A B*	*Input* *x*	*Next state* *A B*	*Flip-flop inputs* J_A K_A	J_B K_B
0 0	0 1	0 0	0 x	0 x
0 0	0 1	0 0	0 x	0 x
0 0	1 0	1 1	1 x	1 x
0 0	1 1	0 1	0 x	1 x
0 1	0 0	0 1	0 x	x 0
0 1	0 1	0 1	0 x	x 0
0 1	1 0	0 1	0 x	x 1
0 1	1 1	1 0	1 x	x 1
1 0	0 0	1 0	x 0	1 0
1 0	0 1	1 0	x 0	1 0
1 0	1 0	0 1	x 1	x 1
1 0	1 1	1 1	x 0	x 1
1 1	0 0	1 1	x 0	x 0
1 1	0 1	1 1	x 0	x 0
1 1	1 0	1 1	1 0	x 1
1 1	1 1	1 1	x 1	x 1

5.18* Design a sequential circuit with two *JK* flip-flops *A* and *B* and two inputs *E* and *F*. If $E = 0$, the circuit remains in the same state regardless of the value of *F*. When $E = 1$ and $F = 1$, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When $E = 1$ and $F = 0$, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.



5.19 A sequential circuit has three flip-flops *A*, *B*, *C*; one input *x_in*; and one output *y_out*. The state diagram is shown in Fig. P5.19. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.

(a)* Use *D* flip-flops in the design.
(b) Use *JK* flip-flops in the design.

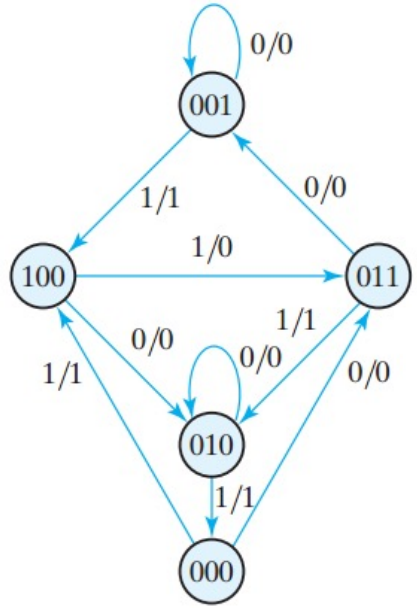


FIGURE P5.19

5.19 A sequential circuit has three flip-flops *A, B, C*; one input *x_in*; and one output *y_out*. The state diagram is shown in Fig. P5.19. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.

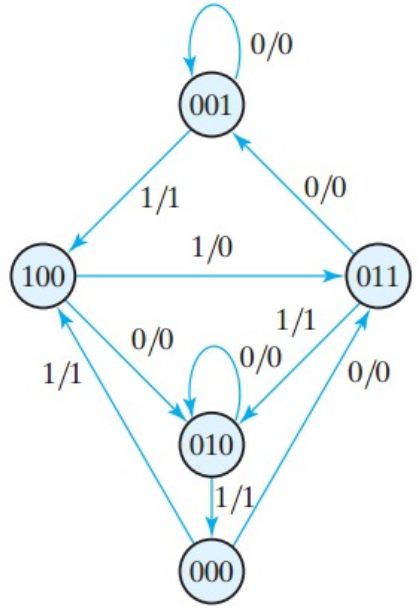


FIGURE P5.19

(a)* Use *D* flip-flops in the design.
(b) Use *JK* flip-flops in the design.

(a) Unused states (see Fig. P5.19): 101, 110, 111.

Present state ABC	*Input x*	*Next state ABC*	*Output y*
000	0	011	0
000	1	100	1
001	0	001	0
001	1	100	1
010	0	010	0
010	1	000	1
011	0	001	0
011	1	010	1
100	0	010	0
100	1	011	1

$d(A, B, C, x) = \Sigma\,(10, 11, 12, 13, 14, 15)$

5.19 A sequential circuit has three flip-flops *A*, *B*, *C*; one input *x_in*; and one output *y_out*. The state diagram is shown in Fig. P5.19. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.

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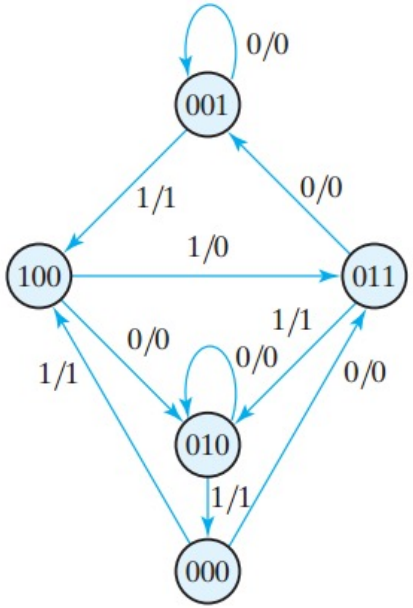
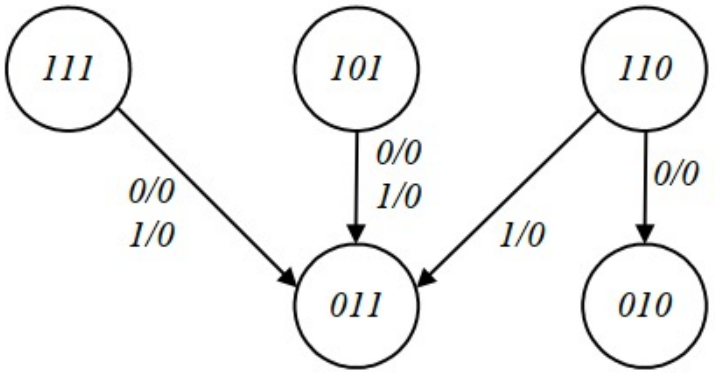
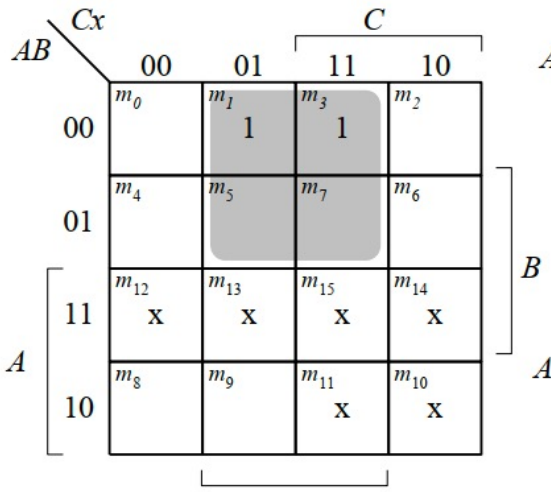


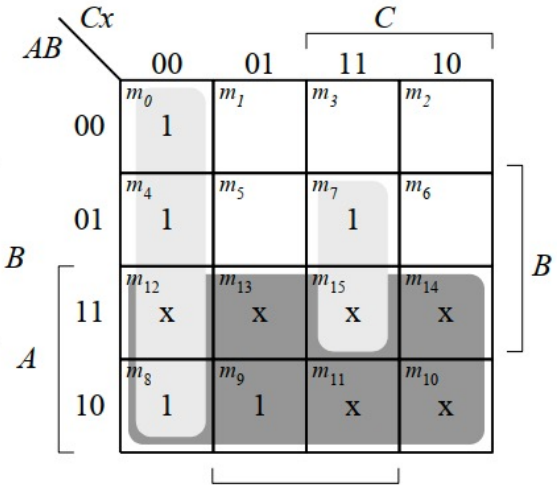
FIGURE P5.19

The machine is self-correcting, i.e., the unused states transition to known states.

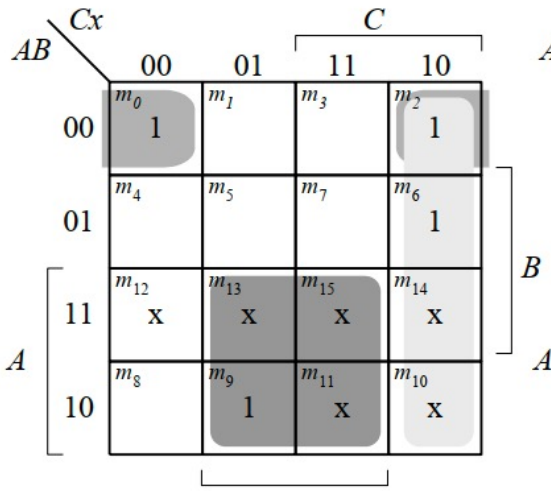




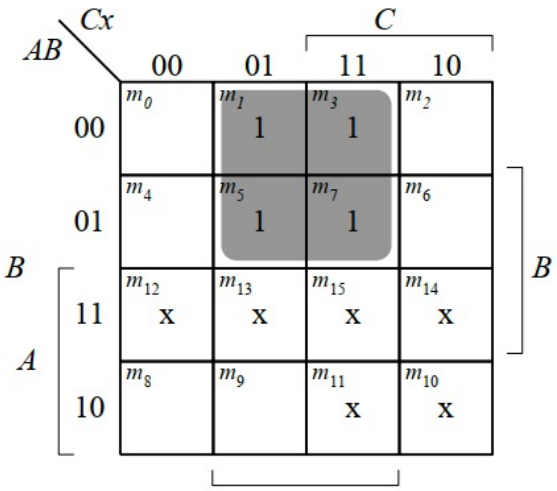
$D_A = A'B'x$



$D_B = A + C'x' + BCx$



$D_C = Cx' + Ax + A'B'x'$



$y = A'x$

5.19 A sequential circuit has three flip-flops *A, B, C*; one input *x_in*; and one output *y_out*. The state diagram is shown in Fig. P5.19. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.

(a)* Use *D* flip-flops in the design.
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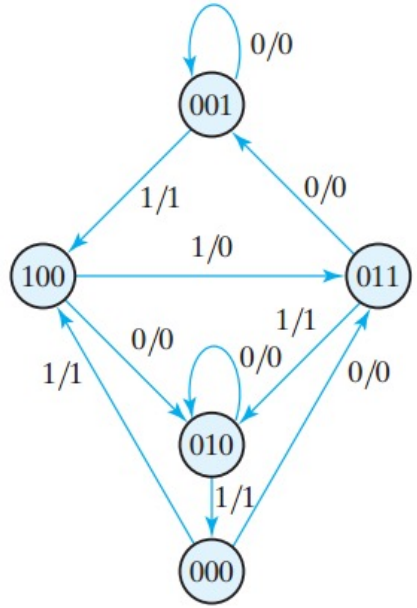

FIGURE P5.19

(b) With JK flip=flops, the state table is the same as in (a).

Flip-flop inputs					
J_A	K_A	J_B	K_B	J_C	K_C
0	x	1	x	1	x
1	x	0	x	0	x
0	x	0	x	x	0
1	x	0	x	x	1
0	x	x	0	0	x
0	x	x	1	0	x
0	x	x	1	x	0
0	x	x	0	x	1
x	1	1	x	0	x
x	1	1	x	1	x

$J_A = B'x$ $\quad K_A = 1$
$J_B = A + C'x'$ $\quad K_B = C'x + Cx'$
$J_C = Ax + A'B'x'$ $\quad K_C = x$
$y = A'x$

The machine is self-correcting because $K_A = 1$.