Computer Architecture
Spring 2019
Homework No. 5
(Due on June 8)

1.

slt $1, $2, $3

Control Signal	**Bit**
RegDst	1
Branch	0
MemRead	0
MemtoReg	0
ALUOP	10
MemWrite	0
ALUSrc	0
RegWrite	1

2.

jr $ra

Control Signal	**Bit**
RegDst	Don’t care
Jump	1
Branch	0
MemRead	0
MemtoReg	Don’t care
ALUOP	Don’t care
MemWrite	0
ALUSrc	Don’t care
RegWrite	0

3.

Nonpipelined: 100 * 800ps = 80,000 ps

Pipelined: 800 + 200 * (100 - 1) = 20,600 ps

Speedup≈ 3.88

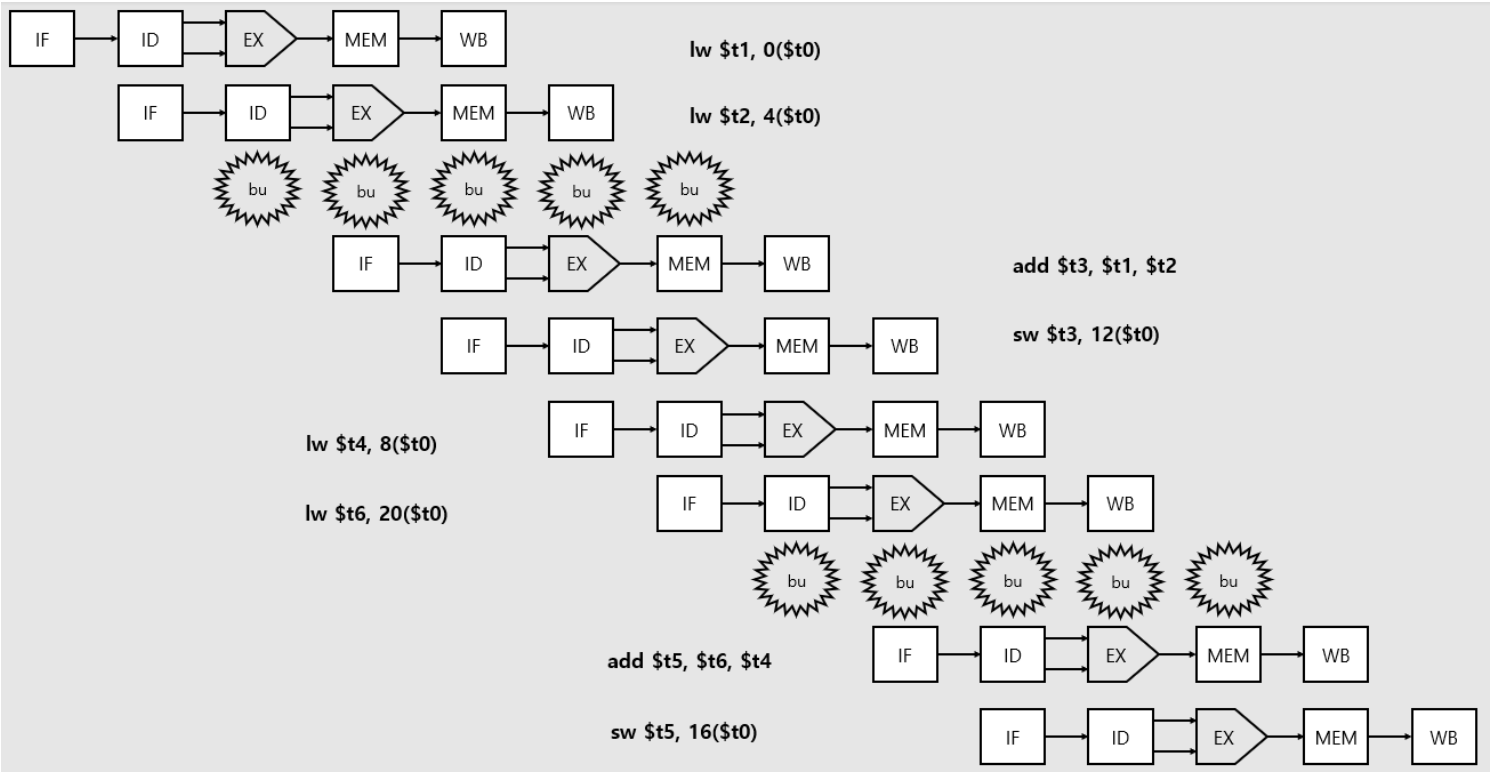
Maximum speedup: 4

4.

1) No delayed load

lw $t1, 0($t0)
lw $t2, 4($t0)
add $t3, $t1, $t2
< stall >
sw $t3, 12($t0)
lw $t4, 8($t0)
lw $t6, 20($t0)
add $t5, $t6, $t4
< stall >
sw $t5, 16($t0)

Total Cycle: 5 + 1 * (10 - 1) = 14



2) Delayed load

lw $t1, 0($t0)
lw $t2, 4($t0)
lw $t4, 8($t0)
lw $t6, 20($t0)
add $t3, $t1, $t2
sw $t3, 12($t0)
add $t5, $t6, $t4
sw $t5, 16($t0)

Total Cycle: 5 + 1 * (8 - 1) = 12