U105
74HC138D

Pin	Signal	Description
A (1)	CS0*	
B (2)	CS1*	
C (3)	CS2*	

+5V_D

OE1 (6)
OE2A (4)
OE2B (5)

Output	Pin	Signal	Description
Y̅0	15	CS1**	Selects Single, 16-bit, parallel load, Mass DAC
Y̅1	14	CS2**	Not used.
Y̅2	13	CS3**	Selects QUAD, 14-bit, parallel load, DAC. Address lines A00 and A01 select 1-of-4 DAC's
Y̅3	12	CS4**	Selects 8 channel, ADC1 via serial interface.
Y̅4	11	CS5**	Selects 8 channel, ADC2 via serial interface.
Y̅5	10	TP111 CS6**	Not used.
Y̅6	9	TP109 CS7**	Not used.
Y̅7	7	TP110 CS8**	Not used.

S101:1 16 — 1 BS1*
S101:2 15 — 2 BS2*
S101:3 14 — 3 BS3*
S101:4 13 — 4 BS4*
S101:5 12 — 5 BS5*
S101:6 11 — 6 BS6*
S101:7 10 — 7 BS7*
S101:8 9 — 8

+5V_D

C113
0.1uF

+5V_D

R105
10K0

DAC and ADC addressing table.

$\overline{BS1}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	A0	A1	DAC Selected
0	0	0	0	X	X	MASS
0	0	1	0	0	0	RO
0	0	1	0	0	1	RES
0	0	1	0	1	0	Lens OS
0	0	1	0	1	1	Q0
0	0	1	1	X	X	ADC1
0	1	0	0	X	X	ADC2
select via serial port, see AD7834 data sht						FR
select via serial port, see AD7834 data sht						ST
select via serial port, see AD7834 data sht						IQ1
select via serial port, see AD7834 data sht						OR

IONICS
DAC and ADC addressing
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