# CMOS Inverter Characterization using SkyWater 130nm PDK and Ngspice

Dikshit Singla, 23b3974

August 17, 2025

**Abstract**

This report presents the design and characterization of a minimum-size CMOS inverter using the SkyWater 130nm PDK in Ngspice. Both transient and DC analyses were performed to extract switching parameters such as propagation delay, rise/fall times, switching threshold ($V_M$), noise margins ($NM_L$, $NM_H$), and voltage thresholds ($V_{IL}$, $V_{IH}$). The results are compared against expected theoretical behavior.

## 1 Objective

- To simulate a minimum-size CMOS inverter using the SkyWater 130A PDK.
- To measure dynamic parameters (rise time, fall time, propagation delays).
- To measure static parameters ($V_M$, $V_{IL}$, $V_{IH}$, $NM_L$, $NM_H$) using DC transfer characteristics.

## 2 Circuit Description

The inverter circuit was implemented using the minimum allowed gate lengths. The NMOS device has $W_n = 0.42\,\mu m$, while the PMOS device has $W_p = 2\,\mu m$.

### 2.1 Ngspice Netlist

**Ques1-1.cir code for transient**

```
* SkyWater PDK
* Minimum size CMOS inverter
* VDD = 1.8 V, Lmin = 0.15um, Wn(min) = 0.42um

.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt

*the voltage sources:
Vdd vdd gnd DC 1.8
V1 in gnd pulse(0 1.8 0p 20p 10p 1n 2n)
```

```
Xnot1 in vdd gnd inter not1
Xnot2 inter vdd gnd load not1

.subckt not1 a vdd vss z
xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w=2 as=0.6 ad=0.6 ps=4.6 pd=4.6
xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=0.42 as=0.126 ad=0.126 ps=1.44 pd=1
C0 z a 0.2f
C1 a vdd 0.2f
C2 z vdd 0.2f
C3 z vss 0.4f
C4 a vss 0.6f
C5 vdd vss 1f
.ends

* simulation command:
.tran 1ps 10ns 0 10p

.measure tran trise TRIG v(load) VAL={0.2*1.8} RISE=1 TARG v(load) VAL={0.8*1.8} RISE
.measure tran tfall TRIG v(load) VAL={0.8*1.8} FALL=1 TARG v(load) VAL={0.2*1.8} FALL
.measure tran tpHL  TRIG v(in)   VAL={0.5*1.8} FALL=1 TARG v(load) VAL={0.5*1.8} FALL
.measure tran tpLH  TRIG v(in)   VAL={0.5*1.8} RISE=1 TARG v(load) VAL={0.5*1.8} RISE
.measure tran tp_avg PARAM='(tpHL + tpLH)/2'

.control
run
plot in load

.endc
```

**Ques1-2.cir code for dc sweep**

```
* SkyWater PDK
* Minimum size CMOS inverter
* VDD = 1.8 V, Lmin = 0.15um, Wn(min) = 0.42um

.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt

*the voltage sources:
Vdd vdd gnd DC 1.8
V1 in gnd pulse(0 1.8 0p 20p 10p 1n 2n)

Xnot1 in vdd gnd inter not1
Xnot2 inter vdd gnd load not1

.subckt not1 a vdd vss z
xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w=2 as=0.6 ad=0.6 ps=4.6 pd=4.6
xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=0.42 as=0.126 ad=0.126 ps=1.44 pd=1
C0 z a 0.2f
```

```
C1 a vdd 0.2f
C2 z vdd 0.2f
C3 z vss 0.4f
C4 a vss 0.6f
C5 vdd vss 1f
.ends
* simulation command:
.dc V1 0 1.8 0.001


.control
run
let vin = v(in)
let vout = v(inter)

* Reference line 1: slope -1 through (0.8, 1.7)
let slope_line1 = (-1)*(vin - 0.8) + 1.7

* Reference line 2: slope -1 through (1.1, 0.1)
let slope_line2 = (-1)*(vin - 1.1) + 0.1
meas dc VM FIND v(in) WHEN v(inter)=v(in) cross=1

* Plot transfer curve + both reference lines
plot vout vs vin slope_line1 vs vin slope_line2 vs vin\
     title "Inverter Transfer Curve with -1 Slope Reference Lines"
.endc
```

**Ques2-1.cir code for transient anaylsis**

```
* SkyWater PDK
* Minimum size CMOS inverter
* VDD = 1.8 V, Lmin = 0.15um, Wn(min) = 0.42um

.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt

*the voltage sources:
Vdd vdd gnd DC 1.8
V1 in gnd pulse(0 1.8 0p 20p 10p 1n 2n)

Xnot1 in vdd gnd inter not2
Xnot2 inter vdd gnd load not1

.subckt not1 a vdd vss z
xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w=2 as=0.6 ad=0.6 ps=4.6 pd=4.6
xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=0.42 as=0.126 ad=0.126 ps=1.44 pd=1
C0 z a 0.2f
C1 a vdd 0.2f
```

```
C2 z vdd 0.2f
C3 z vss 0.4f
C4 a vss 0.6f
C5 vdd vss 1f
.ends

.subckt not2 a vdd vss z
xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w=4 as=1.2 ad=1.2 ps=8.6 pd=8.6
xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=0.84 as=0.252 ad=0.252 ps=2.28 pd=2
C0 z a 0.4f
C1 a vdd 0.4f
C2 z vdd 0.4f
C3 z vss 0.8f
C4 a vss 1f
C5 vdd vss 2f

.ends

* simulation command:
.tran 1ps 10ns 0 10p

.measure tran trise TRIG v(load) VAL={0.2*1.8} RISE=1 TARG v(load) VAL={0.8*1.8} RISE
.measure tran tfall TRIG v(load) VAL={0.8*1.8} FALL=1 TARG v(load) VAL={0.2*1.8} FALL
.measure tran tpHL  TRIG v(in)   VAL={0.5*1.8} FALL=1 TARG v(load) VAL={0.5*1.8} FALL
.measure tran tpLH  TRIG v(in)   VAL={0.5*1.8} RISE=1 TARG v(load) VAL={0.5*1.8} RISE
.measure tran tp_avg PARAM='(tpHL + tpLH)/2'

.control
run
plot in load

.endc
```

**Ques2-2.cir code for dc sweep**

```
* SkyWater PDK
* Minimum size CMOS inverter
* VDD = 1.8 V, Lmin = 0.15um, Wn(min) = 0.42um

.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt

*the voltage sources:
Vdd vdd gnd DC 1.8
V1 in gnd pulse(0 1.8 0p 20p 10p 1n 2n)

Xnot1 in vdd gnd inter not2
Xnot2 inter vdd gnd load not1
```

```
.subckt not1 a vdd vss z
xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w=2 as=0.6 ad=0.6 ps=4.6 pd=4.6
xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=0.42 as=0.126 ad=0.126 ps=1.44 pd=1
C0 z a 0.2f
C1 a vdd 0.2f
C2 z vdd 0.2f
C3 z vss 0.4f
C4 a vss 0.6f
C5 vdd vss 1f
.ends

.subckt not2 a vdd vss z
xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w=4 as=1.2 ad=1.2 ps=8.6 pd=8.6
xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=0.84 as=0.252 ad=0.252 ps=2.28 pd=2
C0 z a 0.4f
C1 a vdd 0.4f
C2 z vdd 0.4f
C3 z vss 0.8f
C4 a vss 1f
C5 vdd vss 2f

.ends

* simulation command:
.dc V1 0 1.8 0.001


.control
run
let vin = v(in)
let vout = v(inter)

* Reference line 1: slope -1 through (0.8, 1.7)
let slope_line1 = (-1)*(vin - 0.8) + 1.7

* Reference line 2: slope -1 through (1.1, 0.1)
let slope_line2 = (-1)*(vin - 1.1) + 0.1
meas dc VM FIND v(in) WHEN v(inter)=v(in) cross=1

* Plot transfer curve + both reference lines
plot vout vs vin slope_line1 vs vin slope_line2 vs vin\
     title "Inverter Transfer Curve with -1 Slope Reference Lines"
.endc
```

# 3 Results

## 3.1 Transient Response

Figure 1,2 shows the input and output waveforms of the inverters INVX1 and INVX2. The measured rise and fall times are tabulated and shown in terminal.

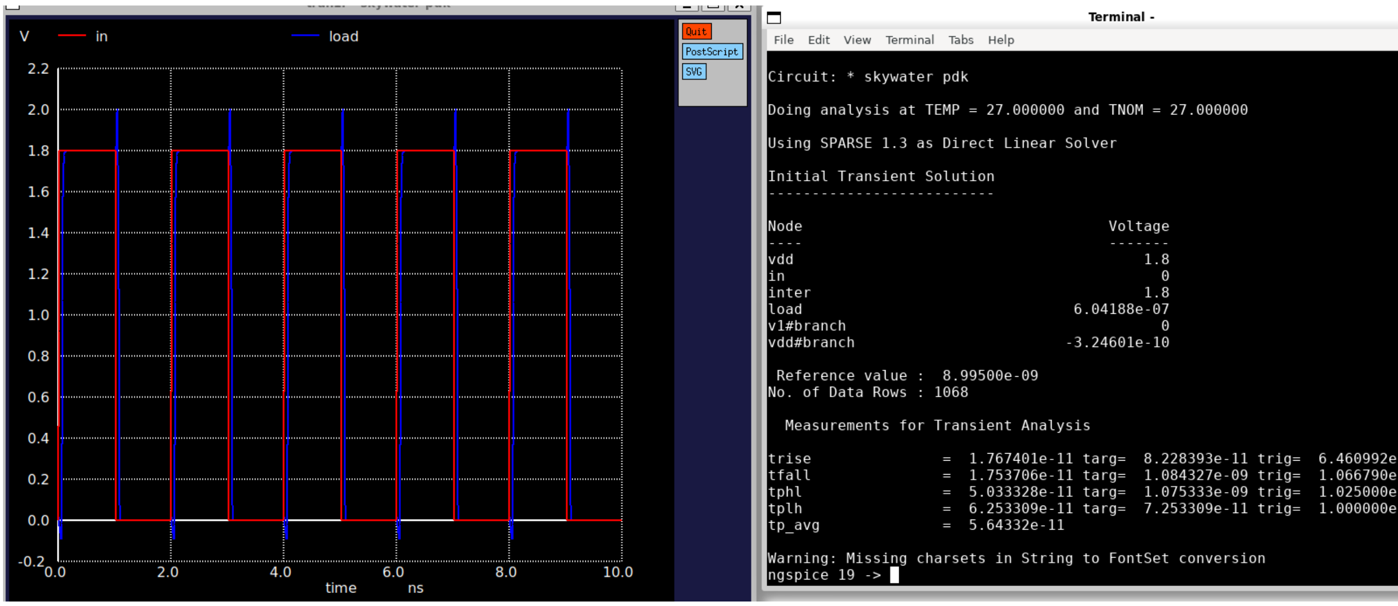


Figure 1: Transient simulation of inverter1 (Input vs. Output).

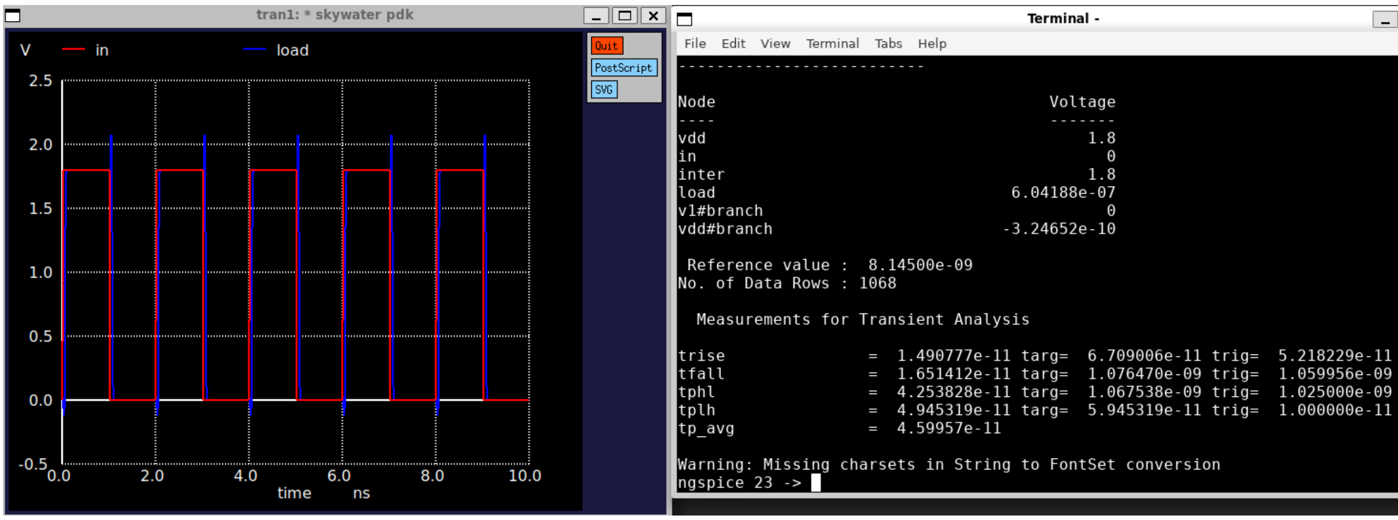


Figure 2: Transient simulation of inverter2 (Input vs. Output).

| Parameter | Value |
|---|---|
| $t_{rise}$ | 17.67 ps |
| $t_{fall}$ | 17.53 ps |
| $t_{prop}$ | 56.43 ps |

Table 1: Measured timing parameters of INV1

| Parameter | Value |
|---|---|
| $t_{rise}$ | 14.9 ps |
| $t_{fall}$ | 16.51 ps |
| $t_{prop}$ | 46 ps |

Table 2: Measured timing parameters of INV2

## 3.2 DC Transfer Characteristic

Figure 3, 4 shows the VTC of the inverters. The switching threshold and noise margins are indicated.

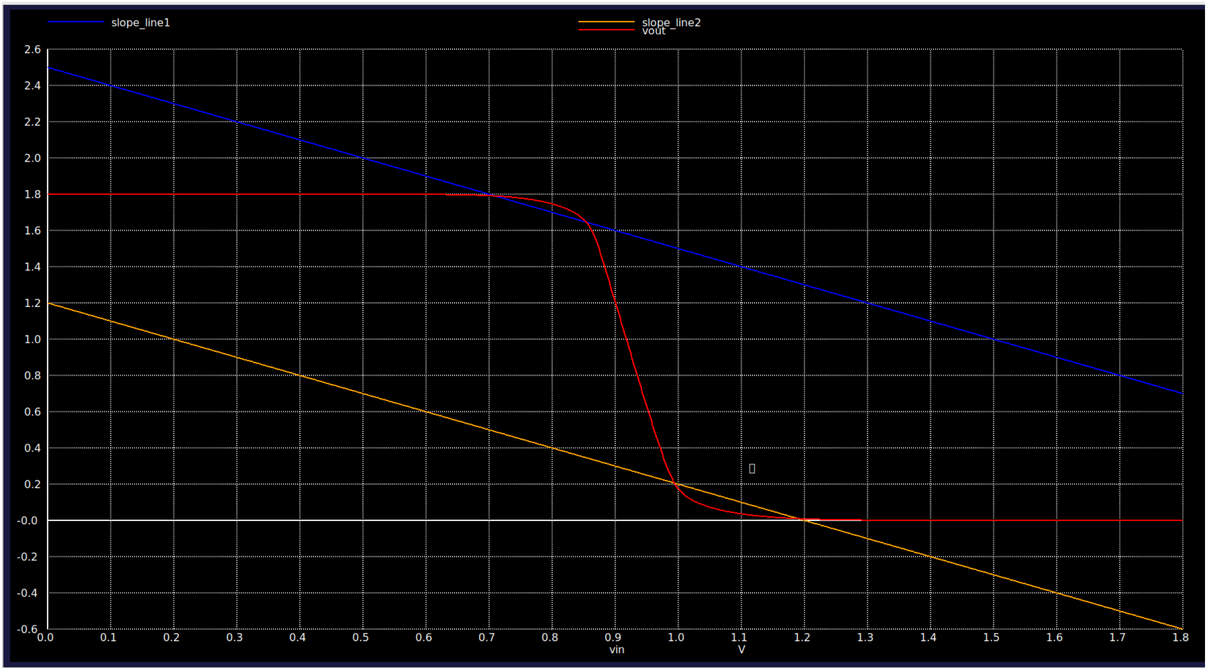


Figure 3: DC Transfer characteristic of inverter1 (Vout vs Vin).

| Parameter | Value |
|---|---|
| $V_M$ | 0.9238 V |
| $V_{IL}$ | 0.20687 V |
| $V_{IH}$ | 1.65263 V |
| $NM_L$ | 0.20687 V |
| $NM_H$ | 0.14737 V |

Table 3: Static parameters of the inverter1

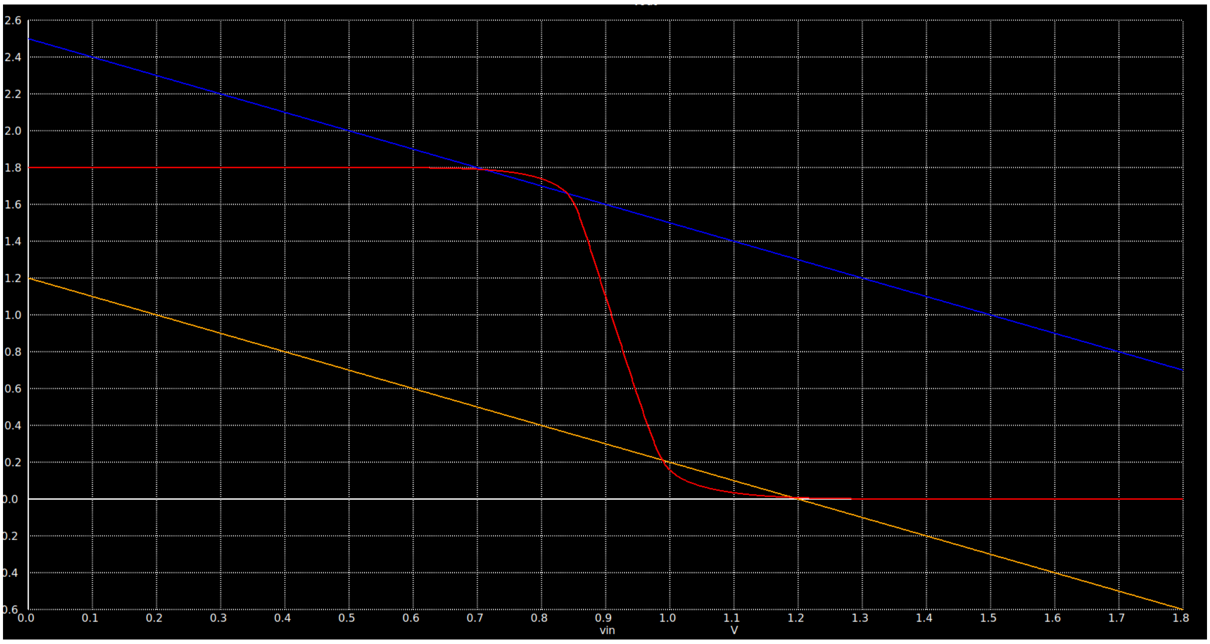


Figure 4: DC Transfer characteristic of inverter2 (Vout vs Vin).

| Parameter | Value |
|---|---|
| $V_M$ | 0.91625 V |
| $V_{IL}$ | 0.2112 V |
| $V_{IH}$ | 1.6605 V |
| $NM_L$ | 0.2112 V |
| $NM_H$ | 0.1395 V |

Table 4: Static parameters of the inverter2

# 4 Discussion

- The switching threshold $V_M$ was observed close to 0.9 V, which is expected for a balanced inverter.
- Rise and fall times were not identical, due to $W_p : W_n$ sizing and parasitics. Rise and fall times were less for INVX2 as it should be.
- Noise margins confirm robustness to input noise up to $\sim$0.2 V.

# 5 Conclusion

A minimum-size CMOS inverter was simulated using the Sky130 PDK. Both transient and static analyses were performed. The inverter exhibits expected behavior with adequate noise margins and propagation delay suitable for low-power digital applications.