EE671 – VLSI Design

Assignment 3: 16-bit Kogge-Stone Adder – Synthesis Report

Group: 28
Course: EE671 – VLSI DESIGN
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Abstract

This report documents the design, verification (pre- and post-synthesis), synthesis results, and the RTL/netlist outputs for a 16-bit Kogge–Stone (KS) adder. The design follows the lab instructions for a register-input, registered-output adder with clocked input registers and clocked output registers. Screenshots and synthesis metrics from Cadence Genus are included.

1 Introduction

The objective of this assignment was to design a 16-bit Kogge–Stone tree adder, verify it using a testbench, and synthesize the design using Cadence Genus to produce the RTL gate-level netlist and reports. The module interface is:

- **Inputs:** A[15:0], B[15:0], CIN, CLK, RST_N (active low)
- **Outputs:** SUM[15:0], COUT

2 Design Description

1. The adder is implemented as a Kogge–Stone parallel-prefix carry network for fast carry propagation.
2. Inputs A, B, and CIN are sampled into input registers on the rising edge of `CLK`. The adder computes SUM and COUT combinationally and these are registered at the output on the next rising edge of `CLK`.
3. All modules and top-level files are written in Verilog with appropriate comments and indentation.

3 Pre-synthesis Verification

3.1 Simulation Setup

- Simulator: Icarus (iverilog) / gtkwave for waveform inspection.
- Testbench: Stimulates multiple vectors including carry propagation edge cases (all-0s, all-1s, alternating patterns, random vectors).
- Clock: 100 MHz (as per assignment).

3.2 Pre-synthesis Waveform

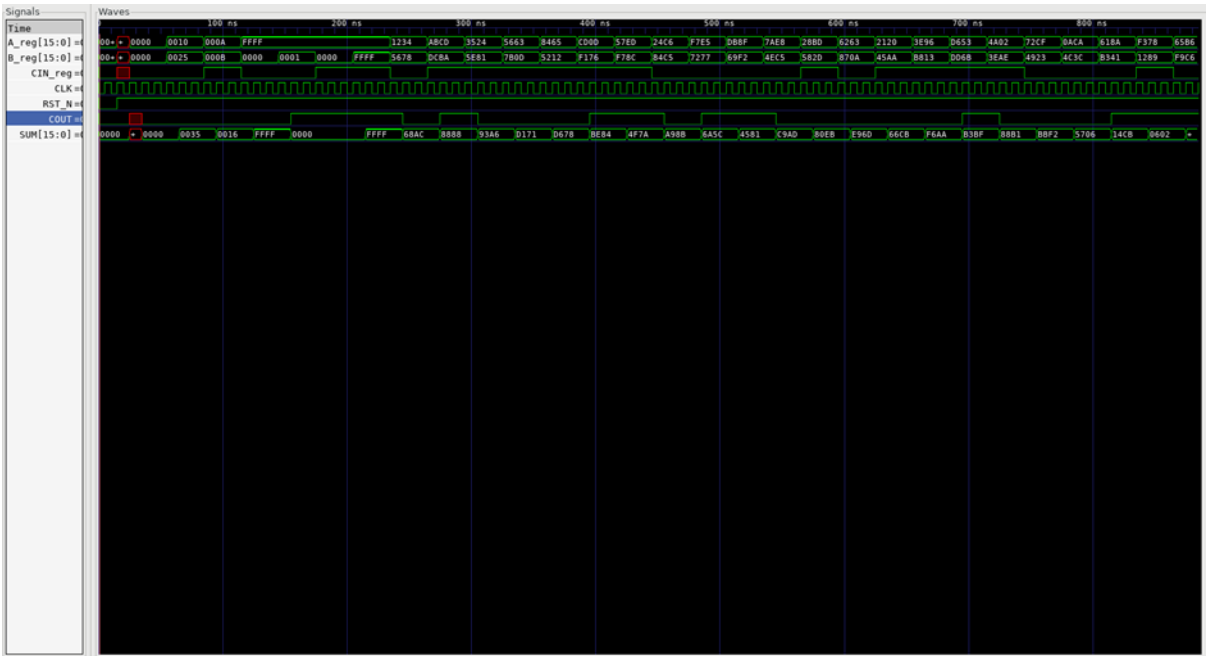

Figure 1: Pre-synthesis simulation waveform (replace `figures/pre_synthesis_waveform.png` with your `waveforms.vcd` screenshot).

4 Synthesis

Synthesis was performed with Cadence Genus using provided `synthesis.tcl` and constraints (`constraints.sdc`). Target clock: 100 MHz.

4.1 Area and Summary Report

Open

area.rpt
~/Synthesis_Examples/KS_ADDDER/Synthesis

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.19-s055_1
  Generated on:           Oct 06 2025  01:40:18 am
  Module:                 kogge_stone_adder_16bit
  Technology libraries:   tcbn65gplustc_ccs 200
                          physical_cells
  Operating conditions:   NCCOM
  Interconnect mode:      global
  Area mode:              physical library
============================================================

        Instance        Module  Cell Count  Cell Area  Net Area   Total Area
-------------------------------------------------------------------------------
kogge_stone_adder_16bit                 96    556.200   154.485      710.685
```

Figure 2: Screenshot of the area report after synthesis

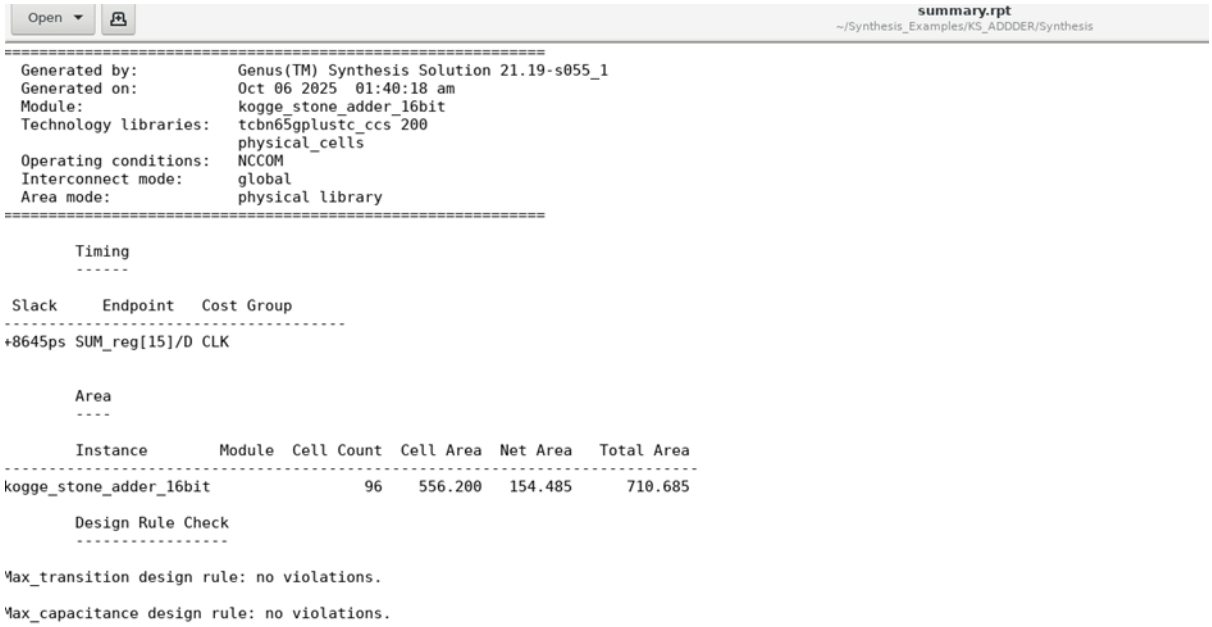

Figure 3: Screenshot of the summary report after synthesis

4.2 Cell Count Summary

Table 1: Cell summary

Description	Count (example)
Number of combinational cells	46
Number of sequential cells (flip-flops)	50
Total number of cells	96

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.19-s055_1
  Generated on:           Oct 06 2025  01:40:18 am
  Module:                 kogge_stone_adder_16bit
  Technology libraries:   tcbn65gplustc_ccs 200
                          physical_cells
  Operating conditions:   NCCOM
  Interconnect mode:      global
  Area mode:              physical library
============================================================


  Gate    Instances   Area          Library
-------------------------------------------------
AO22D0           15   43.200    tcbn65gplustc_ccs
CKXOR2D1         15   54.000    tcbn65gplustc_ccs
DFCNQD1          50  396.000    tcbn65gplustc_ccs
FA1D0             1    9.000    tcbn65gplustc_ccs
XOR2D1           15   54.000    tcbn65gplustc_ccs
-------------------------------------------------
total            96  556.200


     Type      Instances   Area  Area %
-----------------------------------------
sequential            50 396.000   71.2
logic                 46 160.200   28.8
physical_cells         0   0.000    0.0
-----------------------------------------
total                 96 556.200  100.0
```

Figure 4: Results

5 Post-synthesis Verification

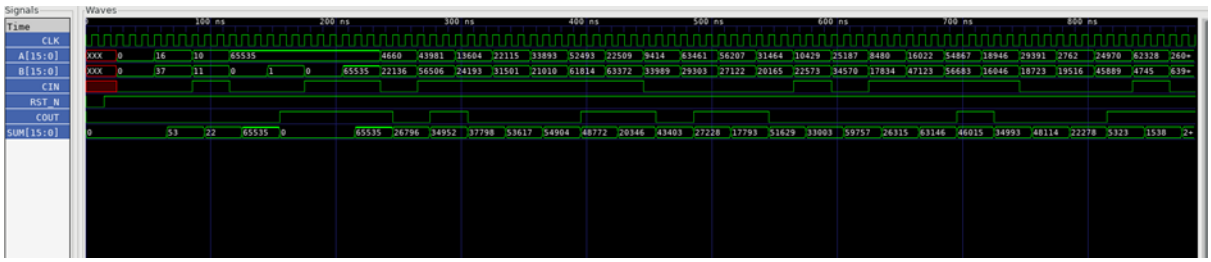

Figure 5: Post-synthesis (gate-level) simulation waveform

6 Files Submitted (ZIP)

1. `KSadder.v` – Top-level Verilog source .
2. `KSadder_TB.v` – Testbench file
3. `KS_adder_netlist.v` – Post-synthesis RTL netlist (from Genus).

7 Conclusion

The 16-bit Kogge–Stone adder was implemented, verified (pre- and post-synthesis), and synthesized. Post-synthesis functional verification confirms equivalence with pre-synthesis behavior (replace with formal equivalence / comparison summary if available). The RTL netlist and synthesis reports are included in the submission ZIP.