EE671: VLSI Design
Assignment No. 2

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Q1) Minimum Size CMOS Inverter Design

Layout

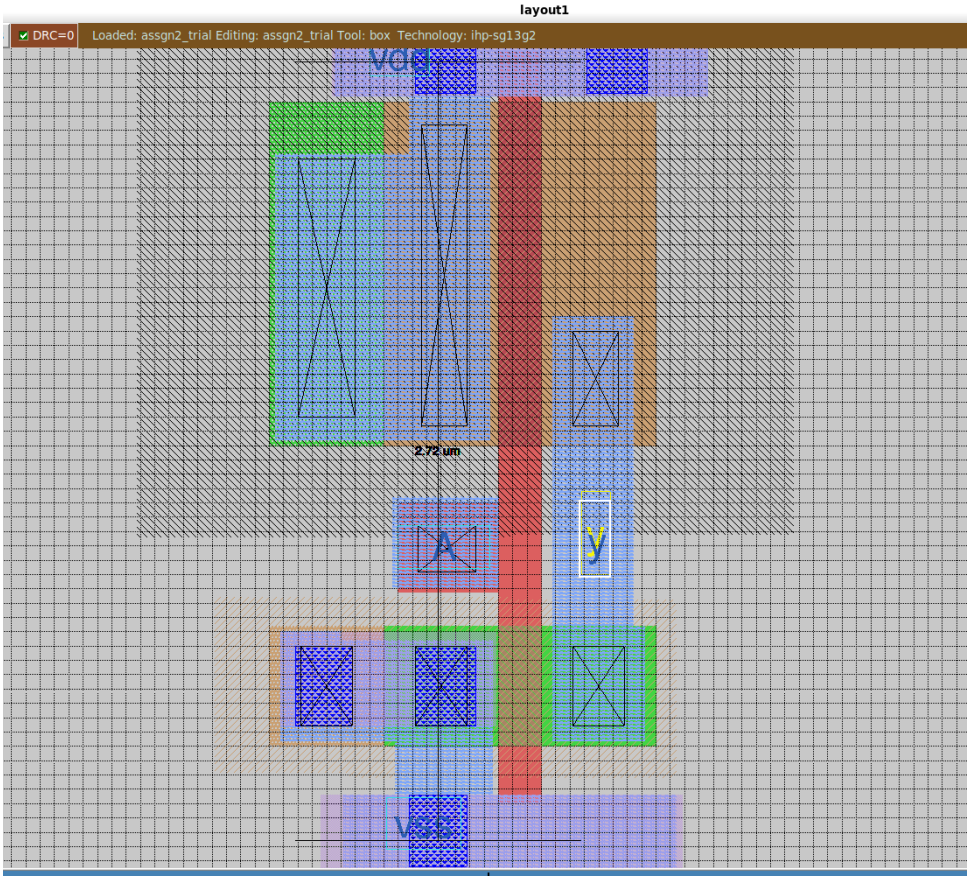

Figure 1: Layout of Strength 1 Inverter

The layout has a total width of 2.72μm, as shown in the figure. Please not that in the top left corner DRC check is 0.

Layout Versus Schematic

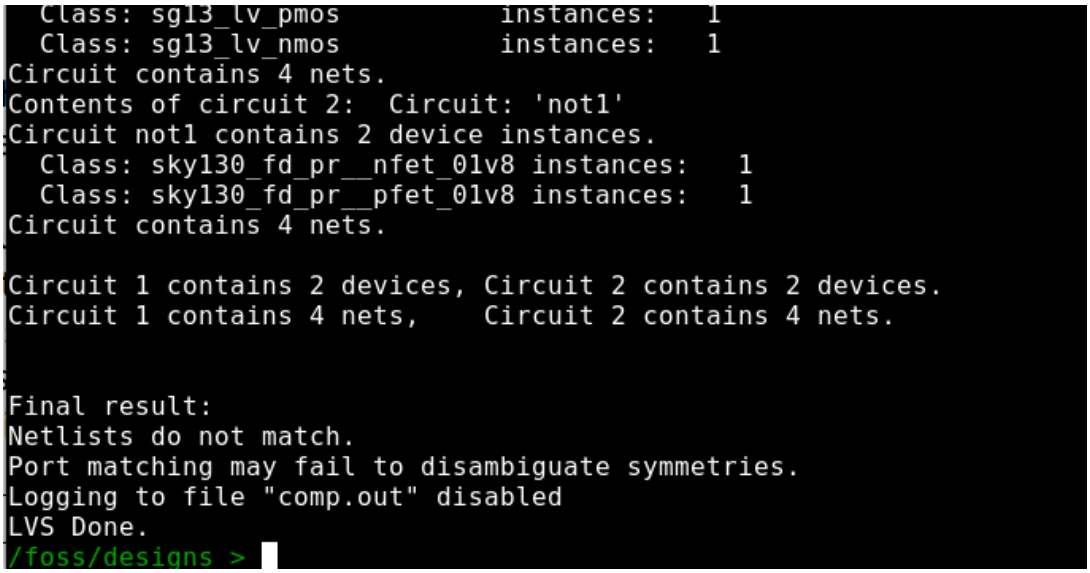

Figure 2: LVS Check of Strength 1 Inverter

The LVS check confirmed that the circuits arent match uniquely due to the difference in area and perimeter otherwise rest of the things were fine.

Simulation Results

I got the pex file which contain the subckt but it is not giving result in spice

Q2) Strength-2 Inverter Design (INVX2)

Layout

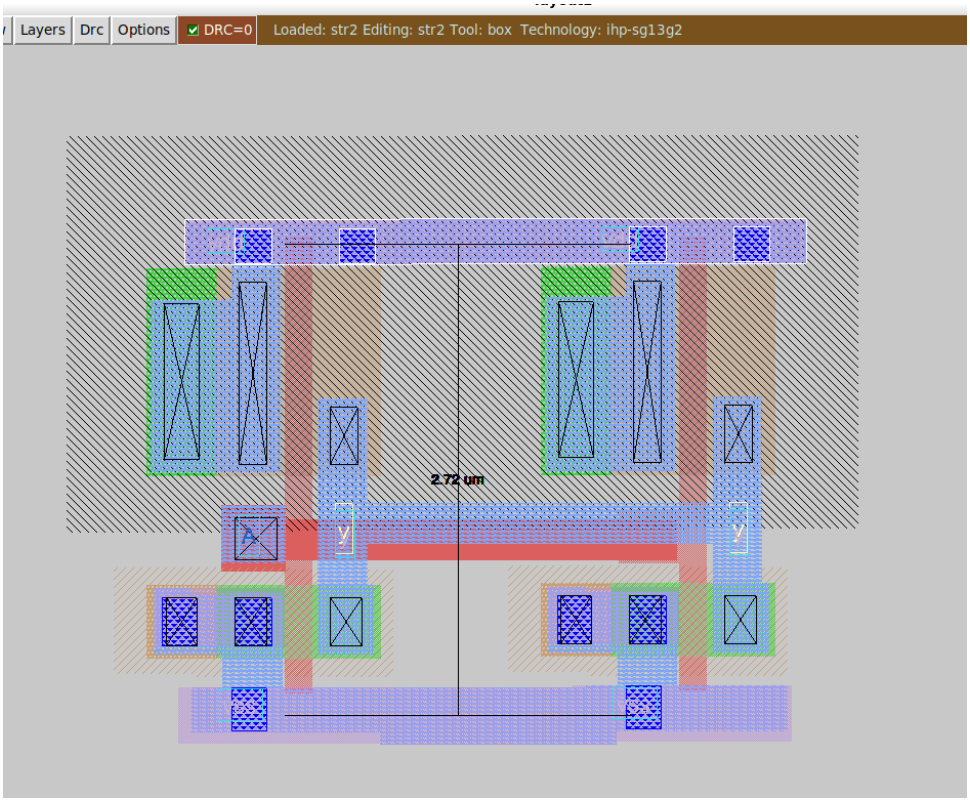

Figure 3: Layout of Strength 2 Inverter

The layout has a total width of 2.72μm, as shown in the figure. Please not that in the top left corner DRC check is 0.

The DRC check was performed, and no errors were found.

Layout Versus Schematic

```
  4 = 2                                  |
                                         |
Instance: sg13_lv_pmos:1                 |Instance: sky130_fd_pr__pfet_01v
  1 = 2                                  |  (1,3) = (2,2)
  2 = 2                                  |  2 = 2
  3 = 2                                  |  4 = 2
  4 = 2                                  |
-----------------------------------------------------------------------------
Netlists do not match.
Port matching may fail to disambiguate symmetries.

Subcircuit pins:
Circuit 1: assgn2_trial                  |Circuit 2: not1
-----------------------------------------|-------------------------------
vdd                                      |vdd
vss                                      |vss
a_n10_n92#                               |A **Mismatch**
y                                        |y
-----------------------------------------------------------------------------
Cell pin lists for assgn2_trial and not1 altered to match.
Device classes assgn2_trial and not1 are equivalent.
```

```
Logging to file "comp.out" enabled

Contents of circuit 1:  Circuit: 'assgn2_trial'
Circuit assgn2_trial contains 2 device instances.
  Class: sg13_lv_pmos          instances:   1
  Class: sg13_lv_nmos          instances:   1
Circuit contains 4 nets.
Contents of circuit 2:  Circuit: 'not1'
Circuit not1 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   1
  Class: sky130_fd_pr__pfet_01v8 instances:   1
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 de
Circuit 1 contains 4 nets,    Circuit 2 contains 4 ne


Final result:
Top level cell failed pin matching.

Logging to file "comp.out" disabled
LVS Done.
/foss/designs >
```

Figure 4: LVS Check of Strength 2 Inverter

The LVS check confirmed that input port is not matching.

Simulation Results

I got the pex file which contain the subckt but it is not giving result in spice
I have attached pex files and layout.spice files