Standard Cell Library Characterization and Design

Team Number: 28

September 13, 2025

Contents

Project Overview

Introduction

This project involves the characterization and design of three standard cells in the standard cell library, including Spice Netlist, layout, LEF, and Verilog views. The goal is to ensure all views are consistent and functional, with performance metrics matching the provided design criteria. The elements that we have designed and characterized include:

- Inverter of Strength 1
- AND gate (3-input AND)
- D-Flip Flop of Strength 1 (Negative Edge triggered)

Project Objectives

- Design NGSpice circuit for each cell with the same rise/fall time as inverter 1x.
- Draw the layout using Magic and ensure zero DRC errors and LVS pass.
- Extract LEF, PEX netlist and perform timing, power, and input capacitance characterizations.
- Create HDL functional definition and validate it using the Icarus Verilog tool.

Chapter 1

Cell 1: INVERTER

1.1 Circuit Diagram

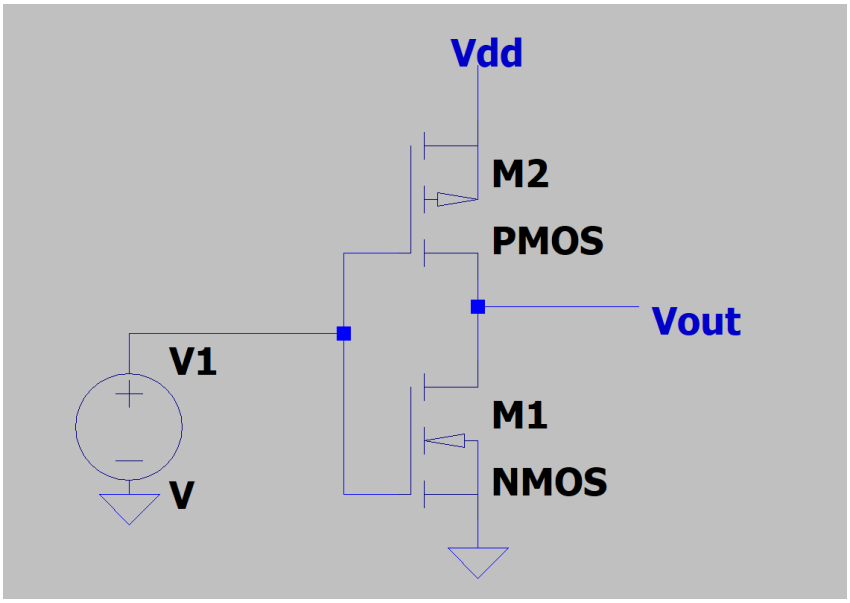

Figure 1.1: Circuit Diagram of Inverter with MOSFETs.

MOSFET Dimensions

Table 1.1: MOSFET Width and Length for Inverter

Device	Width (W)	Length (L)
M1 (NMOS)	0.42 μm	0.15 μm
M2 (PMOS)	1.27 μm	0.15 μm

1.2 Layout

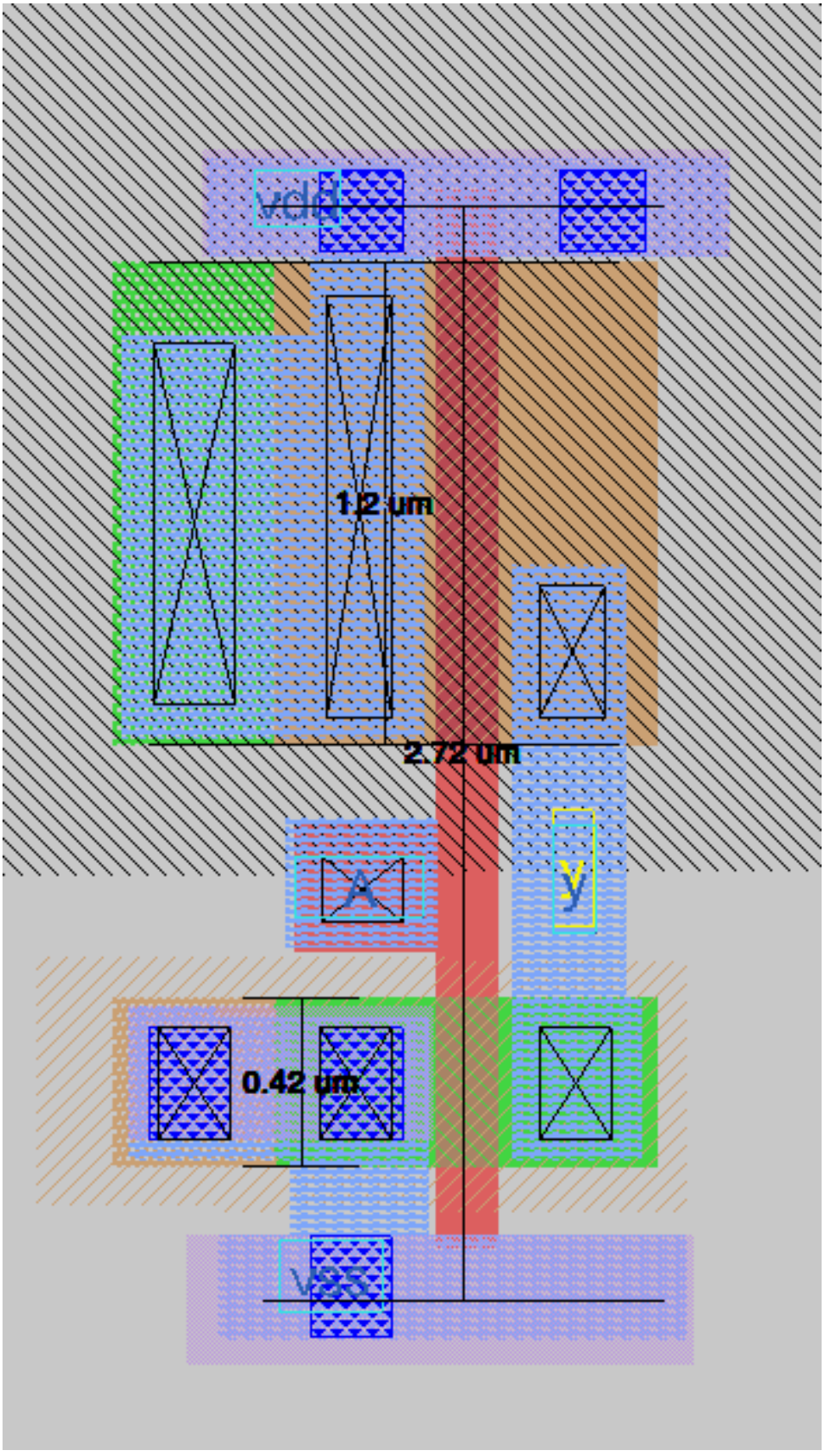

Figure 1.2: Inverter Layout Width X Height(2.72μm)

1.3 PEX Netlist

```
* NGSPICE file created from assgn2_ques1.ext - technology: ihp-sg13g2

.subckt assgn2_ques1 A vdd vss y
X0 y A vss vss sg13_lv_nmos ad=0.11159p pd=0.93333u as=0.6315p ps=4.78u
    w=0.42u l=0.15u
**devattr s=6720,328 d=6720,328
X1 y A vdd vdd sg13_lv_pmos ad=0.31881p pd=2.66667u as=1.118p ps=6.42u
   w=1.2u l=0.15u
**devattr s=19200,640 d=19200,640
C0 y A 0.08016f
C1 vdd A 0.17101f
C2 vdd y 0.12408f
C3 y vss 0.21326f
C4 A vss 0.36721f
C5 vdd vss 0.20526f
.ends
```

Figure 1.3: PEX Netlist of the Inverter

1.4 DRC and LVS Results

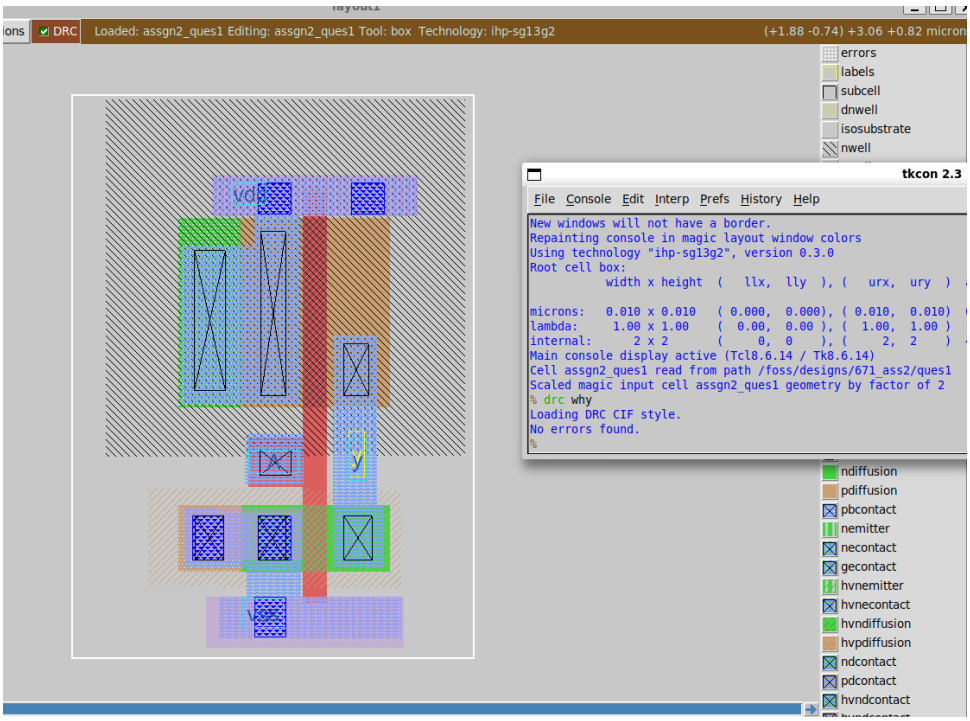

Figure 1.4: DRC Clean Screenshot for Inverter

```
Circuit sky130_fd_pr__nfet_01v8 contains no devices.
Circuit sky130_fd_pr__pfet_01v8 contains no devices.

Contents of circuit 1:  Circuit: 'assgn2_ques1'
Circuit assgn2_ques1 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   1
  Class: sky130_fd_pr__pfet_01v8 instances:   1
Circuit contains 4 nets.
Contents of circuit 2:  Circuit: 'not1'
Circuit not1 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   1
  Class: sky130_fd_pr__pfet_01v8 instances:   1
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets,    Circuit 2 contains 4 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
/foss/designs >
```

Figure 1.5: LVS Clean Screenshot for Inverter

1.5 Simulation Results

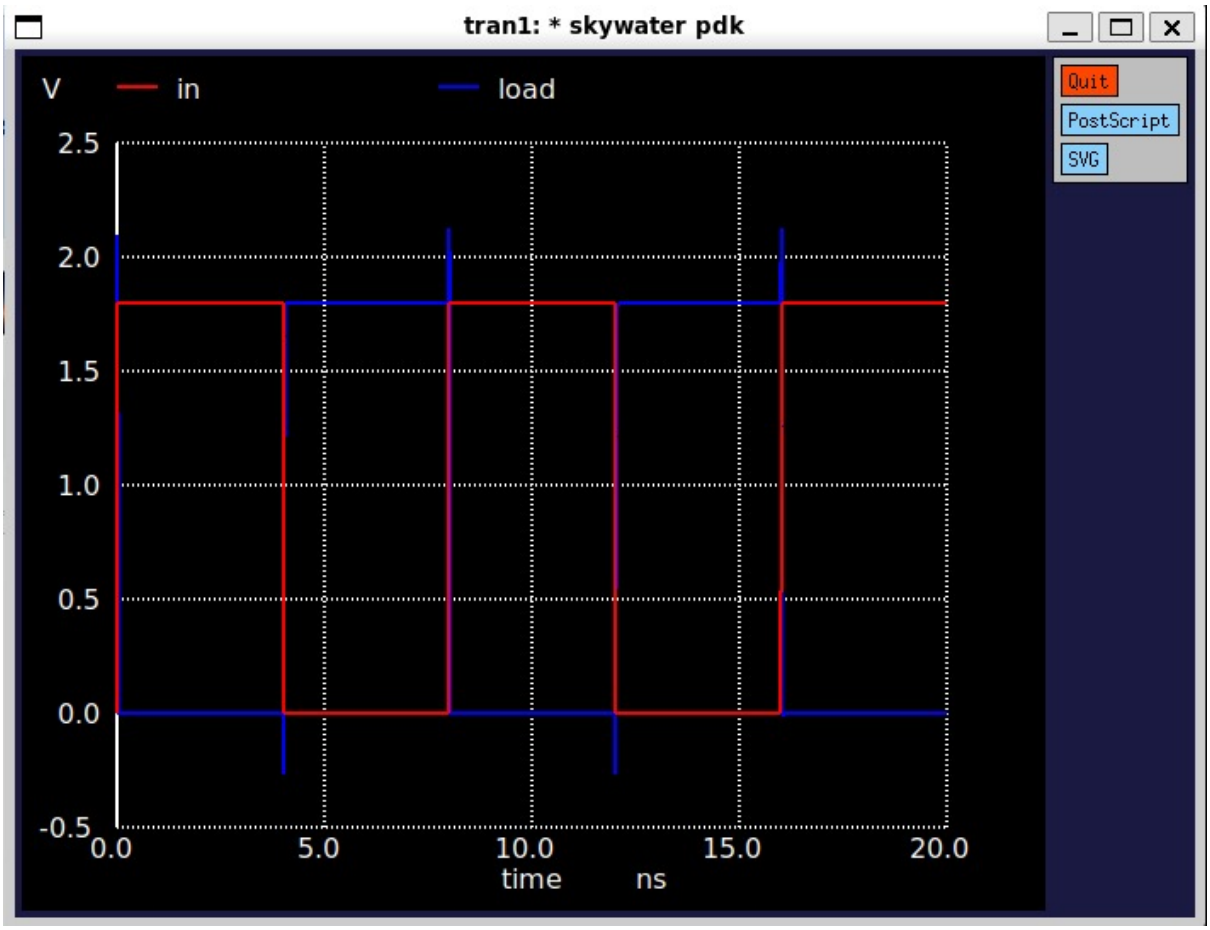

Figure 1.6: 10ps input slew and cap 0.05fF

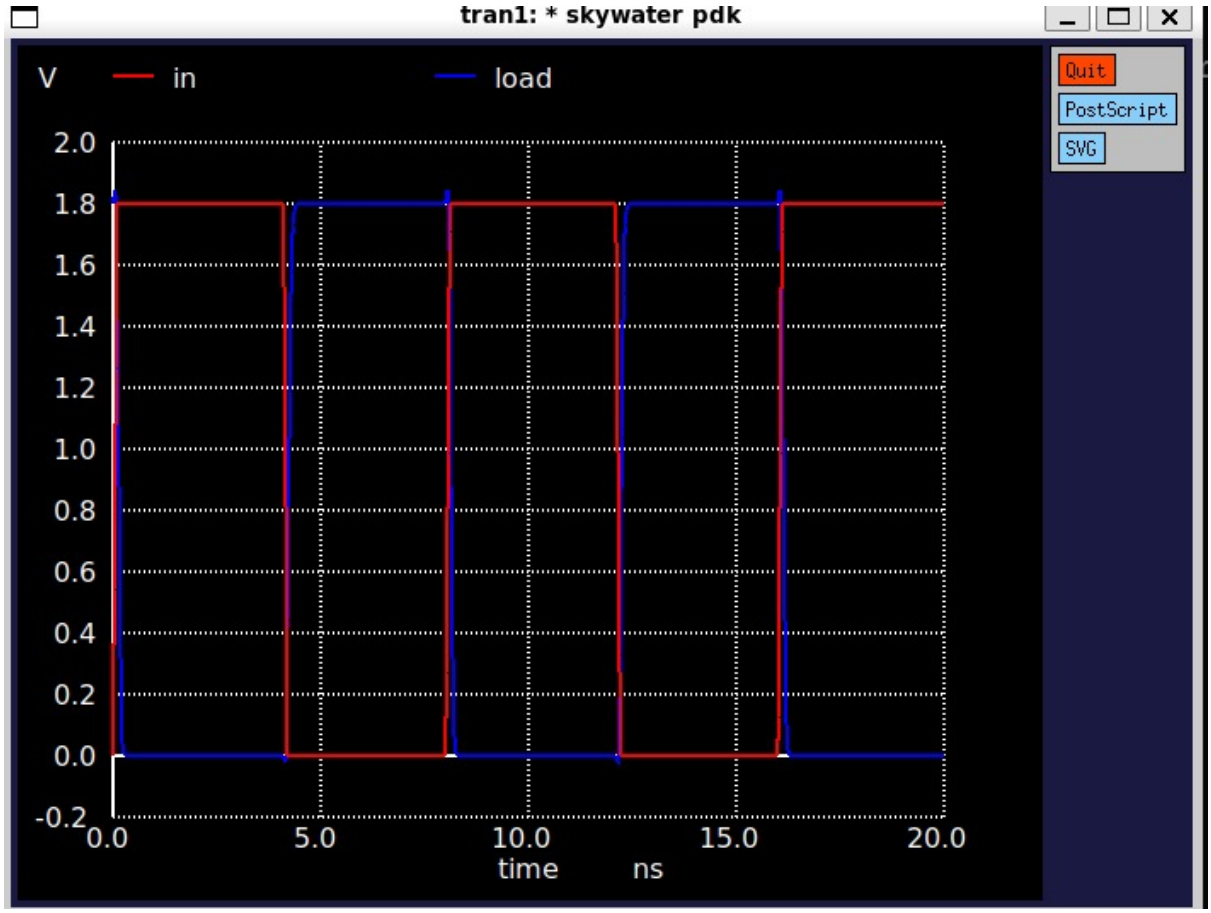

Figure 1.7: 100ps input slew and cap 0.05fF

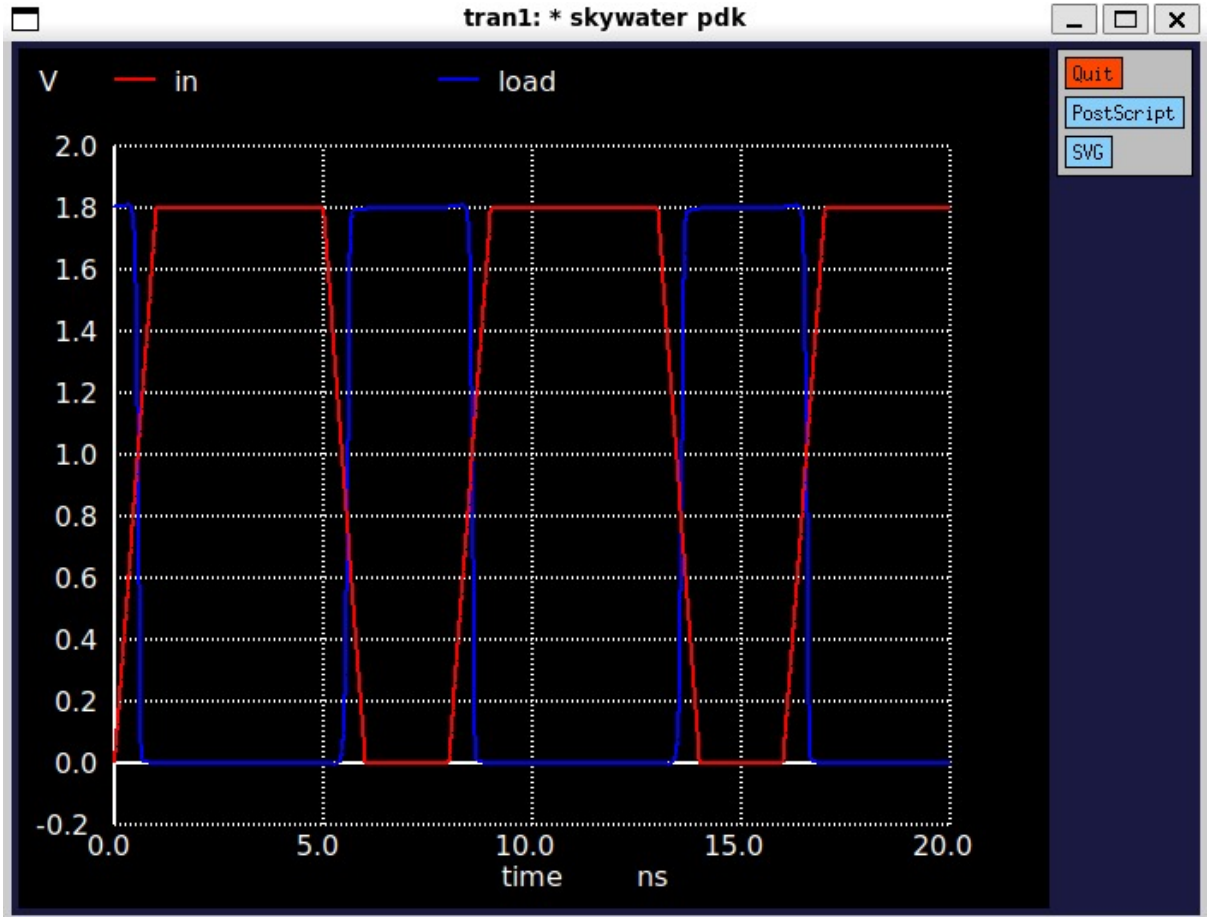

Figure 1.8: 1000ps input slew and cap 0.05fF

1.6 Timing and Power Table

1.6.1 Input Pin Capacitances

Table 1.2: Input Pin Capacitances

Pin	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
A	0.948e-03	0.661e-03	0.804e-03

1.6.2 Transition Time Table

Table 1.3: Output Rise Transitions (ns) — Input Slew vs Output Capacitance

Input Slew	0.5 fF	10 fF	100 fF
10 ps	12.9e-3	23.9e-3	89.5e-3
100 ps	70e-3	70.47e-3	186.8e-3
1000 ps	623.5e-3	623.5e-3	634.5e-3

Table 1.4: Output Fall Transitions (ns) — Input Slew vs Output Capacitance

Input Slew	0.5 fF	10 fF	100 fF
10 ps	12.8e-3	20.2e-3	79.4e-3
100 ps	71.6e-3	71.7e-3	173.8e-3
1000 ps	640.3e-3	640.5e-3	647e-3

1.6.3 Propagation Delay Time Table

Table 1.5: Cell Rise Delay (ns) — Input Slew vs Output Capacitance

Input Slew	0.5 fF	10 fF	100 fF
10 ps	17.04e-3	32.2e-3	69e-3
100 ps	64.03e-3	83.4e-3	212.2e-3
1000 ps	499.7e-3	520.06e-3	725.88e-3

Table 1.6: Cell Fall Delay (ns) — Input Slew vs Output Capacitance

Input Slew	0.5 fF	10 fF	100 fF
10 ps	13.9e-3	30.8e-3	73.4e-3
100 ps	54.1e-3	76.3e-3	218.08e-3
1000 ps	430.6e-3	453.3e-3	680.8e-3

1.6.4 Static Power Table

Table 1.7: Static Power

Condition	Power (nW)
0	0.92
1	2.2

1.6.5 Dynamic Power Table

Table 1.8: Rise Power (nW) — Input Slew vs Output Capacitance

Input Slew	0.5 fF	10 fF	100 fF
10 ps	284.1	2240.8	2825
100 ps	10073.7	9983	10257
1000 ps	82989	82958	82891.5

Table 1.9: Fall Power (nW) — Input Slew vs Output Capacitance

Input Slew	0.5 fF	10 fF	100 fF
10 ps	339.9	518.4	115.03
100 ps	252.74	378.2	366
1000 ps	240.12	370.2	280.4

Chapter 2

Cell 2: AND (3 input AND)

2.1 Circuit Diagram

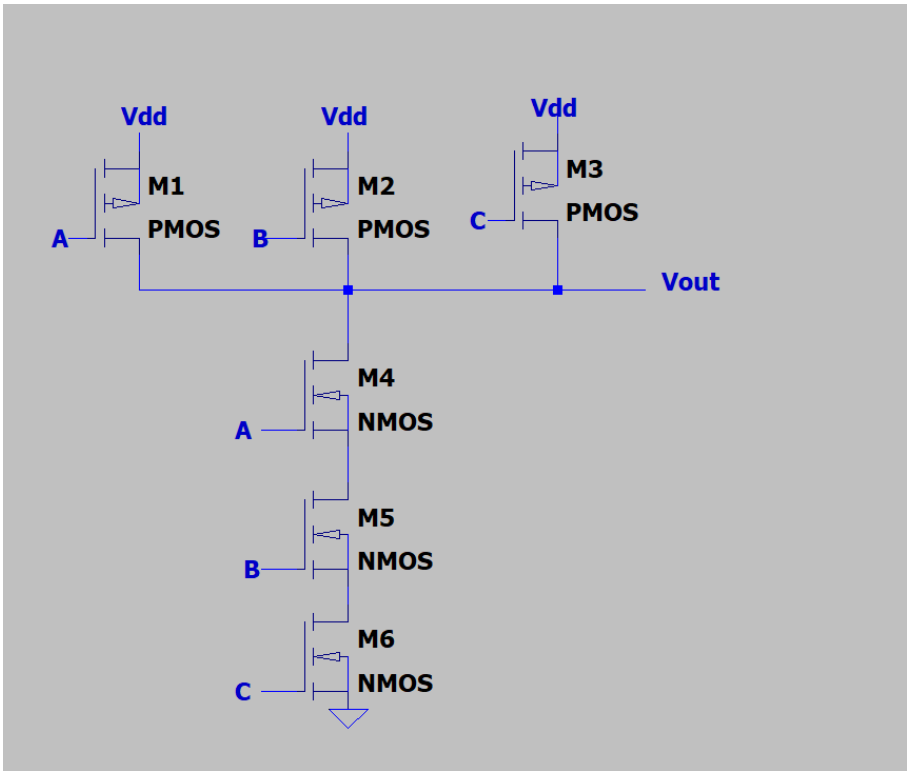

Figure 2.1: Circuit Diagram of AND-OR Circuit with MOSFETs.

2.2 Stick Diagram

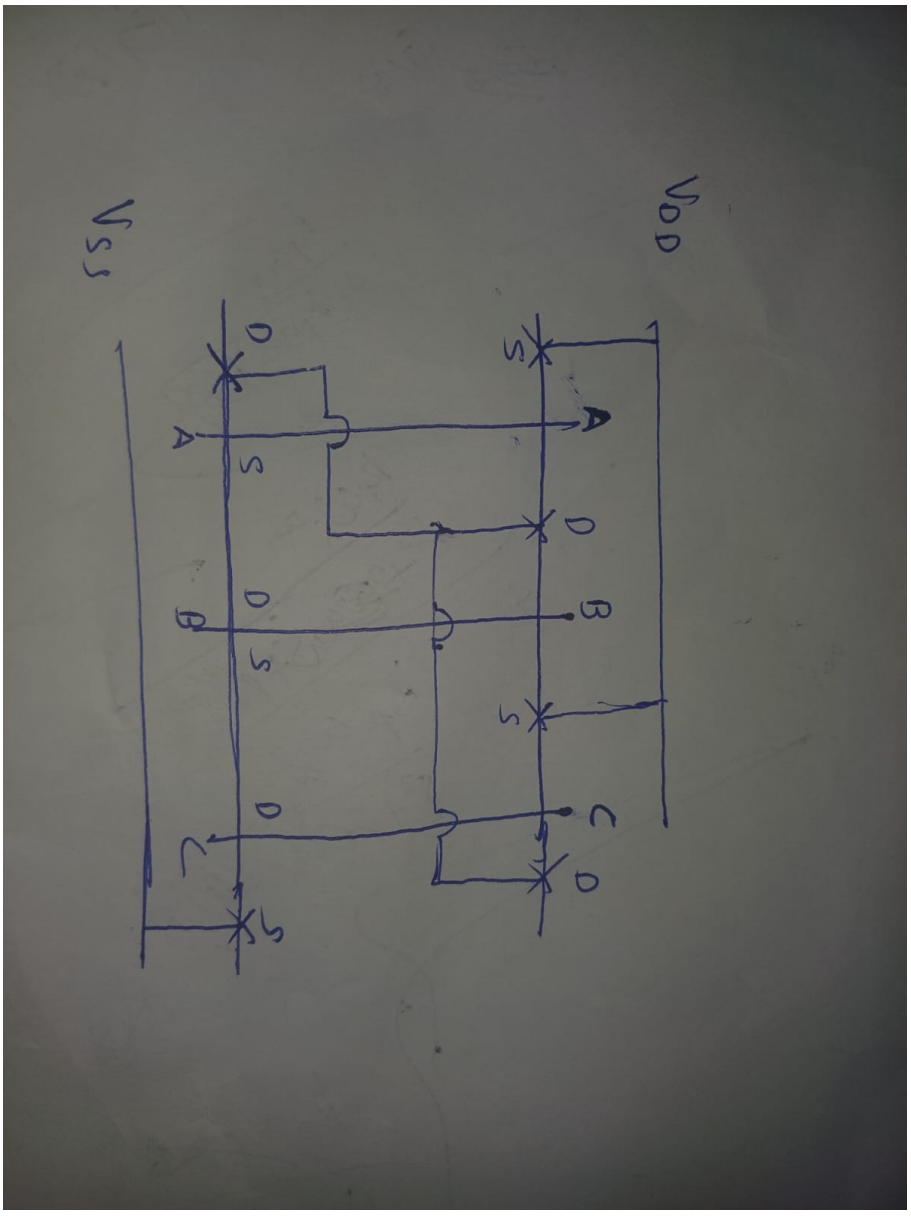

Figure 2.2: And-Or Stick Diagram for the Layout

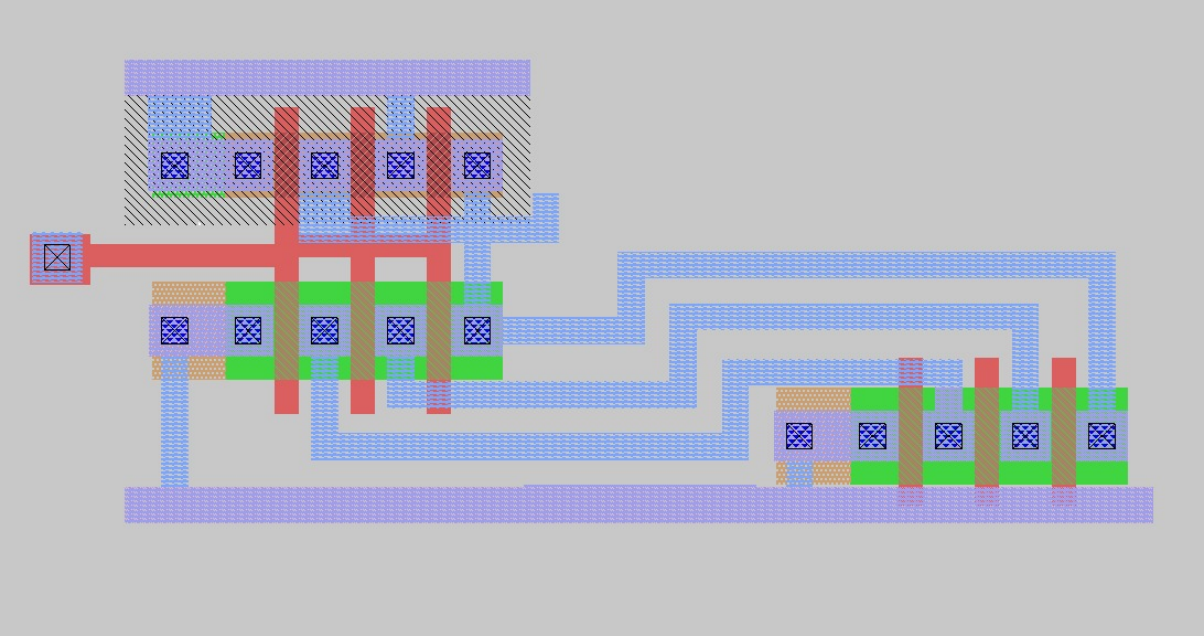

Figure 2.3: layout and3

MOSFET Widths and Lengths

Table 2.1: MOSFET Width and Length for And-Or

MOSFET	Width (W)	Length (L)
M1 (PMOS)	1.27 μm	0.15 μm
M2 (PMOS)	1.27 μm	0.15 μm
M3 (PMOS)	1.27 μm	0.15 μm
M4 (NMOS)	1.26 μm	0.15 μm
M5 (NMOS)	1.26 μm	0.15 μm
M6 (NMOS)	1.26 μm	0.15 μm
M7 (NMOS)	0.42 μm	0.15 μm
M8 (PMOS)	1.27 μm	0.15 μm

2.3 Layout

2.4 PEX Netlist (excerpt)

```
NGSpice PEX netlist excerpt placeholder.
```

Figure 2.4: PEX Netlist Excerpt

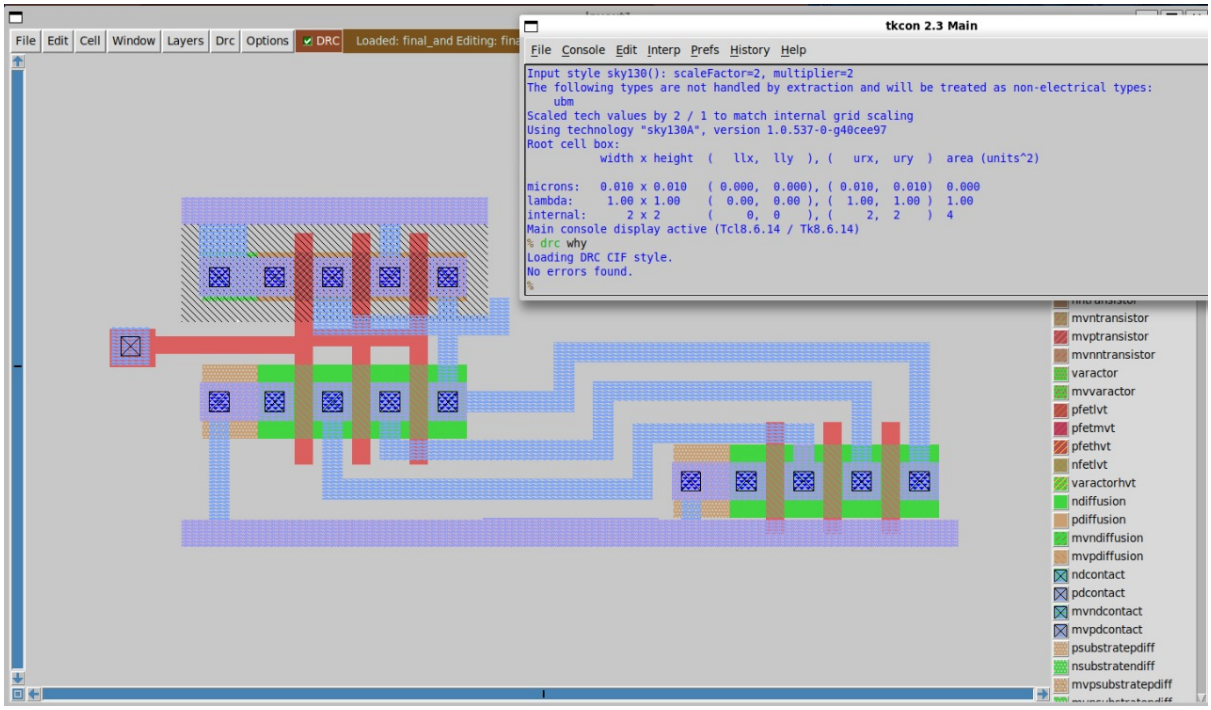

Figure 2.5: DRC clean

2.5 DRC and LVS Results

2.6 Simulations (Explanations and Graphs)

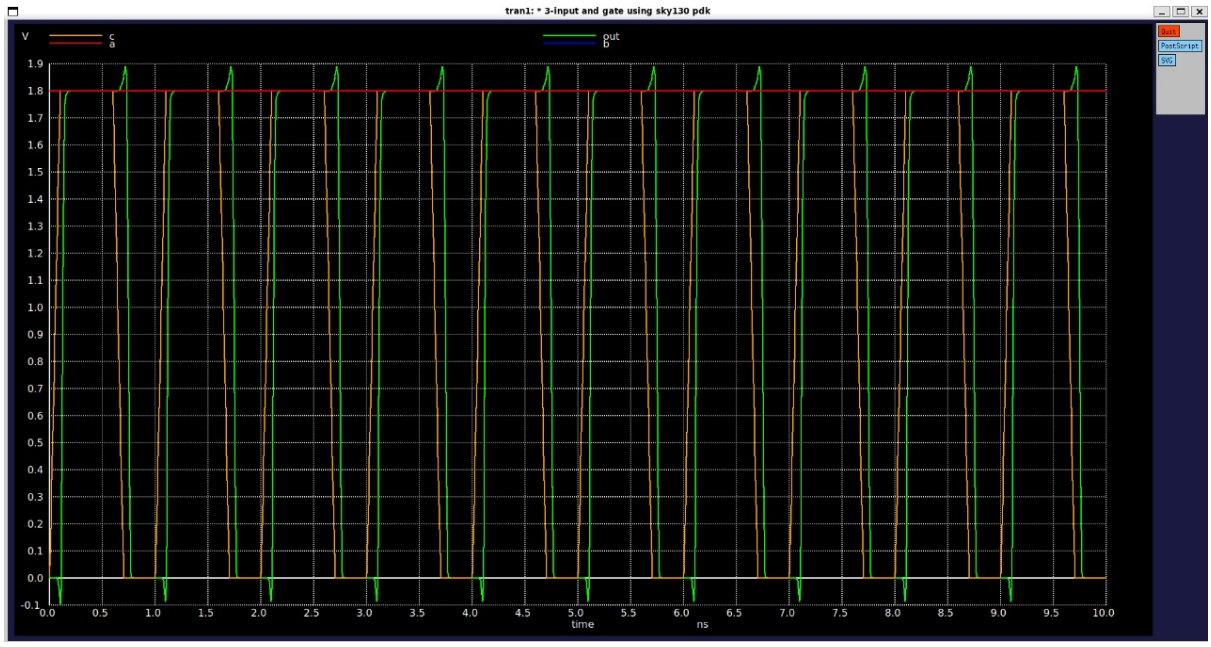

Figure 2.6: C active, other constant

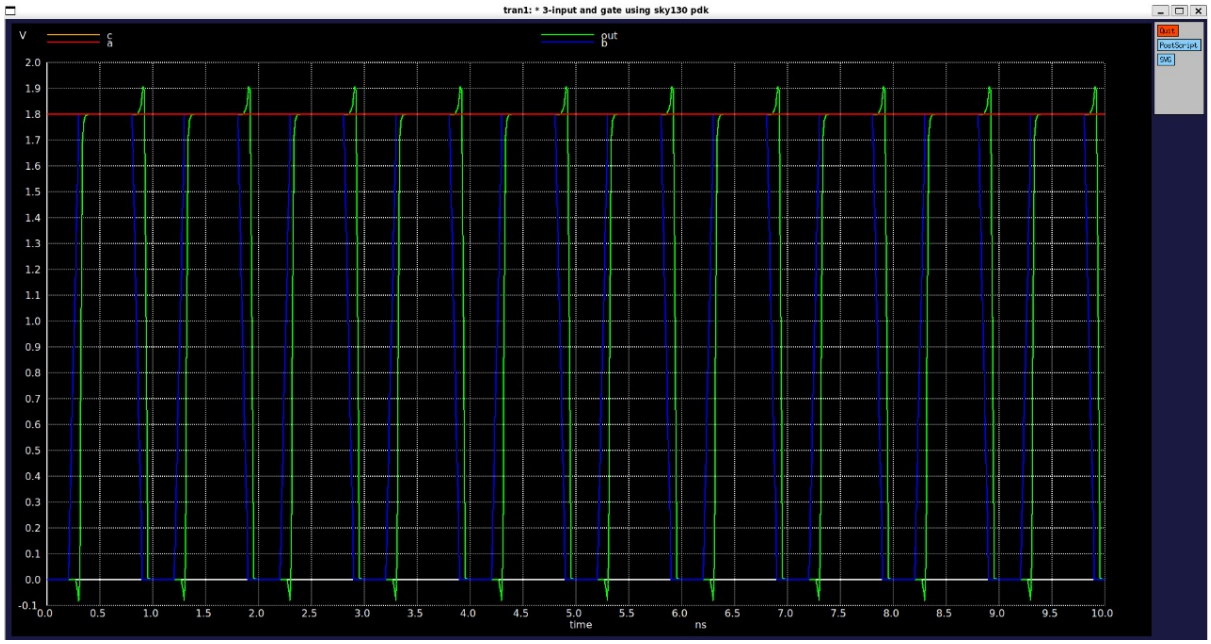

Figure 2.7: B active, other constant

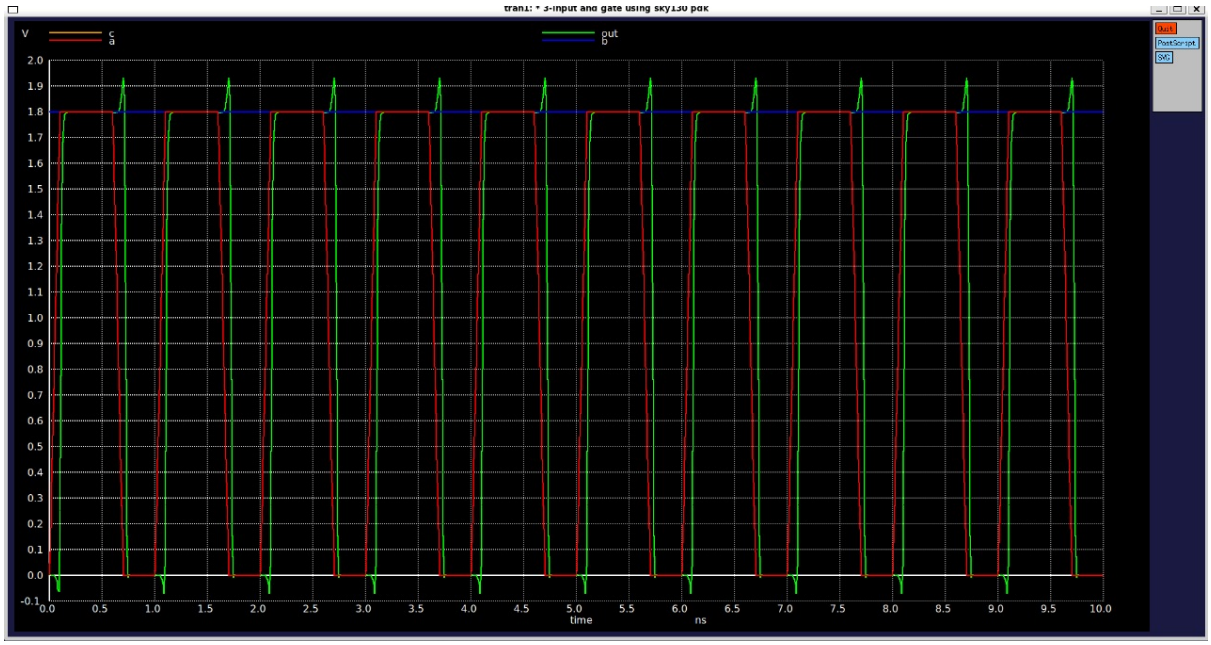

Figure 2.8: A active, other constant

Chapter 3

Cell 3: D Flip Flop

3.1 Circuit Diagram

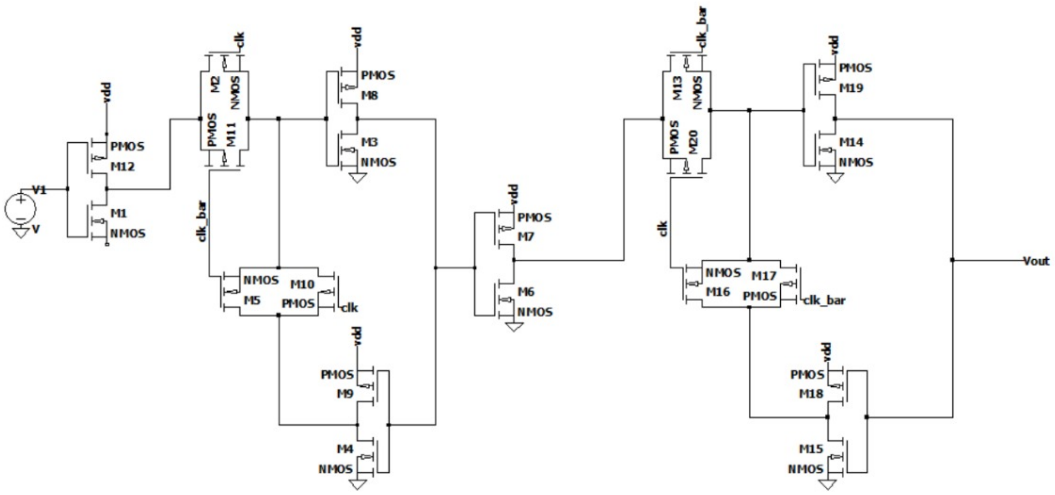

Figure 3.1: Circuit schematic

MOSFET Widths and Lengths

Table 3.1: MOSFET Width and Length for D flip flop

MOSFET	Width (W)	Length (L)
NMOS	0.42 μm	0.15 μm
PMOS	1.27 μm	0.15 μm

3.2 Layout

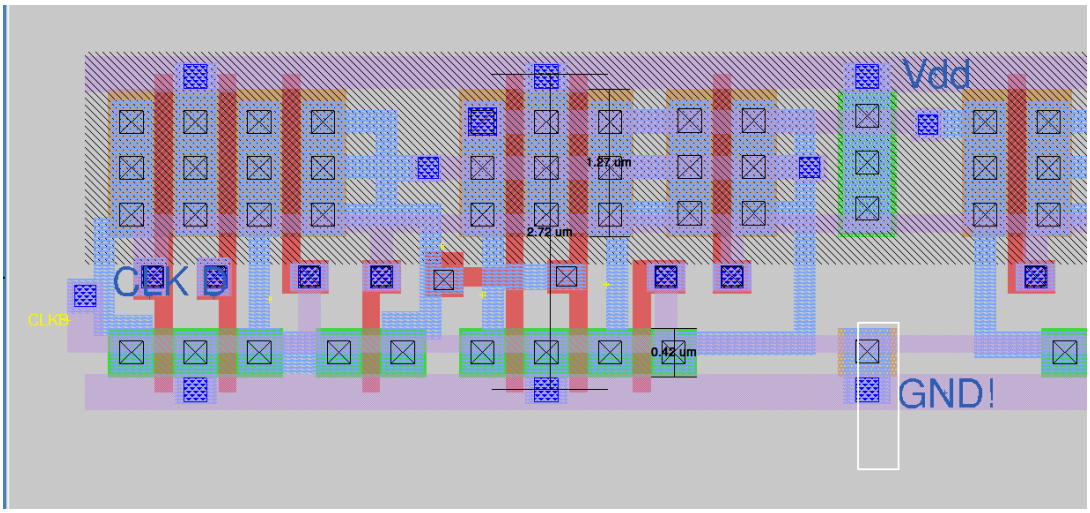

Figure 3.2: D flip flop Layout

3.3 PEX Netlist

```
* NGSPICE file created from dfxtn.ext - technology: sky130A

X0 GND CLK CLKB GND sky130_fd_pr__nfet_01v8 ad=0.096 pd=0.93714 as
    =0.168 ps=1.64 w=0.42 l=0.15
X1 GND 2 3 GND sky130_fd_pr__nfet_01v8 ad=0.096 pd=0.93714 as=0.168 ps
    =1.64 w=0.42 l=0.15
X2 6 CLKB 3 GND sky130_fd_pr__nfet_01v8 ad=0.168 pd=1.64 as=0.168 ps
    =1.64 w=0.42 l=0.15
X3 Vdd CLK CLKB Vdd sky130_fd_pr__pfet_01v8 ad=0.29029 pd=1.90857 as
    =0.508 ps=3.34 w=1.27 l=0.15
X4 Q 7 Vdd Vdd sky130_fd_pr__pfet_01v8 ad=0.508 pd=3.34 as=0.29029 ps
    =1.90857 w=1.27 l=0.15
X5 4 3 Vdd Vdd sky130_fd_pr__pfet_01v8 ad=0.508 pd=3.34 as=0.29029 ps
    =1.90857 w=1.27 l=0.15
X6 1 D GND GND sky130_fd_pr__nfet_01v8 ad=0.168 pd=1.64 as=0.096 ps
    =0.93714 w=0.42 l=0.15
X7 4 3 GND GND sky130_fd_pr__nfet_01v8 ad=0.084 pd=0.82 as=0.096 ps
    =0.93714 w=0.42 l=0.15
X8 Vdd 2 3 Vdd sky130_fd_pr__pfet_01v8 ad=0.29029 pd=1.90857 as=0.508
    ps=3.34 w=1.27 l=0.15
X9 8 7 GND GND sky130_fd_pr__nfet_01v8 ad=0.084 pd=0.82 as=0.096 ps
    =0.93714 w=0.42 l=0.15
X10 Q 7 GND GND sky130_fd_pr__nfet_01v8 ad=0.168 pd=1.64 as=0.096 ps
    =0.93714 w=0.42 l=0.15
X11 6 CLK 3 Vdd sky130_fd_pr__pfet_01v8 ad=0.508 pd=3.34 as=0.508 ps
    =3.34 w=1.27 l=0.15
X12 6 CLKB 8 Vdd sky130_fd_pr__pfet_01v8 ad=0.508 pd=3.34 as=0.508 ps
    =3.34 w=1.27 l=0.15
X13 2 CLK 1 GND sky130_fd_pr__nfet_01v8 ad=0.168 pd=1.64 as=0.168 ps
    =1.64 w=0.42 l=0.15
X14 2 CLK 4 Vdd sky130_fd_pr__pfet_01v8 ad=0.508 pd=3.34 as=0.508 ps
    =3.34 w=1.27 l=0.15
X15 8 7 Vdd Vdd sky130_fd_pr__pfet_01v8 ad=0.508 pd=3.34 as=0.29029 ps
    =1.90857 w=1.27 l=0.15
```

```
X16 Vdd 6 7 Vdd sky130_fd_pr__pfet_01v8 ad=0.29029 pd=1.90857 as=0.508
   ps=3.34 w=1.27 l=0.15
X17 2 CLKB 4 GND sky130_fd_pr__nfet_01v8 ad=0.168 pd=1.64 as=0.084 ps
   =0.82 w=0.42 l=0.15
X18 6 CLK 8 GND sky130_fd_pr__nfet_01v8 ad=0.168 pd=1.64 as=0.084 ps
   =0.82 w=0.42 l=0.15
X19 2 CLKB 1 Vdd sky130_fd_pr__pfet_01v8 ad=0.508 pd=3.34 as=0.254 ps
   =1.67 w=1.27 l=0.15
X20 GND 6 7 GND sky130_fd_pr__nfet_01v8 ad=0.096 pd=0.93714 as=0.168 ps
   =1.64 w=0.42 l=0.15
X21 1 D Vdd Vdd sky130_fd_pr__pfet_01v8 ad=0.254 pd=1.67 as=0.29029 ps
   =1.90857 w=1.27 l=0.15
C0 1 CLK 0.04425f
C1 CLK 6 0.33002f
C2 Vdd 3 0.83127f
C3 CLK 7 0.08758f
C4 6 7 0.68201f
C5 3 CLKB 0.11808f
C6 Vdd CLKB 0.31919f
C7 3 D 0
C8 2 3 0.64605f
C9 Vdd D 0.07342f
C10 2 Vdd 0.39594f
C11 CLKB D 0.07255f
C12 2 CLKB 0.15223f
C13 Q 6 0.01267f
C14 2 D 0
C15 8 3 0
C16 8 Vdd 0.14803f
C17 3 4 0.10353f
C18 Vdd 4 0.14781f
C19 Q 7 0.10495f
C20 8 CLKB 0.03889f
C21 CLKB 4 0.09004f
C22 2 4 0.19755f
C23 3 1 0
C24 3 CLK 0.20383f
C25 3 6 0.14216f
C26 Vdd 1 0.12343f
C27 Vdd CLK 0.54154f
C28 Vdd 6 0.39582f
C29 3 7 0.00648f
C30 CLKB 1 0.129f
C31 Vdd 7 0.77569f
C32 CLKB CLK 0.88359f
C33 CLKB 6 0.27587f
C34 1 D 0.05383f
C35 CLK D 0.14934f
C36 2 1 0.13947f
C37 2 CLK 0.58023f
C38 2 6 0.00437f
C39 CLKB 7 0.07134f
C40 2 7 0
C41 8 CLK 0.10875f
C42 8 6 0.20013f
C43 Vdd Q 0.13748f
C44 4 CLK 0.06462f
C45 8 7 0.10584f
```

```
C46 CLKB Q 0.00168f
C47 4 7 0
C48 Q GND 0.20568f
C49 D GND 0.14513f
C50 CLK GND 0.60702f
C51 Vdd GND 3.64435f
C52 8 GND 0.11032f
C53 4 GND 0.11053f
C54 1 GND 0.14012f
C55 7 GND 0.49242f
C56 6 GND 0.4627f
C57 3 GND 0.38351f
C58 2 GND 0.44406f
C59 CLKB GND 2.01245f
```

Figure 3.3: PEX Netlist of the Inverter

3.4 DRC and LVS Results

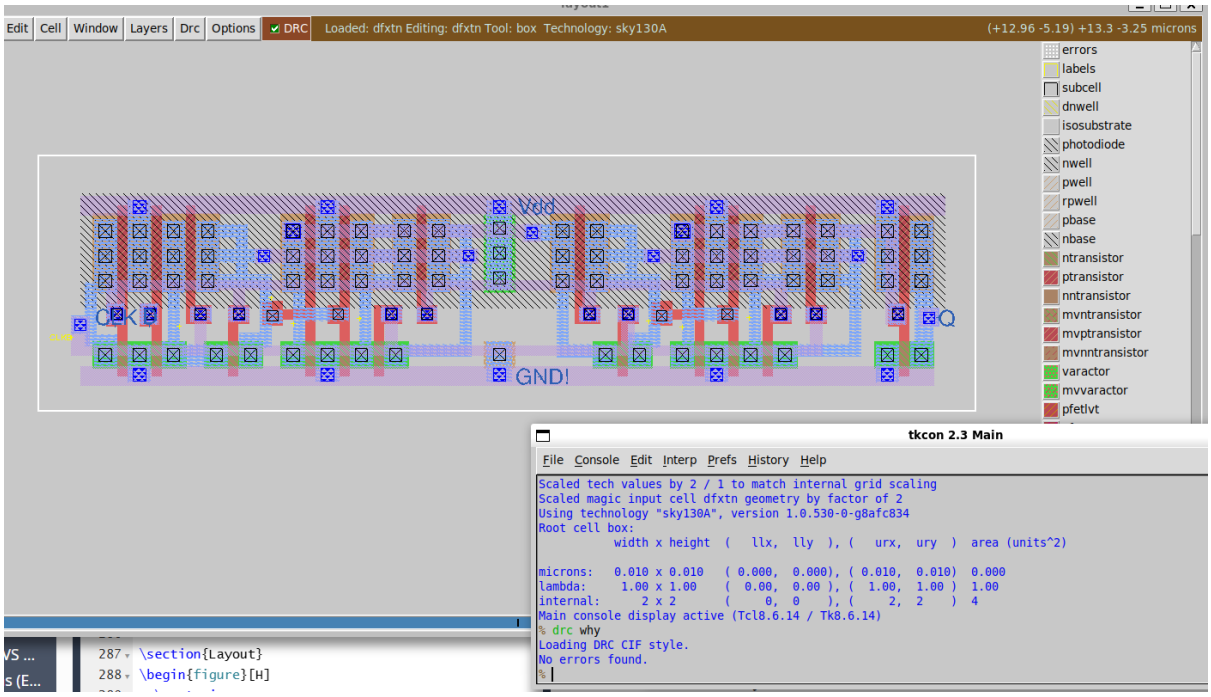

Figure 3.4: DRC Clean Screenshot for D Flip Flop

```
File  Edit  View  Terminal  Tabs  Help
Circuit dfxtn contains 22 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  11
  Class: sky130_fd_pr__pfet_01v8 instances:  11
Circuit contains 13 nets.
Contents of circuit 2:  Circuit: 'dfxtns'
Circuit dfxtns contains 22 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  11
  Class: sky130_fd_pr__pfet_01v8 instances:  11
Circuit contains 13 nets.

Circuit 1 contains 22 devices, Circuit 2 contains 22 devices.
Circuit 1 contains 13 nets,    Circuit 2 contains 13 nets.


Final result:
Circuits match uniquely.
Property errors were found.

The following cells had property errors:
 dfxtn

Logging to file "comp.out" disabled
LVS Done.
/foss/designs >
```

Figure 3.5: LVS Clean Screenshot for D Flip Flop

3.5 Simulations (Explanations and Graphs)

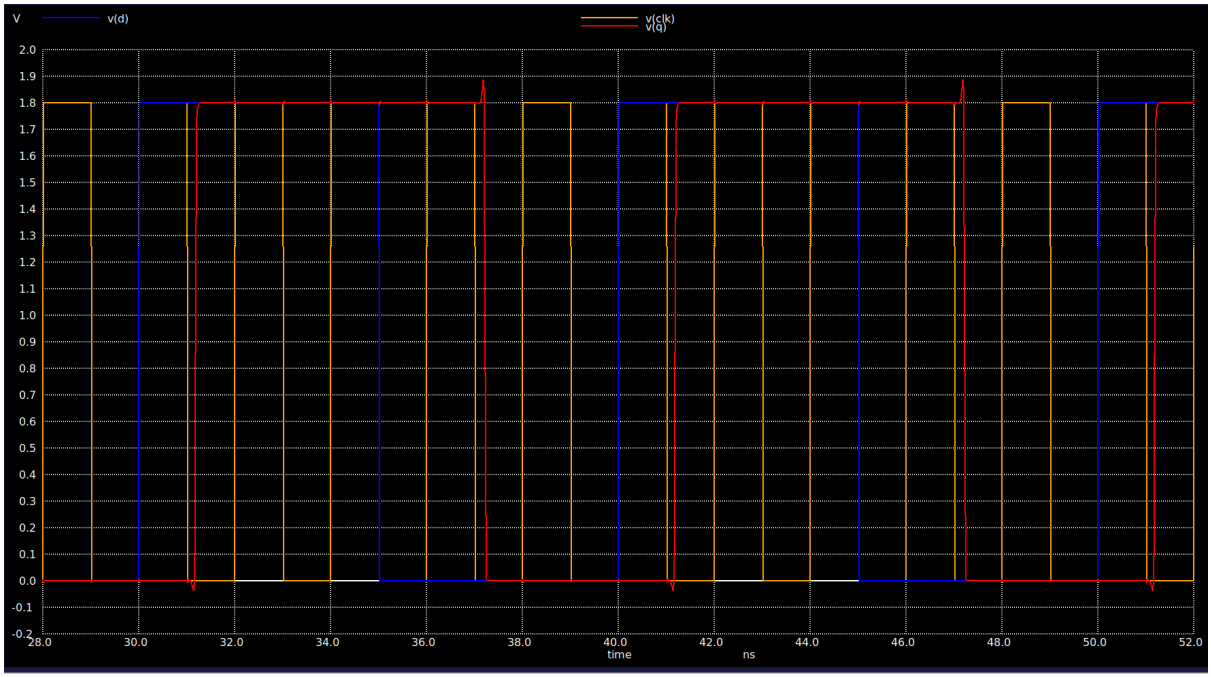

Figure 3.6: Waveform simulation

3.6 Timing and Power Table (selected)

3.6.1 Input Pin Capacitances

Table 3.2: Input Pin Capacitances (D and CLK)

Input Pin	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
D	0.65e-03	0.40e-03	0.535e-03
CLK	4.4e-02	2.8e-02	3.6e-02

3.6.2 Setup and Hold Constraints (examples)

Table 3.3: Setup Time Constraints (Rise Constraint sample values)

Input Slew	CLK Slew (sample)	Value (ns)
10 ps	1000 ps	4.515 ns
1000 ps	10 ps	6.5 ns

3.6.3 Transition Times (examples)

Table 3.4: Output Rise Transitions (related pin D)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.024 ns	0.074 ns	0.59 ns
100 ps	0.023 ns	0.074 ns	0.59 ns
1000 ps	0.023 ns	0.074 ns	0.59 ns

Table 3.5: Output Fall Transitions (related pin D)

Input Slew	0.5 fF	10 fF	100 fF
10 ps	0.02 ns	0.078 ns	0.642 ns
100 ps	0.02 ns	0.078 ns	0.642 ns
1000 ps	0.02 ns	0.078 ns	0.642 ns

please refer attached pdf file for all sections .

Chapter 4

Team Contributions

- **Member 1: Dikshit Singla**
  - Setup and Hold Simulations for the D Flip Flop
  - Report Making
  - Designing the layout of INV and DFF cells —including DRC, LEF and LVS
  - Timing and Power simulations AND3
  - Ngspice Netlists for INV
- **Member 2: Sahil Wani**
  - Verilog files for all the 3 cells
  - Timing and Power Characterization of INV gate
  - Designing the layout of DFF cells —including DRC, LEF and LVS
  - Ngspice Netlists for DFF and AND
- **Member 3: Mohammad Bohra**
  - Designing the layout of AND3 cells —including DRC, LEF and LVS
- **Member 4: Rahul Naik**
  - Nothing

References

- NGSpice documentation: http://ngspice.sourceforge.net/docs.html
- Magic VLSI documentation: http://opencircuitdesign.com/magic/index.html
- Icarus Verilog: http://iverilog.icarus.com/
- *CMOS VLSI Design: A Circuits and Systems Perspective* — Neil Weste and David Harris
- Course Lecture Slides: EE-671