|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Cache | Cache Line Size | Total Size | Associativity  (Ways) | Number of sets =  (C[2]/(C[1]\*C[3])) |
| L1-Data | 64 | 49152 | 12 | 64 |
| L2 | 64 | 1310720 | 20 | 1024 |
| L3 | 64 | 8388608 | 8 | 16384 |

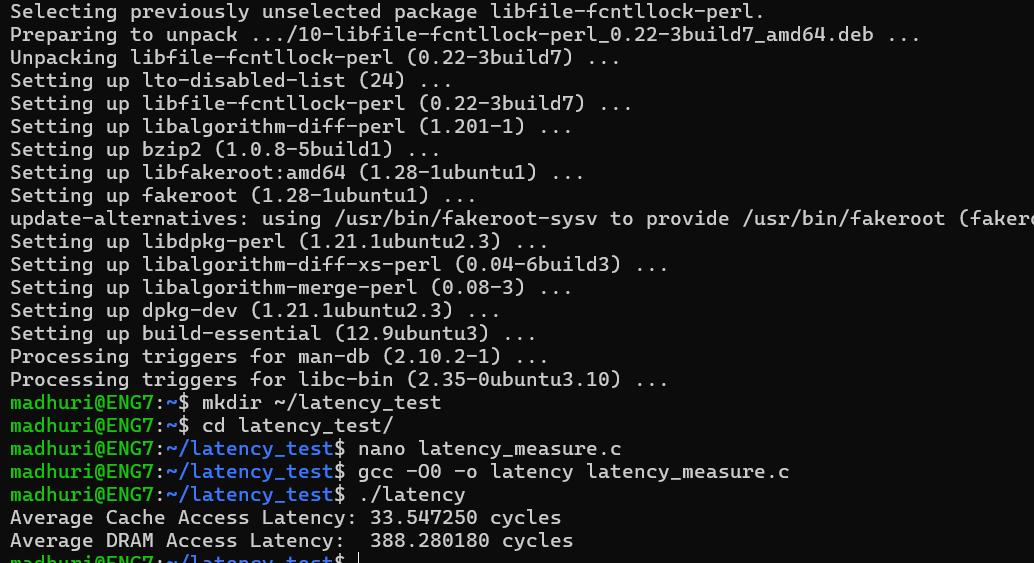
**Exploring Cache Architecture and Access Timing**

LS 2025: Computer Architecture & Hardware security  
Mission1  
 Dikshit Singla, 23b3974

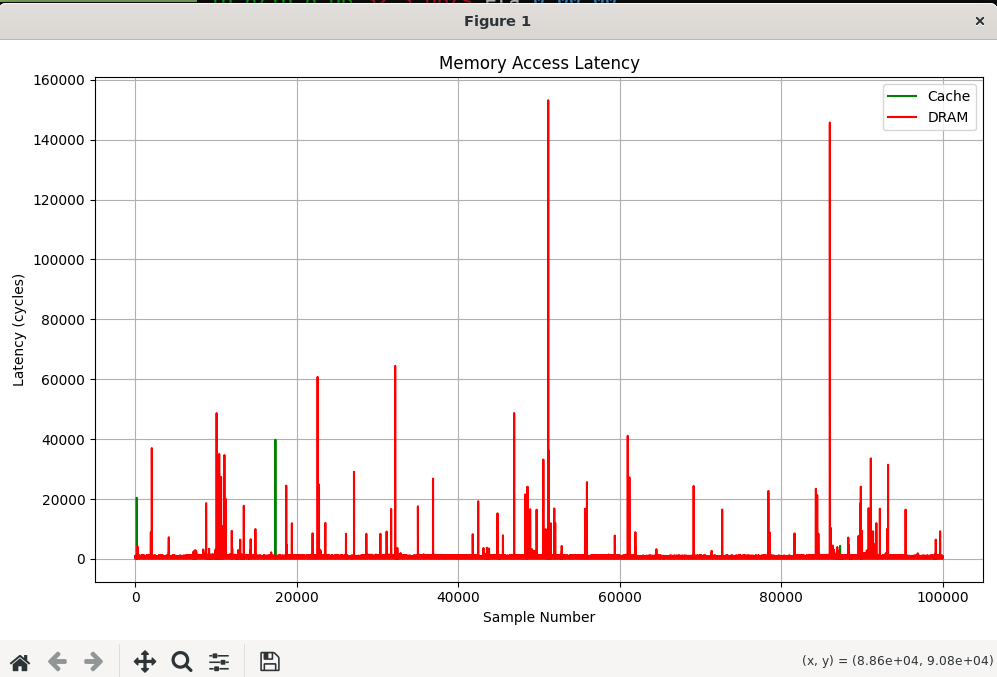
Part 1.1 Determining Machine Architecture

Part 1.2: Measuring Memory Access Latencies

|  |  |
| --- | --- |
| Memory Type | Measured Latency |
| Cache | 33.54 cycles |
| DRAM | 388.28 cycles |



Plot-



Code explanation-

I have taken samples to be 100000  
then I defined a function to calculate the access time using the standard functions like rdtsc, lfence, sfence, clflush,

Then in the main()

I have allocated the memory and set the caution for error

I am saving the results in a csv file

Then dram\_total,cache\_total is total of all latencies entries used to calculate the average. And cache ,dram are used to save in csv to make the plot .  
and the results are printed.