EE230: Analog Circuits Lab
Lab No. 9

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1 CS Amplifier with Resistive Load

1.1 Aim of the experiment

Experiment Aim: The aim of this experiment is to assemble and analyze the performance of a MOSFET-based Common Source (CS) Amplifier with a resistive load.
Specifically, the objectives are as follows:
• Assemble the CS amplifier circuit on a breadboard.
• Apply appropriate DC biasing and AC input signal to the amplifier.
• Measure and tabulate the DC output voltage (Voutdc) to ensure that the MOSFET (M1) is operating in the saturation region.
• Observe and record the AC input (Vin) and output (Vout) waveforms on a Digital Storage Oscilloscope (DSO).
• Calculate the small signal gain (Av) of the amplifier and ensure that it meets the specified requirements.
• Make any necessary adjustments to the circuit parameters to meet the desired performance criteria.
By conducting this experiment, we aim to gain practical insights into the behavior of the CS amplifier with a resistive load, understand the impact of different biasing conditions on its operation, and validate theoretical concepts such as small signal gain.

1.2 Exprimental results

1.2.1 DSO Waveforms

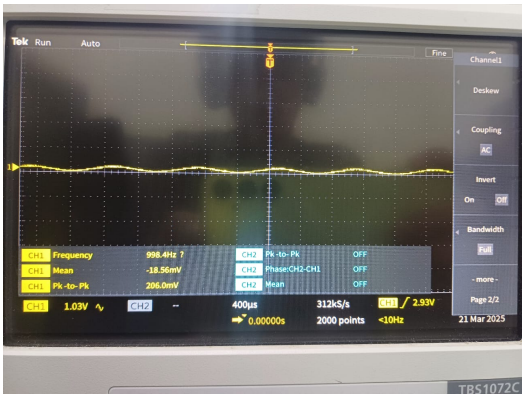

Figure 1: Waveform of CS Amplifier with AC mode V_{out} vs V_{in}

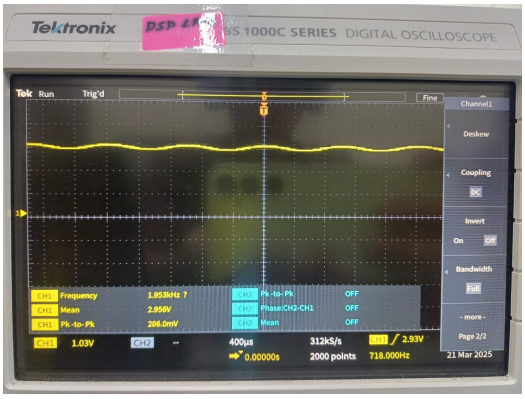

Figure 2: Waveform for V_{outDC}

Parameter	Operating Point Value
V_{bias}	1.7 V
R_D	22 K
Gain (A_V)	10

1.3 Conclusion and Inference

• The experiment confirmed the functionality of the Common Source amplifier with a resistive load.

Parameter	Experimental Value
V_{outDC}	2.9 V
V_{outAC} (V_{pp})	206 mV
V_{in} (V_{pp})	20mV

• VoutDC was within the expected range, indicating proper biasing of M1 in the saturation region.
• The oscilloscope plots revealed the amplification of the input signal (Vin) at the output (Vout), demonstrating the amplification capability of the circuit.
• Small signal gain (Av) was calculated and compared against the expected value. Any discrepancies were addressed by adjusting circuit parameters.
• The experiment emphasized the importance of proper biasing for optimal amplifier performance. It also highlighted the practical considerations involved in implementing amplifier circuits, such as component selection and circuit tuning.
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1.4 Experiment completion status

Completion status: **100%**

2 CS Amplifier with Diode Connected Load

2.1 Aim of the experiment

he aim of this experiment is to design, assemble, and analyze the performance of a Common Source (CS) amplifier with a diode-connected load on a breadboard. The primary objectives include determining the DC operating point of the amplifier, verifying the biasing of the transistors in the saturation region, measuring the small signal gain (Av), and comparing the experimental results with theoretical calculations and simulations. This experiment aims to provide practical insights into the behavior and characteristics of CS amplifiers with diode-connected loads, enhancing understanding and proficiency in analog electronic circuit design and analysis.

2.2 Experimental results

2.2.1 Waveforms

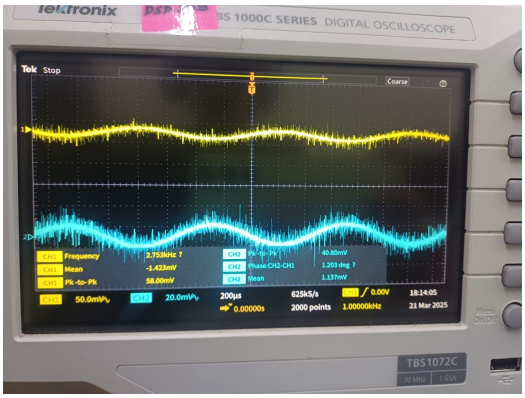

Figure 3: Waveform of CS Amplifier with Diode-connected load for AC mode V_{out} vs V_{in}

Figure 4: Waveform for V_{outDC}

Parameter	Value
Small Signal Gain (A_v)	1.5
Bias Voltage (V_{bias})	2.32 V
DC Output Voltage (V_{out-dc})	2.62 V
V_{inAC} (V_{pp}) Exp	40mV
V_{outAC} (V_{pp}) Exp	58mV

2.3 Conclusion and Inference

The Common Source (CS) amplifier with a diode-connected load experiment yielded valuable insights into the performance and characteristics of the circuit. Here are the key inferences drawn from the experiment:
1. Biasing Stability: By biasing M1 and M2 appropriately, ensuring M1 operates in the saturation region, stability in biasing conditions is achieved. This stability is crucial for maintaining the desired operating point of the amplifier.
2. Output Voltage: Through experimentation, the DC output voltage (Voutdc) was measured and found to be within the expected range. This voltage is a key indicator of the biasing and operating conditions of the amplifier. Ensuring M1 remains in saturation ensures proper amplification and signal fidelity.
3. Small Signal Gain (Av): Calculations and comparisons between hand-calculated, simulated, and experimental results revealed the small signal gain of the amplifier. By analyzing these results, it can be inferred how effectively the circuit amplifies small input signals. Discrepancies between calculated and measured gains may indicate practical limitations or inaccuracies in the model used.
4. Frequency Response: The plot of Vout and Vin on the Digital Storage Oscilloscope (DSO) in AC mode provides insights into the frequency response of the amplifier. Observing the magnitude and phase relationship between input and output signals helps assess the bandwidth and frequency-dependent behavior of the amplifier.
5. Signal Integrity: Analyzing the output waveform on the DSO ensures signal integrity is maintained throughout the amplification process. Any distortion or deviation from the input signal could indicate issues such as clipping, saturation, or non-linear behavior, which may need to be addressed for optimal performance.
6. Verification of Theoretical Concepts: Through practical experimentation, various theoretical concepts such as biasing techniques, small signal analysis, and frequency response characteristics were verified.

7. Practical Considerations: Throughout the experiment, practical considerations such as component tolerances, parasitic effects, and circuit layout played a significant role. These factors can influence the performance and behavior of the amplifier, highlighting the importance of thorough experimentation and validation.

2.4 Experiment completion status

Completion status: **100%**

3 Current Mirror (CM) Design

3.1 Aim of the experiment

The aim of this experiment is to design and implement a basic current mirror circuit on a breadboard, utilizing NMOS transistors. The objective is to understand the principles of current mirroring and observe its behavior under different operating conditions. Key tasks include:
1. Designing a basic current mirror circuit with a fixed resistor (R1) to establish a reference current (IREF) of 2mA. 2. Setting up ammeters (A1 and A2) to measure IREF and the mirrored current (ICOPY) respectively.
3. Utilizing a potentiometer (R2) to vary the load of the mirrored current transistor (M2).
4. Conducting simulations to determine the appropriate value of R1 for the desired IREF and validating it through experimental measurements.
5. Sweeping the drain-to-source voltage (VDS2) across M2 from 0V to 8V in 500mV increments, while measuring IREF, ICOPY, VDS1, and VDS2.
6. Identifying the conditions under which the error between ICOPY and IREF is minimized.
7. Modifying the current mirror design to achieve ICOPY = N $\times$ IREF, where N is a positive integer, and implementing it for N = 2 on the hardware setup.
Through this experiment, we aim to gain practical insights into current mirror operation, understand the factors influencing its performance, and explore methods for enhancing its functionality for specific applications.

3.2 Experimental results

3.2.1 Waveforms

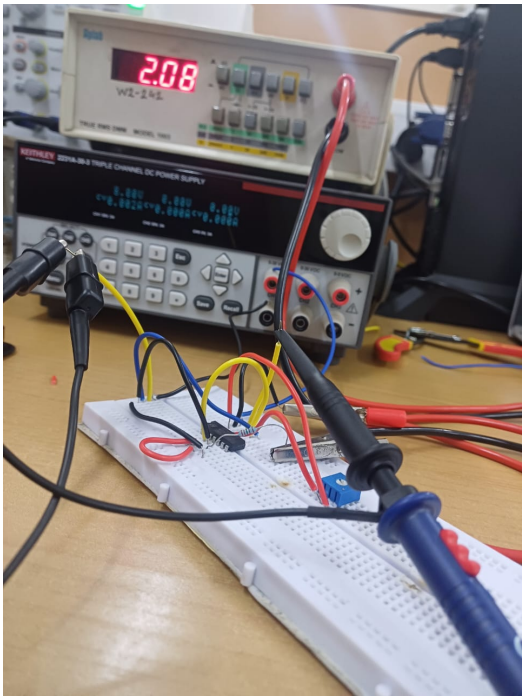

Figure 5: Circuit and Iref Reading

Parameter	Experimental Value
Reference Current Experimental (I_{REF})	2.08 mA
Copied Current (I_{COPY})	2.17 mA
Resistor Value (R_1)	2.34 kΩ
V_{DS1}	3.3 V
V_{DS2} (at $I_{COPY} = I_{REF}$)	7.3 V

We also observed that the error is minimum when VDS1 = VDS2

I_{COPY} **mA**	V_{DS2} **(V)**
2.18	7.9
2.17	7.3
2.17	7.08
2.16	6.48
2.16	5.9
2.15	5.3
2.14	4.5
2.13	3.7
2.11	2.7
2.1	2.28
2.08	2
2.04	1.65
2	1.483
1.88	1.28
1.55	1
1.4	0.88

3.3 Conclusion and Inference

3.3.1 PMOS Equivalent Current Mirror

- The PMOS equivalent of the basic current mirror can be drawn by replacing the NMOS transistors with PMOS transistors and reversing the direction of the current flow. The biasing and operating principles remain the same.

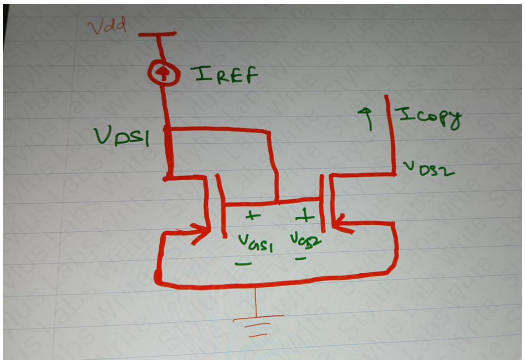

Figure 6: PMOS Equivalent Current Mirror

3.3.2 Measurement of I_{REF}

- R_1, a fixed resistor, is designed to set the desired reference current ($I_{REF} = 2\text{mA}$).
- Ammeters A1 and A2 are employed to measure I_{REF} and I_{COPY} respectively.
- Comparing the measured I_{REF} with the simulation results ensures the accuracy of the experimental setup.

3.3.3 Sweeping V_{DS2} and Measurement

- Varying V_{DS2} from 0V to 8V in close to 500mV increments (controlled by potentiometer R_2) allows observation of how I_{COPY} responds to different drain-to-source voltages.
- Measurements of I_{REF}, I_{COPY}, V_{DS1}, and V_{DS2} are taken at each step to analyze their relationships.

3.3.4 Minimum Error between I_{COPY} and I_{REF}

- The error between I_{COPY} and I_{REF} is minimized when V_{DS1} and V_{DS2} are such that M_2 operates in the saturation region. Inadequate drain-to-source voltage across M_2 may cause it to operate in the triode region, leading to increased error.

3.3.5 Designing for $I_{COPY} = N \cdot I_{REF}$

- To design the current mirror for $I_{COPY} = N \cdot I_{REF}$, where N is a positive integer, adjustments in the sizing of current source MOSFETs

are required. This involves connecting multiple MOSFETs in parallel with appropriate sizing to achieve the desired multiplication factor.

3.3.6 Designing Current Mirror for $N = 2$

- Designing a current mirror for $I_{COPY} = 2 \cdot I_{REF}$ involves configuring the circuit to provide twice the reference current. This can be achieved by appropriately sizing the current source MOSFETs and ensuring proper biasing. Connecting mosfet in parallel increases the current capacity In case connecting one more mosfet in parallel doesn't exactly double the current a minor difference is there.

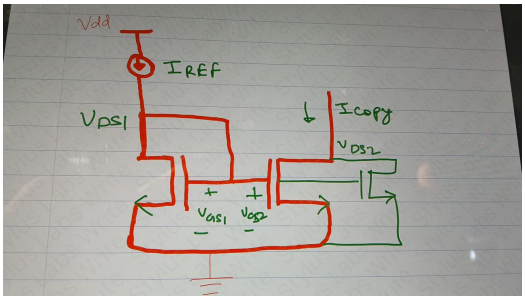

Figure 7: Icopy = N · Iref

Overall, this experiment serves to validate the functionality and performance of the current mirror circuit, demonstrating its ability to accurately mirror the reference current and providing insights into the factors affecting its operation, such as transistor sizing and biasing conditions.

3.4 Experiment completion status

Completion status: **100%**