Microelectronic Systems Project

The DLX microprocessor

Group 04:
Sansone Giacomo - s307761
Silvestri Giuseppe - s307792
Valenza Arianna - s317742

Introduction

The DLX is a pipelined RISC architecture which was originally developed by Hennessy and Patterson. We followed their original work, adapting the architecture to the features we decided to add.

The pipeline has 5 stages (F, D, E, M, W). The CPU is implemented by connecting a controller and a datapath. Memories are external.

After the behavioral simulation, we synthesised it using Synopsys Design Compiler and performed the place and route with Cadence Innovus.

Our PRO features

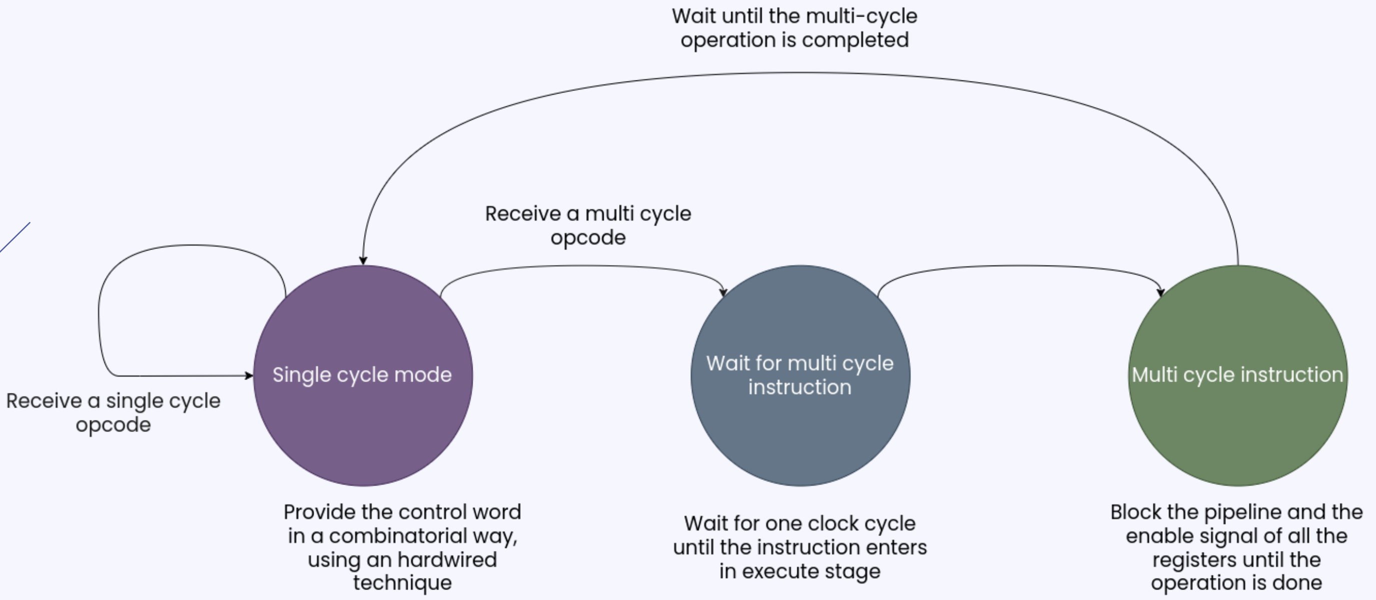
Long latency operations

- Multiplication, using Booth's algorithm;
- Division, using the radix-4 SRT algorithm with *minimally redundant digit set*. We studied the algorithm starting from a computer arithmetic book, and we documented both the theory behind it and its implementation.

Simulation

- Automated simulation scripts to verify the correctness of our programs.

The controller to handle multi-cycle instructions



Wait until the multi-cycle operation is completed

Receive a multi cycle opcode

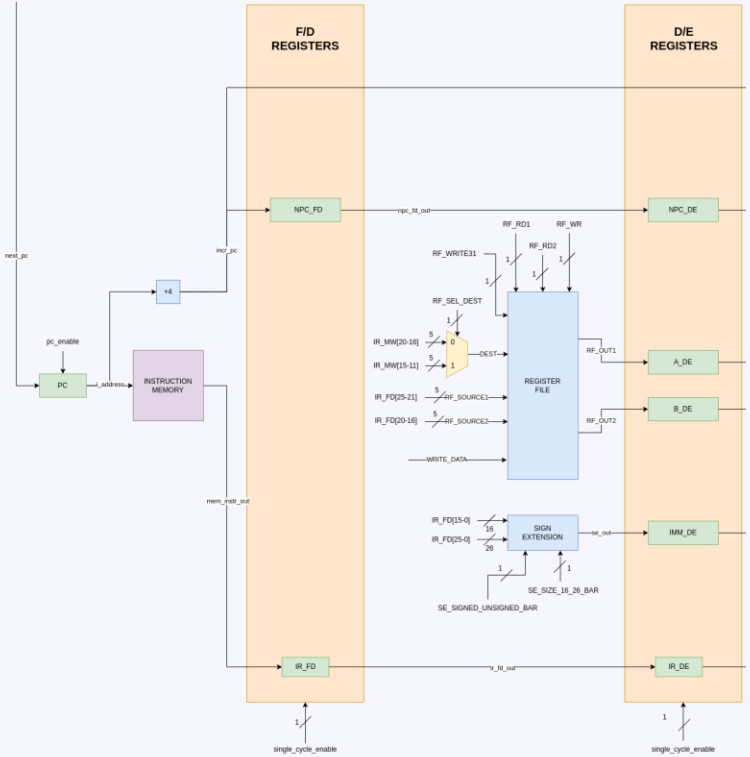
Receive a single cycle opcode

Provide the control word in a combinatorial way, using an hardwired technique

Wait for one clock cycle until the instruction enters in execute stage

Block the pipeline and the enable signal of all the registers until the operation is done

The fetch and decode stages



During the fetch stage, a new instruction is fetched from the IRAM, and the control word associated to it is stored.

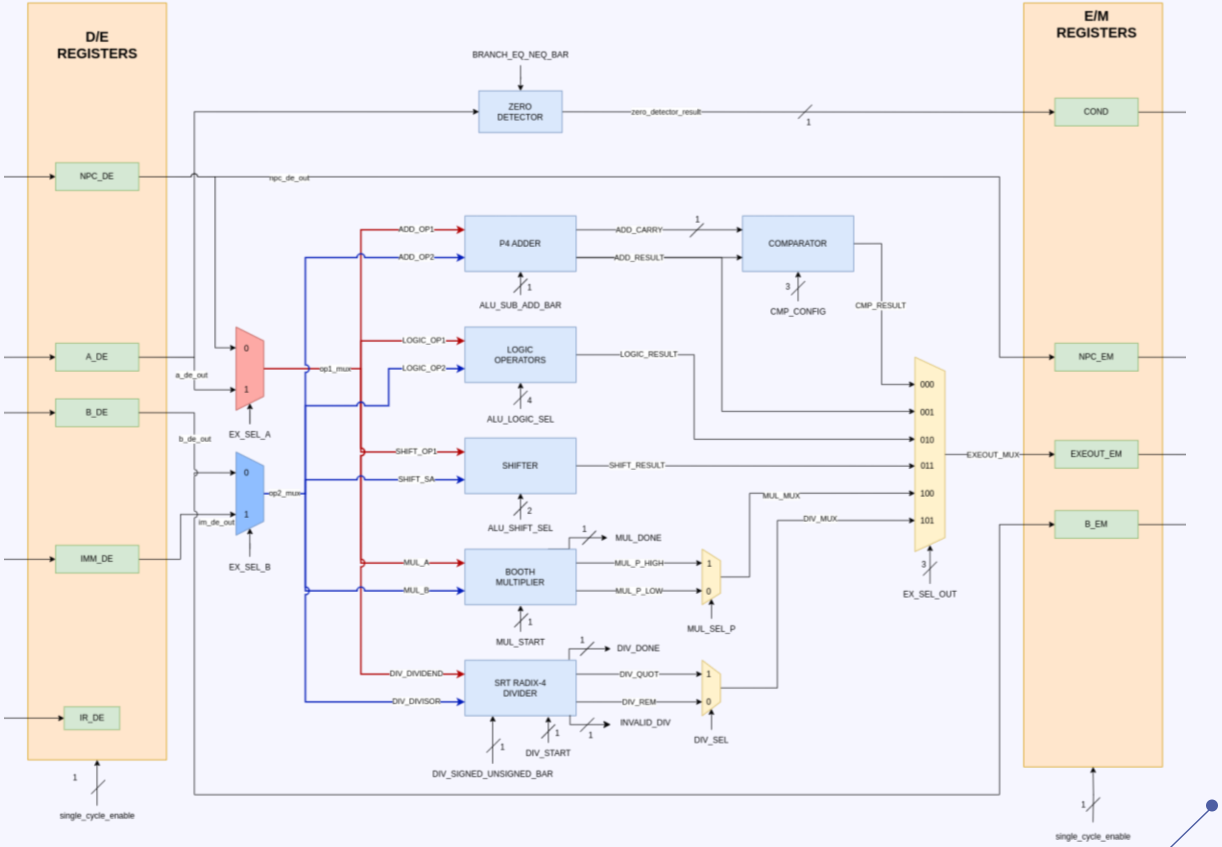
In the decode stage, all the operands for the next stage are generated.

The execute stage

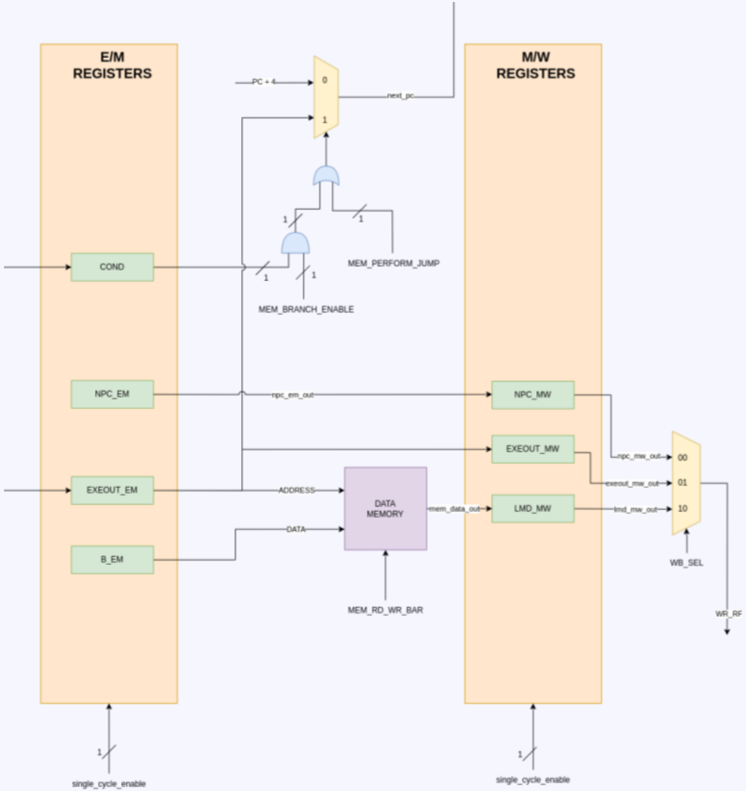
In the execution stage the correct operands are chosen among the possible ones, and the selected operation is performed.

In case of a multi-cycle instruction, the controller stops the pipeline by setting **single_cycle_enable** to 0.

The branch condition is also evaluated.



The memory and write back stages



In the memory stage, we (if need be) access the DRAM for load/store operations and compute the next program counter.

In the write back stage, we select the value that should be written in the register file at the falling edge of the clock (if any).

The multiplier

It is a radix-4 Booth multiplier which produces a result on 64 bits. It requires 16 clock cycles in the execute stage.

The divider

It is a radix-4 SRT divider with minimally redundant digit-set [-2, +2], which requires 11 clock cycles in the execution stage. The divisor is on 32, bits, the dividend on 16 bits.

Radix-4 SRT – Main characteristics

The dividend and the divisor must be normalised before the beginning of the execution (preprocessing phase).

The quotient, which is zero when *i* = 0, is iteratively computed as:

$$Q_{i+1} = 4 \cdot Q_i + q_i$$

The remainder, which is the dividend when *i* = 0, is computed as:

$$A_{i+1} = 4 \cdot (A_i - q_i \cdot d \cdot 2^N)$$

Where q_i ∈ [-2,2] is the digit calculated at iteration *i* based on the value of the divisor *d* and the remainder A_i.

After all the iterations have been completed, a postprocessing phase is required in order to get the results in the correct format.

The simulation environment

Using our scripts, it is possible to run the simulation of an assembly file and automatically check the correctness of the final value stored in a dram cell or a register.

Here are some available examples:

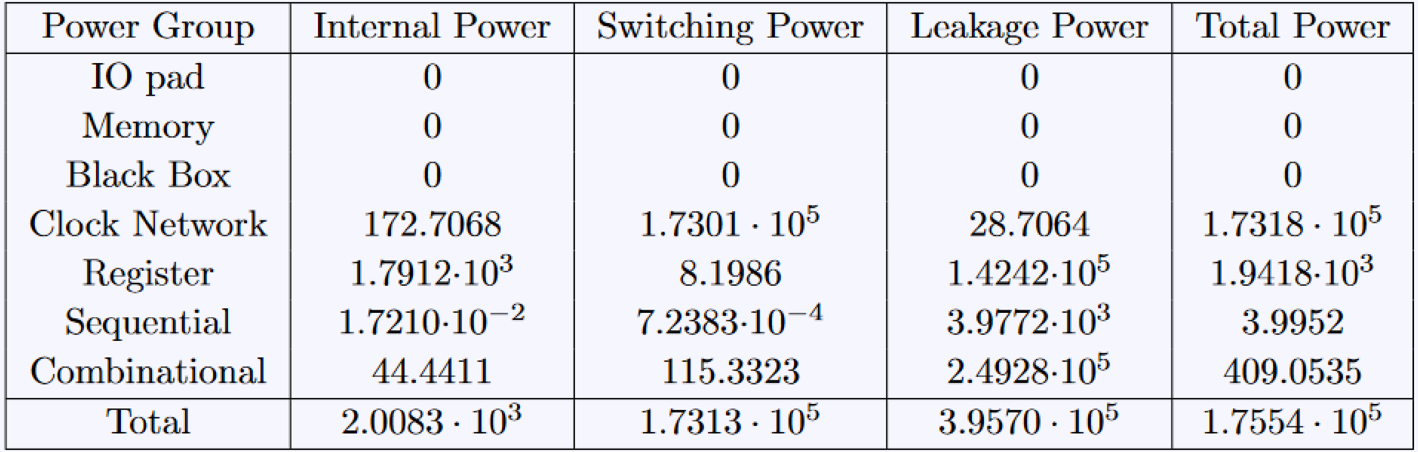
Bubble sort of an array in memory

Binomial of two numbers

Recursive factorial computation

Synthesis

The synthesis has been made using a script. The process was done with a clock period of 7 ns, because of the 64-bit RCA used inside the multiplier (in which there is the critical path of the architecture). Here are the results of the power consumption in µW:

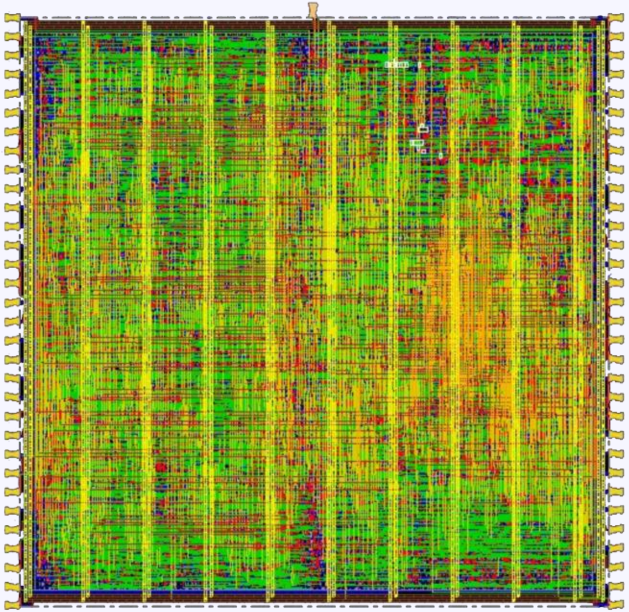


Power Group	Internal Power	Switching Power	Leakage Power	Total Power
IO pad	0	0	0	0
Memory	0	0	0	0
Black Box	0	0	0	0
Clock Network	172.7068	$1.7301 \cdot 10^5$	28.7064	$1.7318 \cdot 10^5$
Register	$1.7912{\cdot}10^3$	8.1986	$1.4242{\cdot}10^5$	$1.9418{\cdot}10^3$
Sequential	$1.7210{\cdot}10^{-2}$	$7.2383{\cdot}10^{-4}$	$3.9772{\cdot}10^3$	3.9952
Combinational	44.4411	115.3323	$2.4928{\cdot}10^5$	409.0535
Total	$2.0083 \cdot 10^3$	$1.7313 \cdot 10^5$	$3.9570 \cdot 10^5$	$1.7554 \cdot 10^5$

Physical design

- Configuring the environment;
- Structuring the floorplan;
- Inserting power rings;
- Inserting stripes;
- Standard cell power routing;
- Placement;
- Placing IO pins;
- Post Clock-Tree-Synthesis Optimization;
- Place filler;
- Routing;
- Post Routing Optimization;
- Timing and integrity analysis.

The overall analysis reports that the DLX occupies an area of 18798.5 μm^2 , 23557 gates and 10486 cells.



Thank you!

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