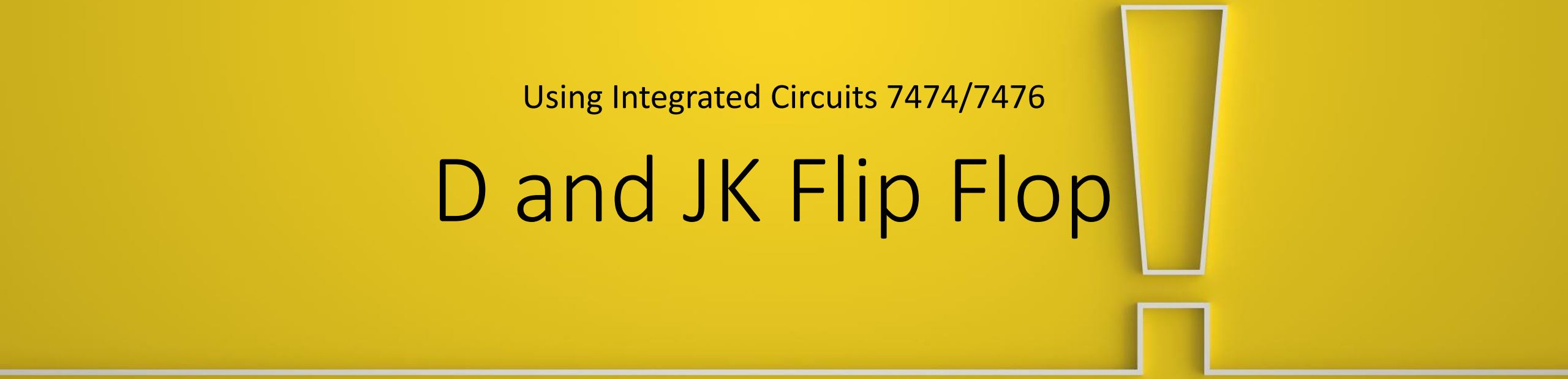
Using Integrated Circuits 7474/7476

D and JK Flip Flop



Direct Inputs(Asynchronous Operation)

7474 IC D- flipflop have the capability to be forced to the set or reset state (which ignores the D and clock inputs)

- Many circuits requires the initialization of flip flops to a known state independent of a clock pulse.
- The preset and clear inputs of Flips Flops are used for direct inputs.
- Preset and clear inputs are asynchronous Inputs.
- These inputs are useful for bringing flip flops to an initial state before their clocked operation.

Pulse or level triggering

- Type of triggering where the state transition Starts as soon as the pulse reaches the logic 1 level.
- If the other inputs change while the clock is still 1, a new state may occur.
- Drawback is that flip flop response the transition of state during entire pulse duration.

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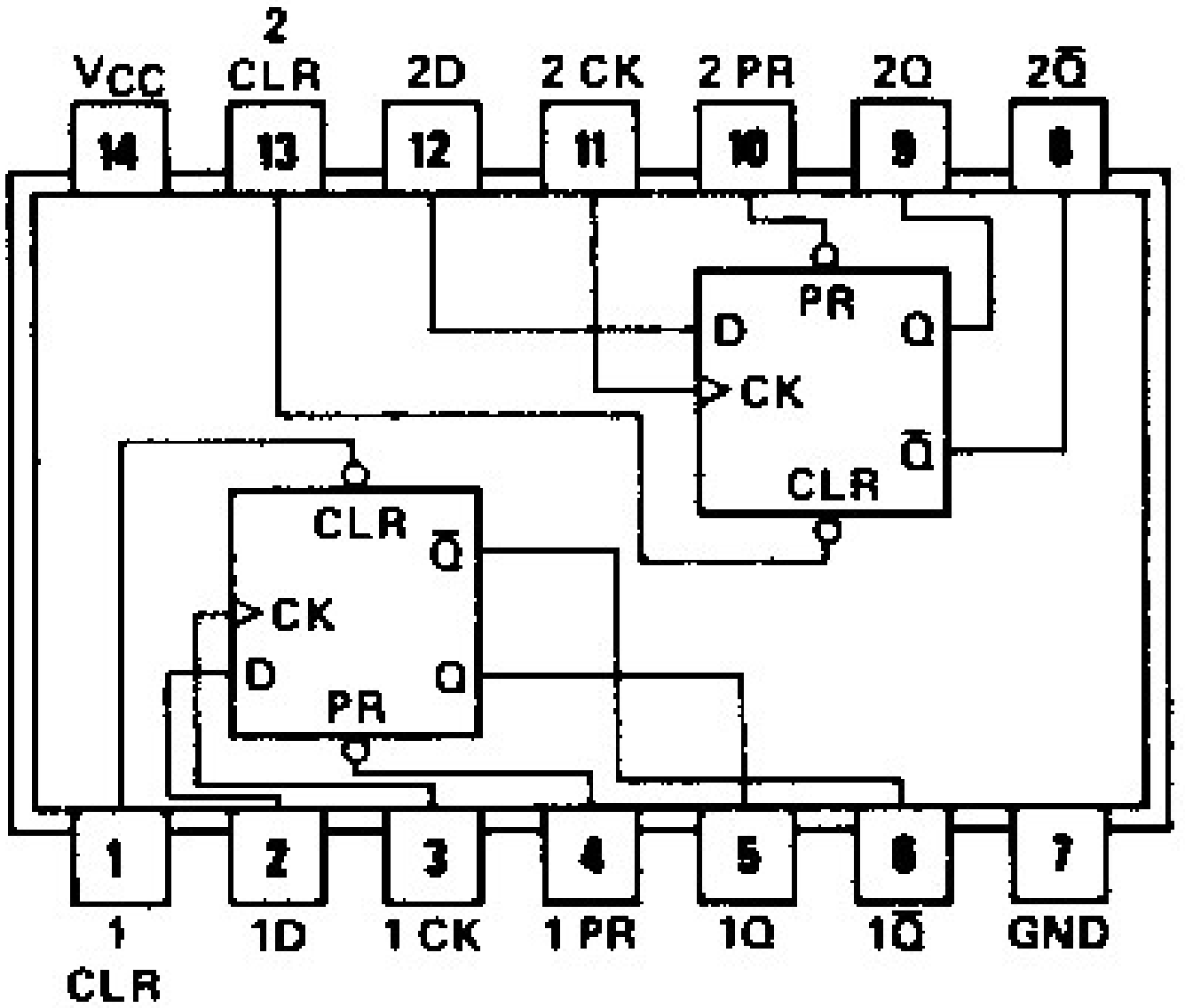
Edge triggering

- In edge triggering drawback at pulse triggering is overcomed.
- when the clock pulse input exceeds a specific threshold level the inputs are locked.
- The flip flop is not affected by further changes in the inputs until the clock pulse returns to zero and another pulse occurs.
- Some edge-triggered flip flopsCause a transition on the positive edge of the clock pulse.
- others on the negative edge of the pulse.
- We take it as positive edge trigger or negative edge trigger.

7474

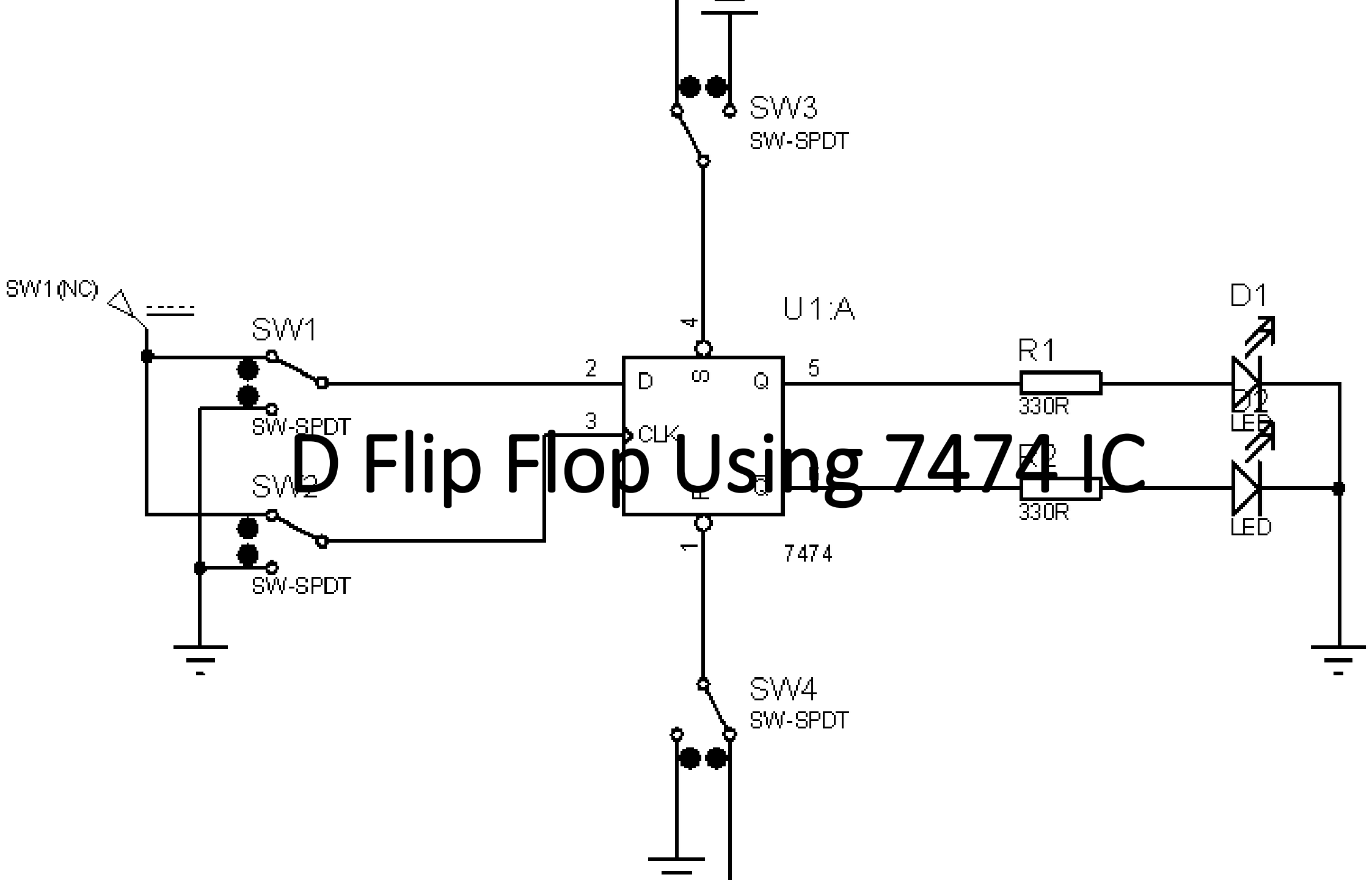

2
VCC
CLR
2D
2 CK
2 PR
2Q
2Q̄
14
13
12
11
10
9
8
PR
D
Q
CK
Q̄
CLR
CLR
Q̄
CK
D
Q
PR
1
2
3
4
5
6
7
1
CLR
1D
1 CK
1 PR
1Q
1Q̄
GND

Characteristic Table/ Equation/ Excitation table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

	D'	D
Q'_n	0	1
Q_n	0	1

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1



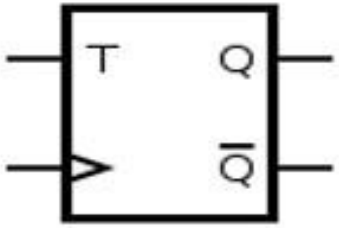
D Flip Flop Using 7474 IC

D flip Flop with Preset Clear

D	Preset	Clear	Q_n	Q_{N+1}
×	0	1	0	1
×	1	0	1	0
0	1	1	0	0
1	1	1	0	1
0	1	1	1	0

TFlipFlop

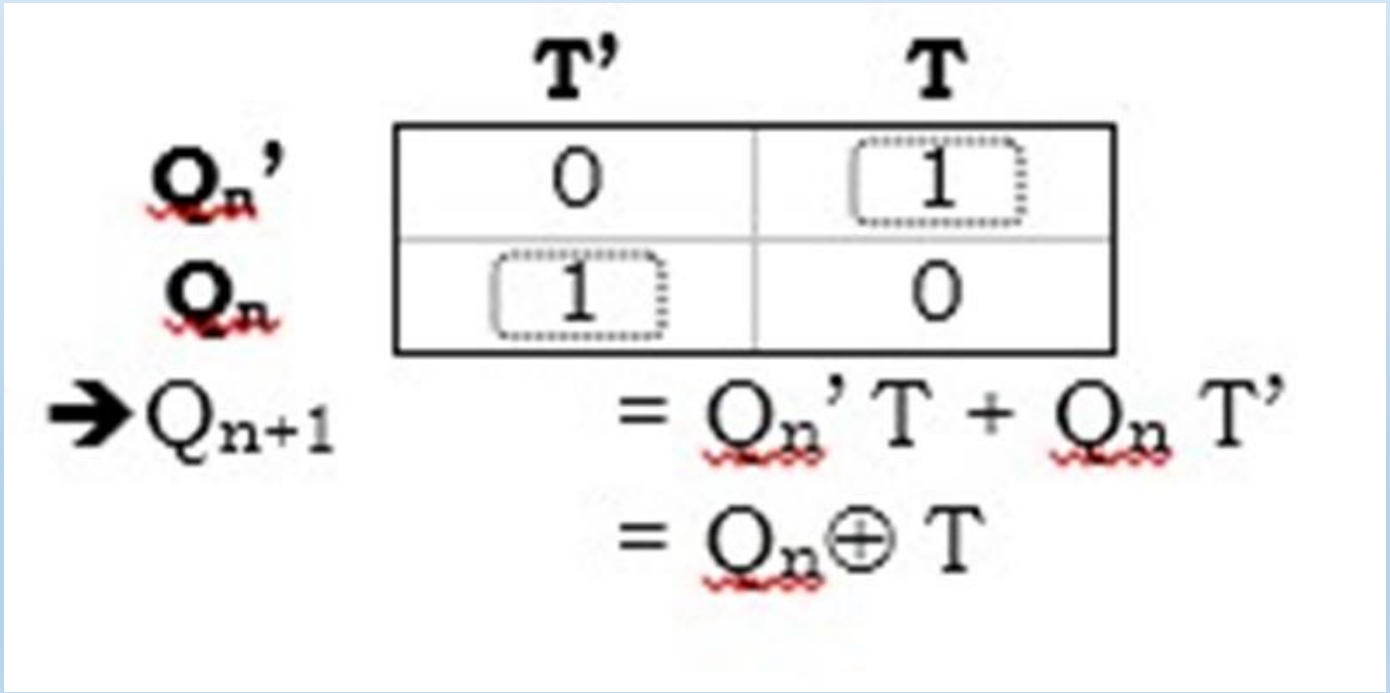
Clk	T	Q_{n+1}
0	X	Q_n(Memory)
1	0	Q_n(Memory)
1	1	Q_n'



- Toggle flip flop is basically a JK flip flop with J and K terminals permanently connected together. It has only input denoted by **T** as shown in the Block Diagram given below.

Characteristic Table

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

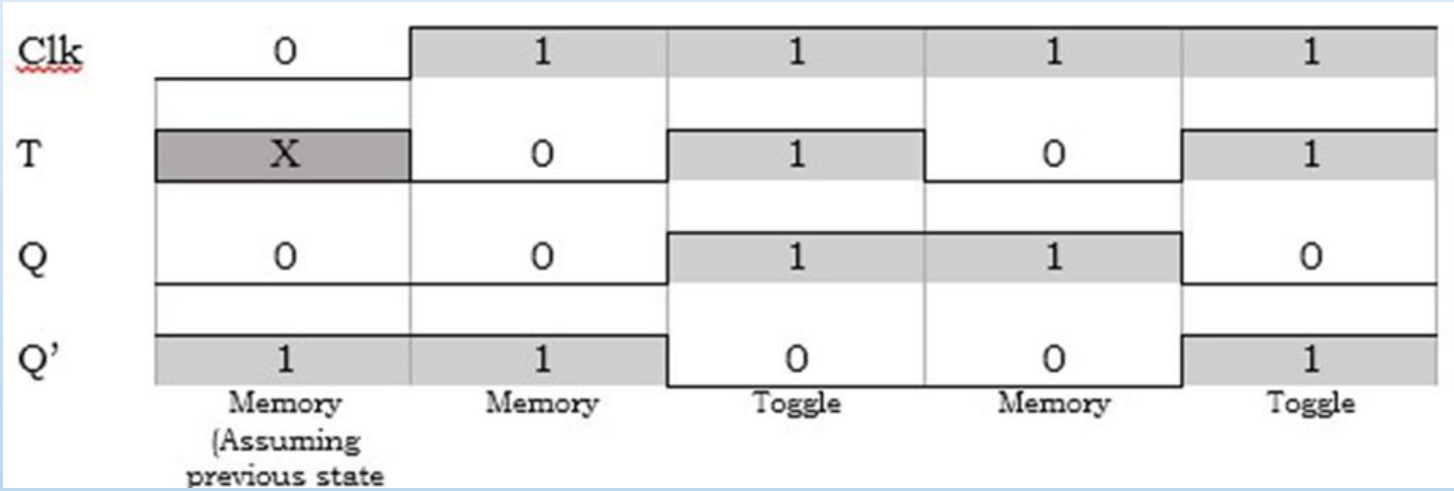


- Characteristic Eqaution

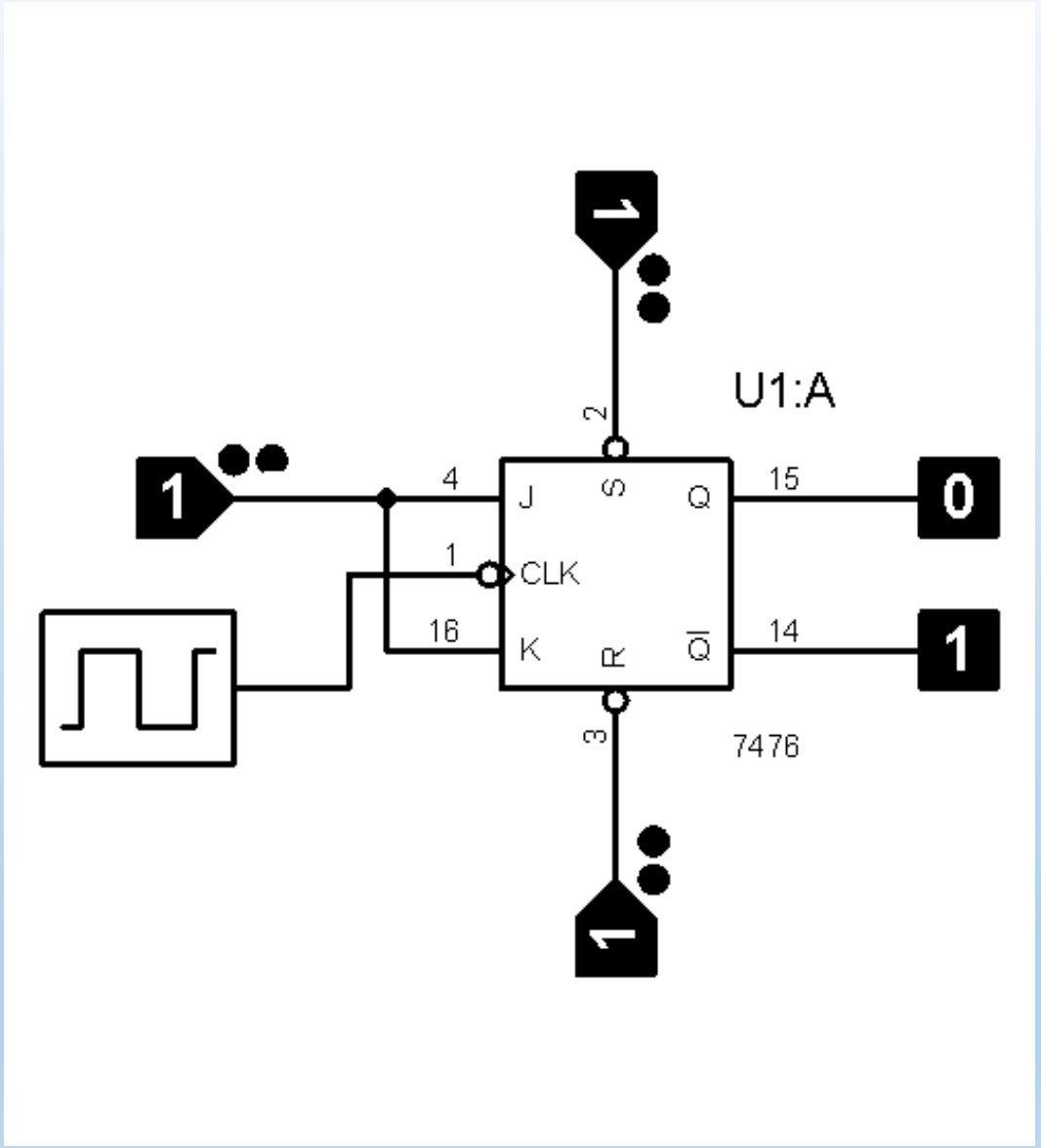
Excitation Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

- Timing Diagram T FlipFlop



T using 7476



JK FLIP FLOP

IC 7476

OBJECTIVES

- 1.To investigate and verify the property of JK flip flop using gates.
- 2.To investigate and verify the property of JK flip flop using7476 IC.
- 3.To know about direct inputs(preset/clear) using 7476 IC.
- 4.To know about methods of triggering flip flops.

JK Combinations

- •**Case 1**
- At J=0 and K=0 the condition remains unchanged.
- •**Case 2**
- At J=1 and K=0 when the flip flop receives
- Clk pulse Q goes or stays HI and Q’ goes or stays LO . In other words the 1 on the J input is passed directly to Q output.
- •**Case 3**
- At J=0 and K=1 when there is clk pulse 1 in K input is passed directly to Q’ output.
- •**Case 4**
- At J=1 k=1 flip flop toggles at each clock pulse.

JK table

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

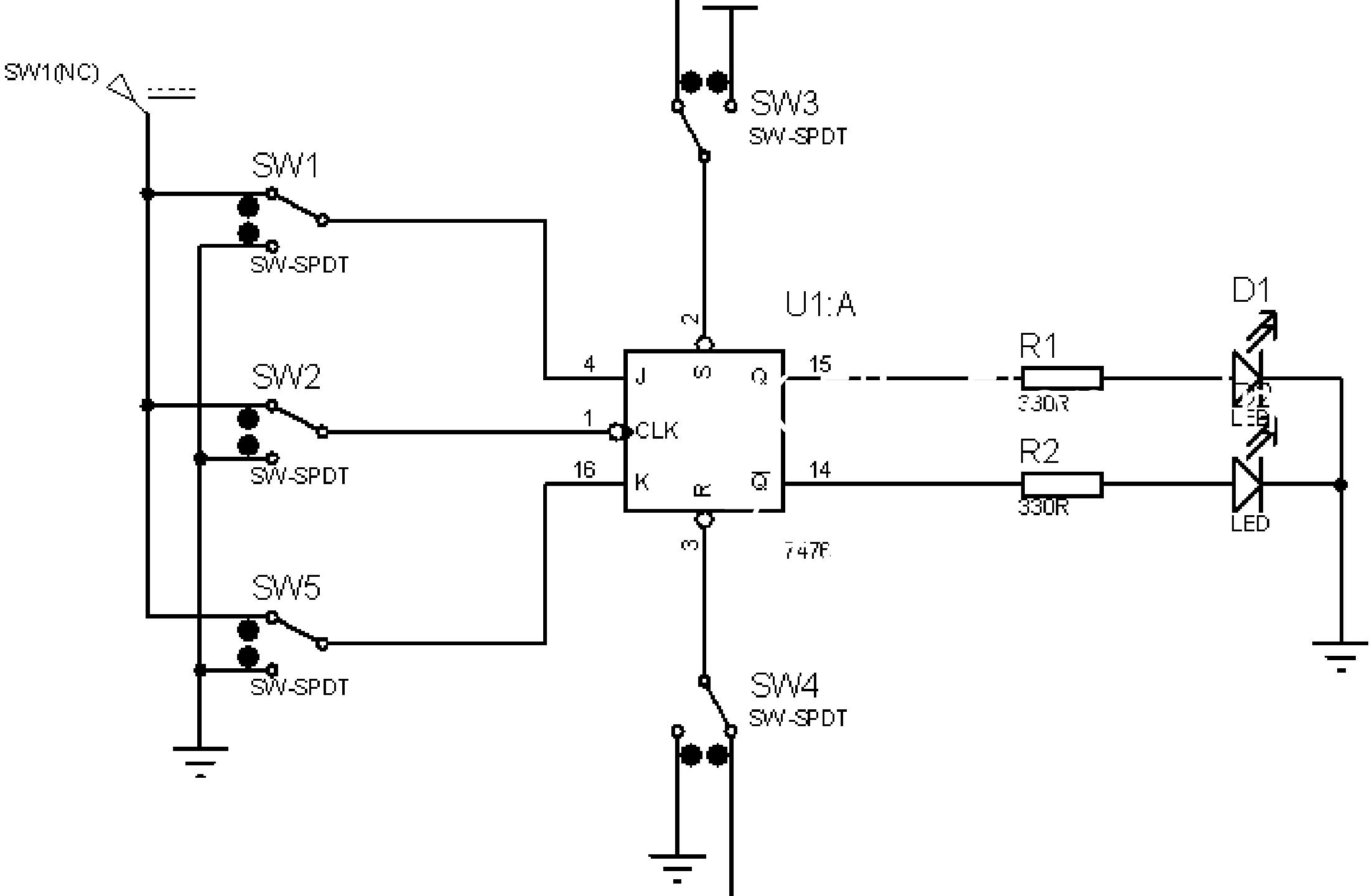
	J'K'	J'K	JK	JK'
Q'_N	0	0	1	1
Q	1	0	0	1

Characteristic Equation for JK Flip Flop

- $Q_{N+1} = JQ'_n + K'Q_N$

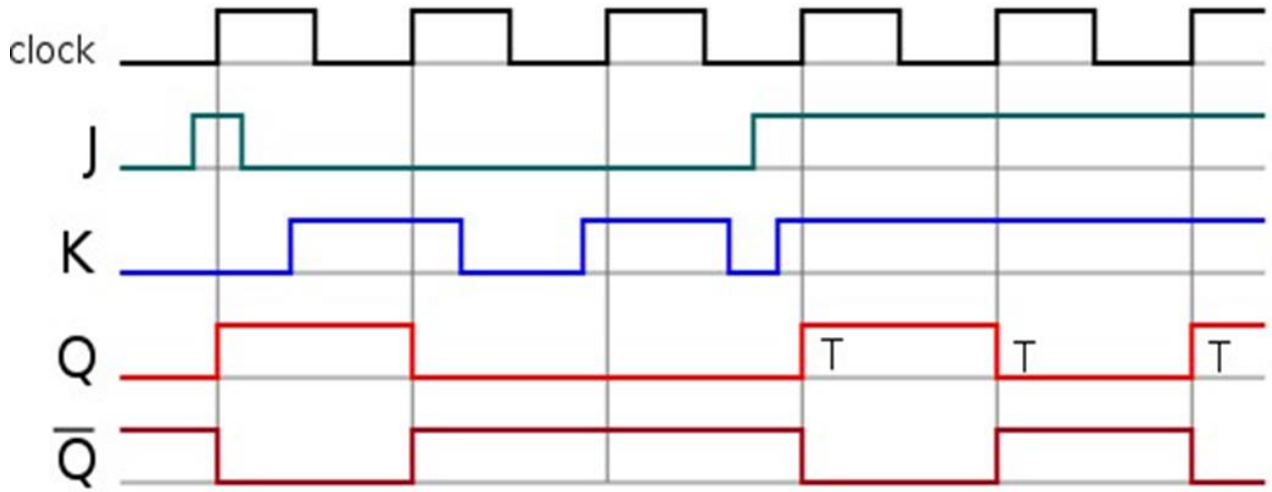
Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0


SW1(NC)
SW1
SW-SPDT
SW2
SW-SPDT
SW5
SW-SPDT
SW3
SW-SPDT
SW4
SW-SPDT
U1:A
4
J
2
S
Q
15
1
CLK
16
K
3
R
Q
14
74?P
R1
330R
R2
330R
D1
LED
LED

JK flip flop With Preset and Clear

J	K	Preset	Clear	Q_n	Q_{N+1}
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	1	1	0	0
0	1	1	1	1	0
1	0	1	1	0	1
1	0	1	1	1	1
1	1	1	1	0	1
1	1	1	1	1	0

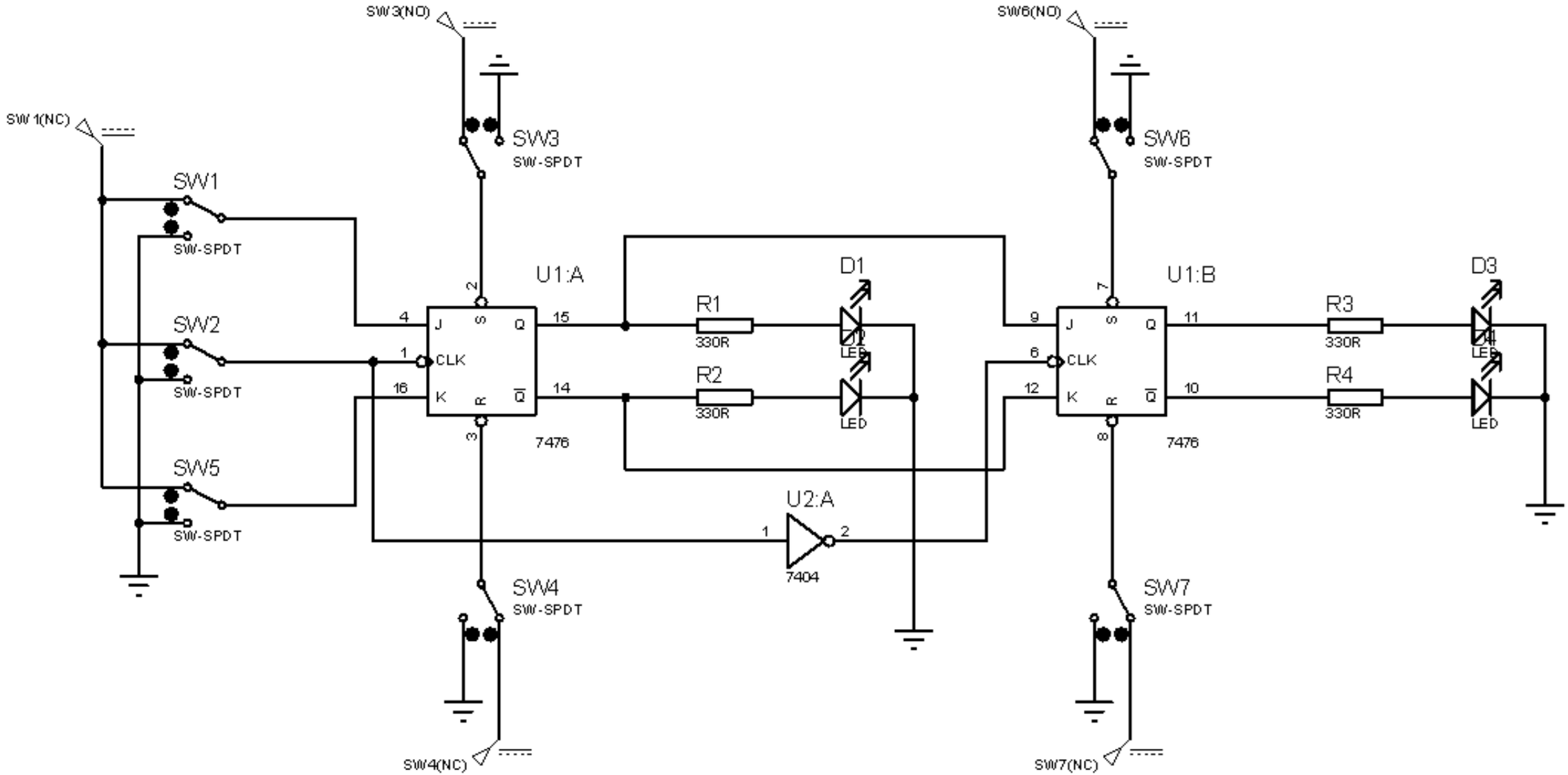


JK Flip Flop Timing Diagram

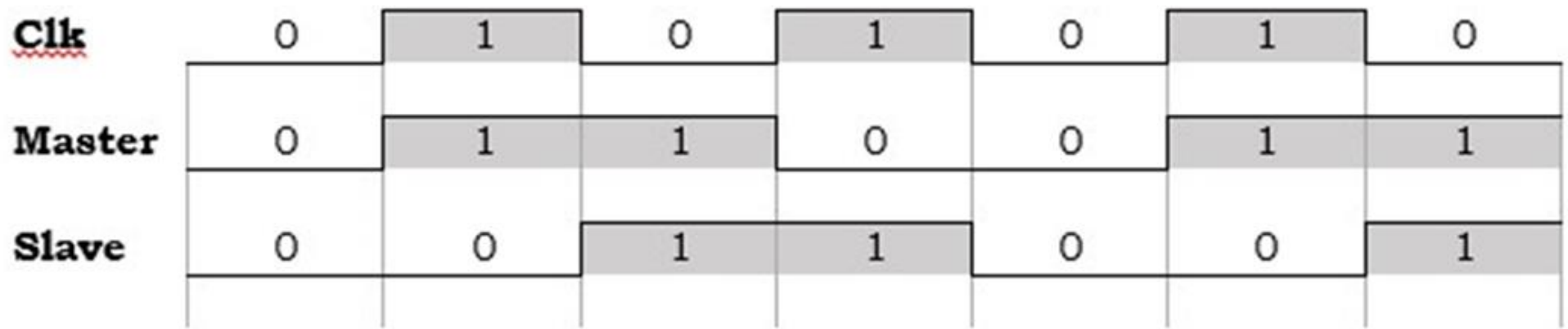
JK Master Slave

Using 7474

- The JK master/slave flip-flop is also known as the pulse triggering flip-flop. The circuit accepts input data when clock signal is high and passes the data to the output on the falling edge of the clock signal.
- They are composed of two sections: master and slave. The master section is basically a gated latch and slave section is same as master except that it is provided by inverted clock section rather by external JK input. The master section inputs at the leading edge of the clock pulse whereas, slave section inputs at the falling edge of a clock pulse.
- When Clk=1, the master J-K flip flop gets disabled. The Clk input of the master input will be the opposite of the slave input. So, the master flip flop output will be recognized by the slave flip flop only when the Clk value becomes 0. Thus, when the clock pulse males a transition from 1 to 0, the locked outputs of the master flip flop are fed through to the inputs of the slave flip-flop making this flip flop edge or pulse-triggered.


SW1(NC)
SW3(NO)
SW6(NO)
SW1
SW-SPDT
SW2
SW-SPDT
SW5
SW-SPDT
SW3
SW-SPDT
SW6
SW-SPDT
U1:A
U1:B
J
S
Q
CLK
K
R
Q
7476
R1
330R
R2
330R
R3
330R
R4
330R
D1
D2
D3
D4
LED
U2:A
7404
SW4
SW-SPDT
SW7
SW-SPDT
SW4(NC)
SW7(NC)

JK Master Slave Timming Diagram


Clk
0
1
0
1
0
1
0
Master
0
1
1
0
0
1
1
Slave
0
0
1
1
0
0
1