Register

- Register is a type of memory element that store the data.
- Register has the combination of flip-flops.
- In order to increase the storing capacity of the register, the number of flip-flops used must be increased.
- The n-bit register consists of n number of flip-flops and is capable of storing n-bit words.
- The D flip-flop is used to make register as it gives same output as input.

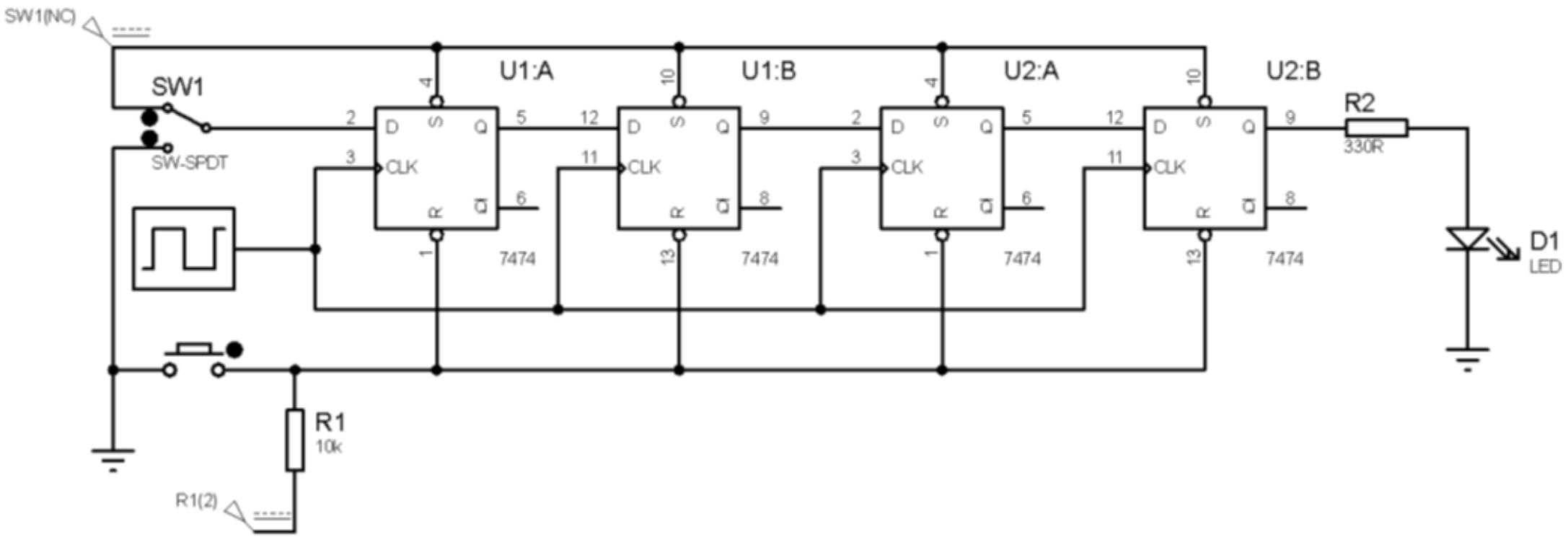
Shift Register

- Shift registers are a type of sequential logic circuit, mainly for storage of digital data.
- They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop.
- All flip-flop is driven by a common clock, and all are set or reset simultaneously.
- There are two ways to shift data in to register and out of it, either serial or parallel.
- The SERIAL SHIFTING method shift one bit at a time for each clock.
- In PARALLEL SHIFTING all data gets shifted simultaneously.

Types of Shift register

- Depending on the method of entering data and data retrieving process, it can be divided in four classes. They are as follows:
- **SISO (Serial In Serial Out)**
- **SIPO (Serial In Parallel Out)**
- **PIPO (Parallel In Parallel Out) / Buffer**
- **PISO (Parallel In Serial Out)**

Construction of 4-bit SISO register (Right shift)



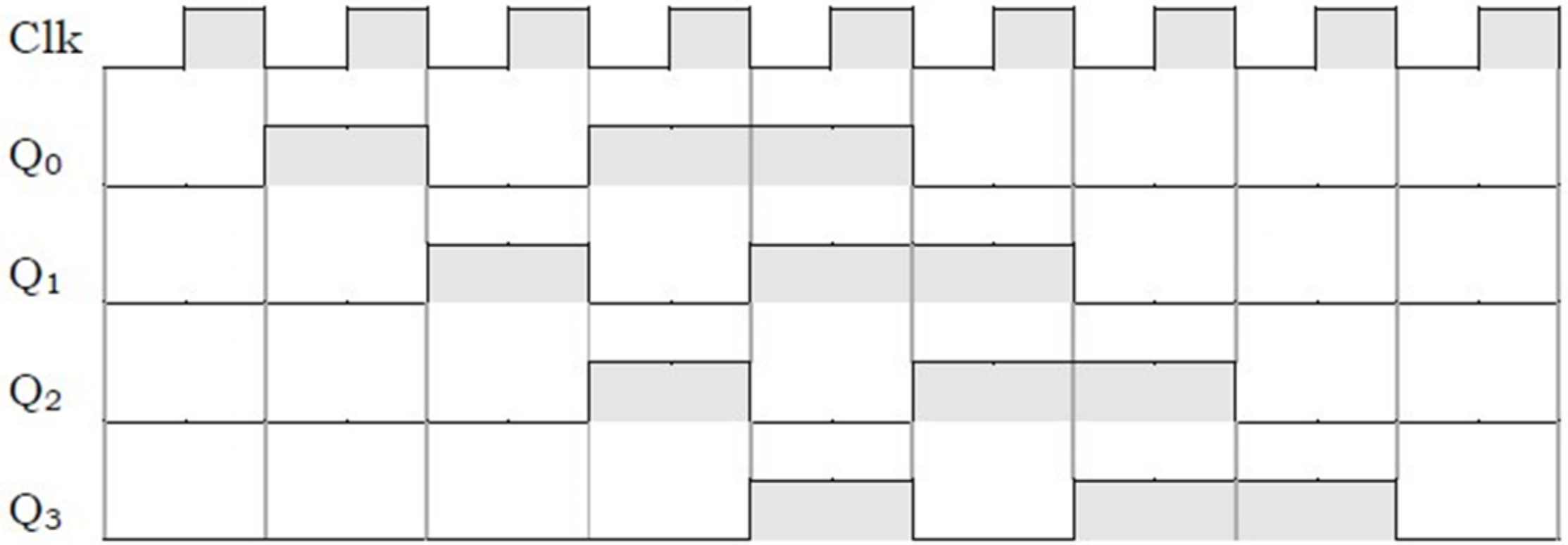
Functional Table

- Let the desired data to be operated be 1101, then the functional table and timing diagram of the circuit will be:

Functional Table

Clk	Q_0	Q_1	Q_2	Q_3	
0	0	0	0	0	
1	1	0	0	0	
2	0	1	0	0	
3	1	0	1	0	
4	1	1	0	1	→Data entered serially
5	0	1	1	0	1
6	0	0	1	1	0 →Data out serially
7	0	0	0	1	1
8	0	0	0	0	1

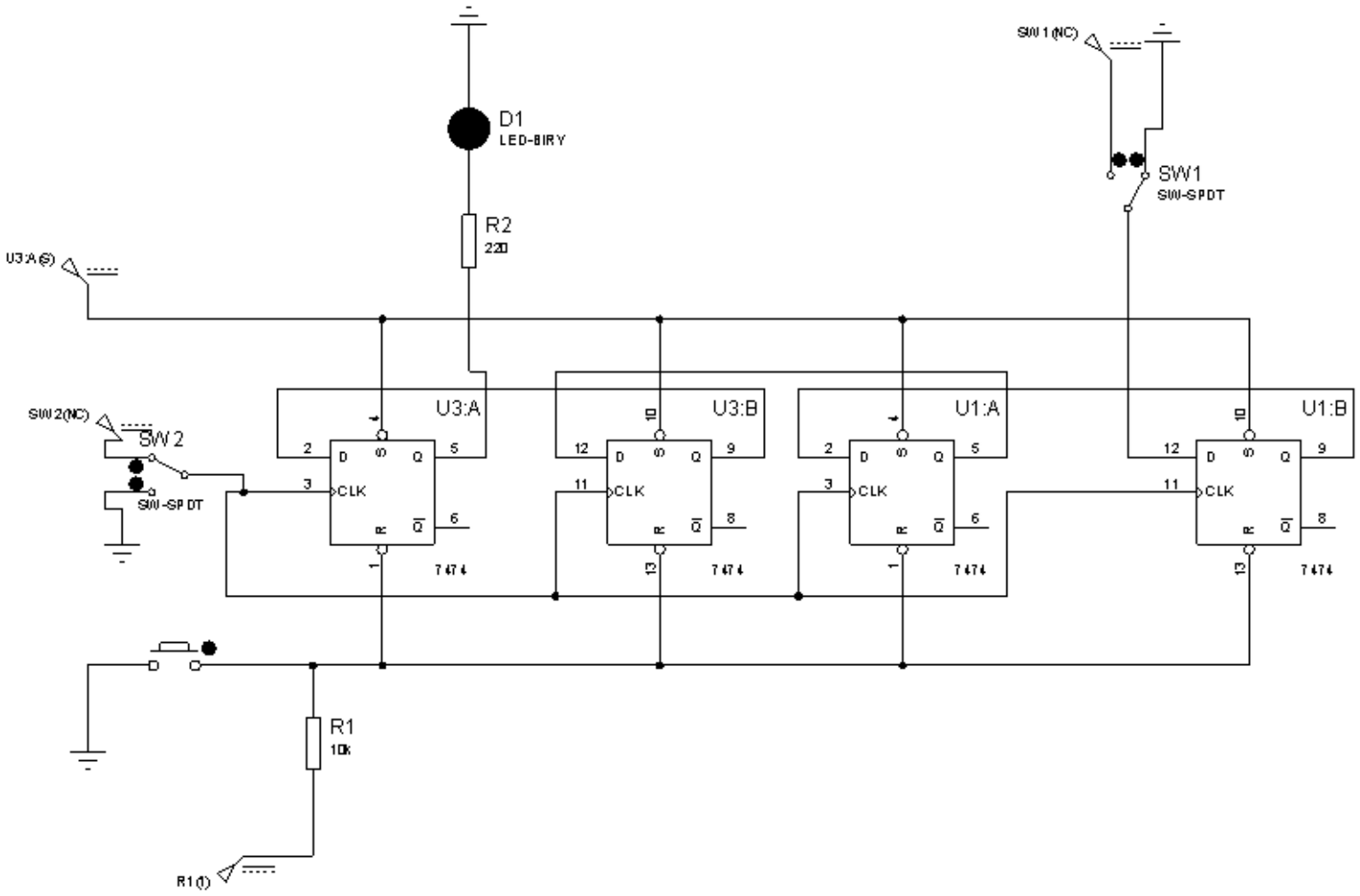
SISO Right Shift timing Diagram



SISO Description

- The above register accepts 4-bit data serially form the LSB.
- 4-clock pulses are required to enter the data and then the data are shifted towards right.
- The data firstly stored in the 1st flip-flop gets shifted to the next flip-flop, all the way till the 4th flip-flop.
- This process is repeated with all the inputs.
- The out put is then released from the rightmost bit i.e. MSB, serially.

Construction of 4-bit SISO register (Left shift)

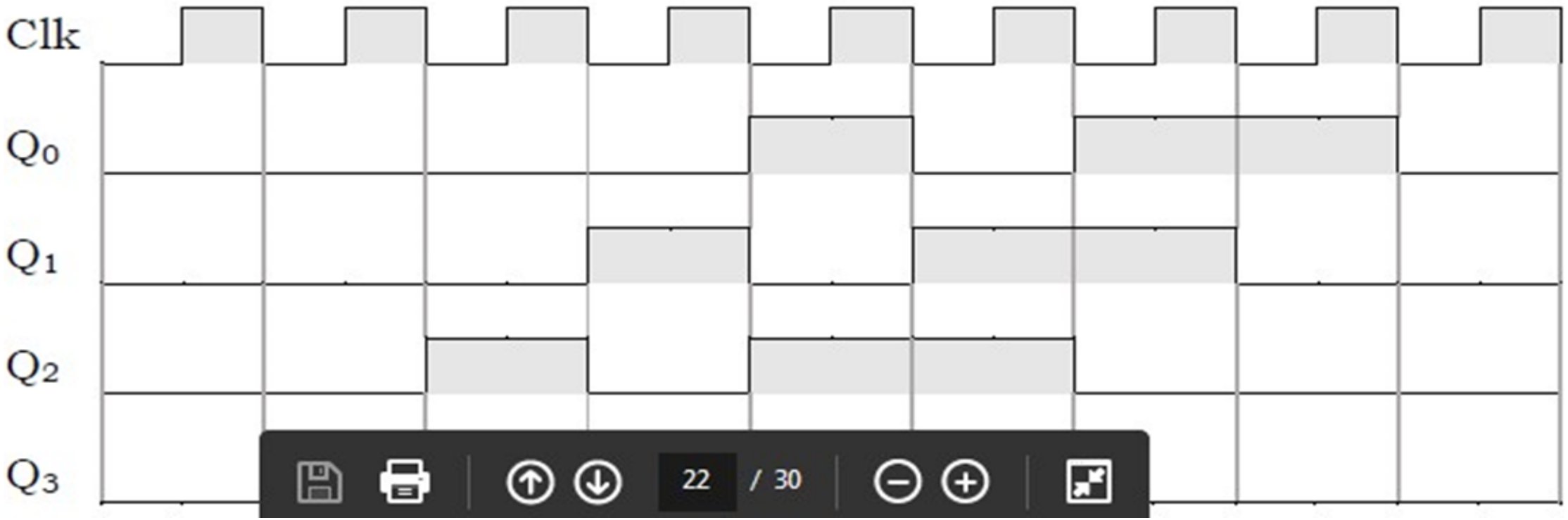


Functional Table (Left Shift)

Functional Table

	Clk	Q_0	Q_1	Q_2	Q_3	
	0	0	0	0	0	
	1	0	0	0	1	
	2	0	0	1	0	
	3	0	1	0	1	
	4	1	0	1	1	→Data
1	5	0	1	1	0	entered
0	6	1	1	0	0	serially
1	7	1	0	0	0	
1	8	0	0	0	0	

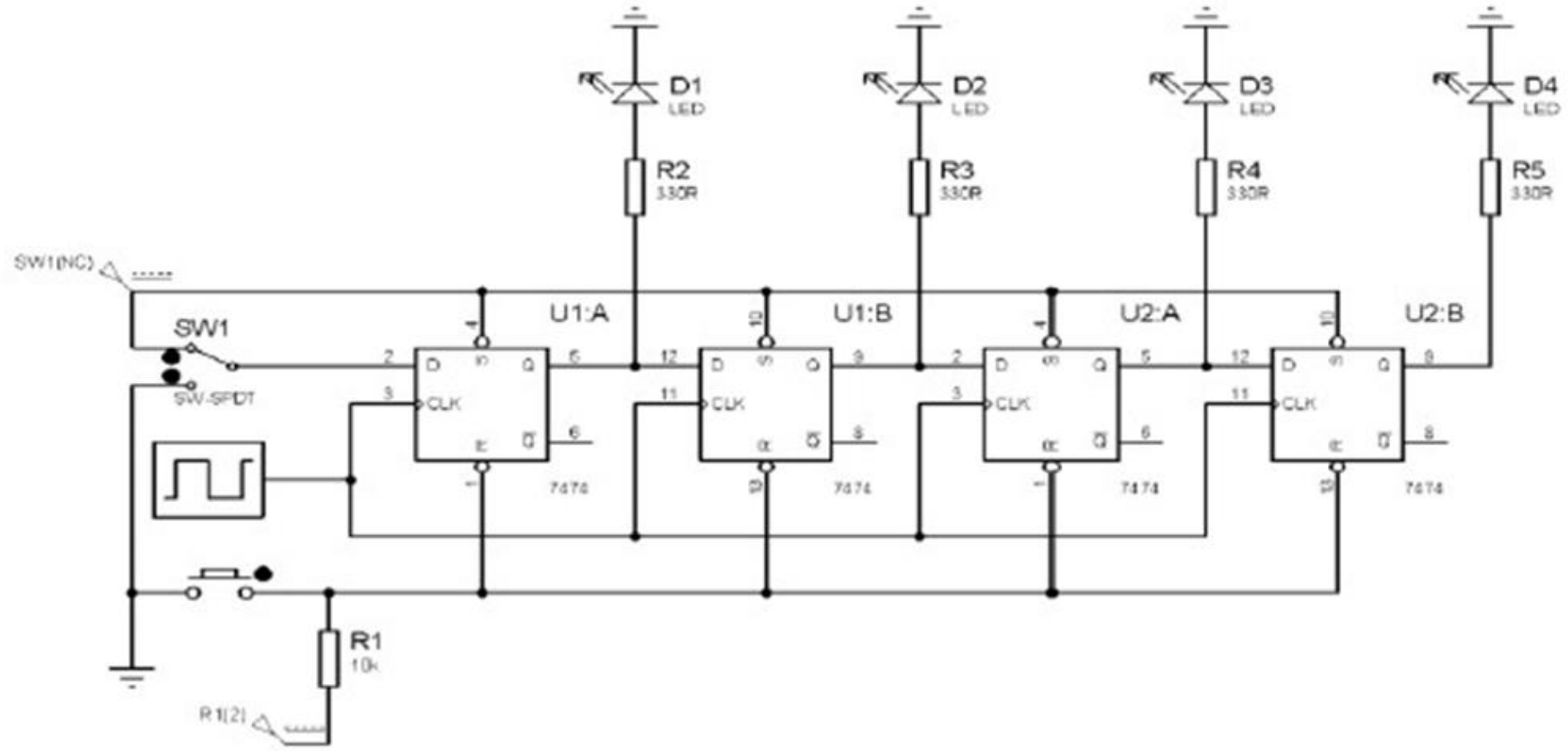
Timing Diagram Left Shift



SIPO (Serial In Parallel Out)

- In this kind of register, data bits are entered serially in the same manner as in the SISO registers.
- The difference is the way in which the data bits are taken out of the register.
- Once the data are stored, each bit appears on its respective output line .
- All bits are available simultaneously.

SIPO Practical Logic Diagram



SIPO Description

- In SIPO register 4-bit data are entered simultaneously like in the SISO.
- The data are shifted towards the left until the final bit of the data is entered.
- Once the entering and storing process is over, the data can be retrieved all at once .
- Then the data appears on the own output lines parallel.

Functional Table

- Let the desired data to be operated be 1101, then the functional table and timing diagram of the circuit will be:

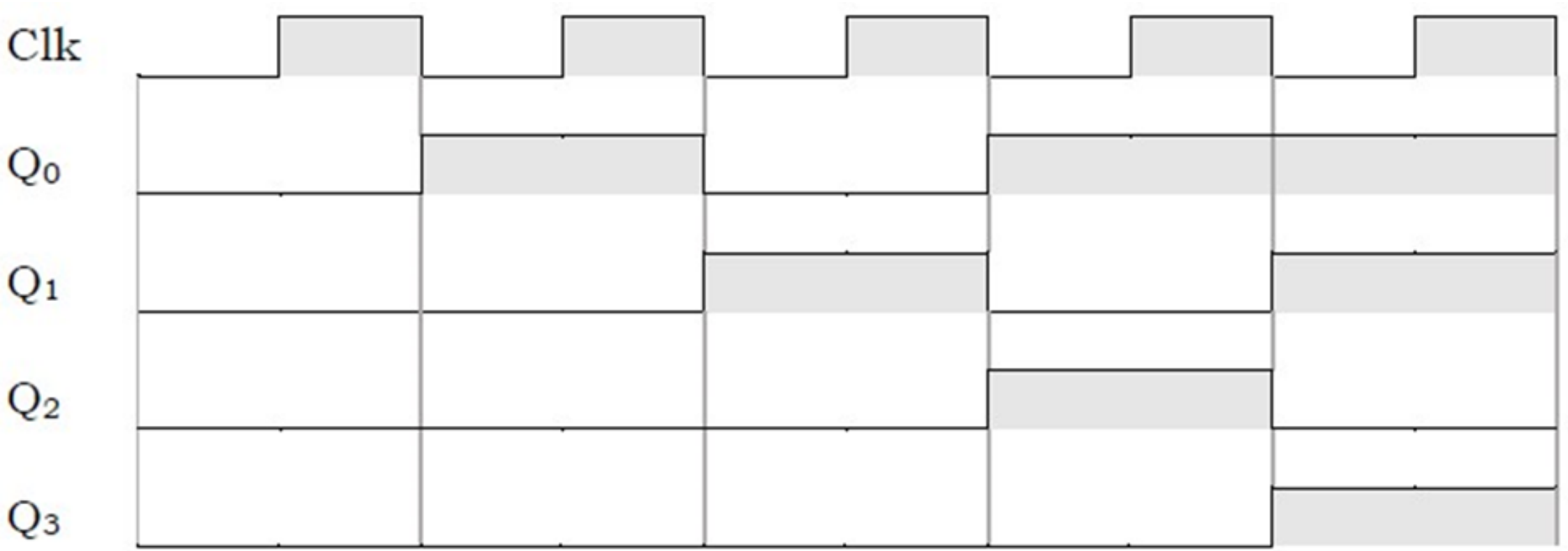
Functional Table

Clk	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	1	1	0	1
	1	1	0	1

→Data entered serially

Data taken out parallelly

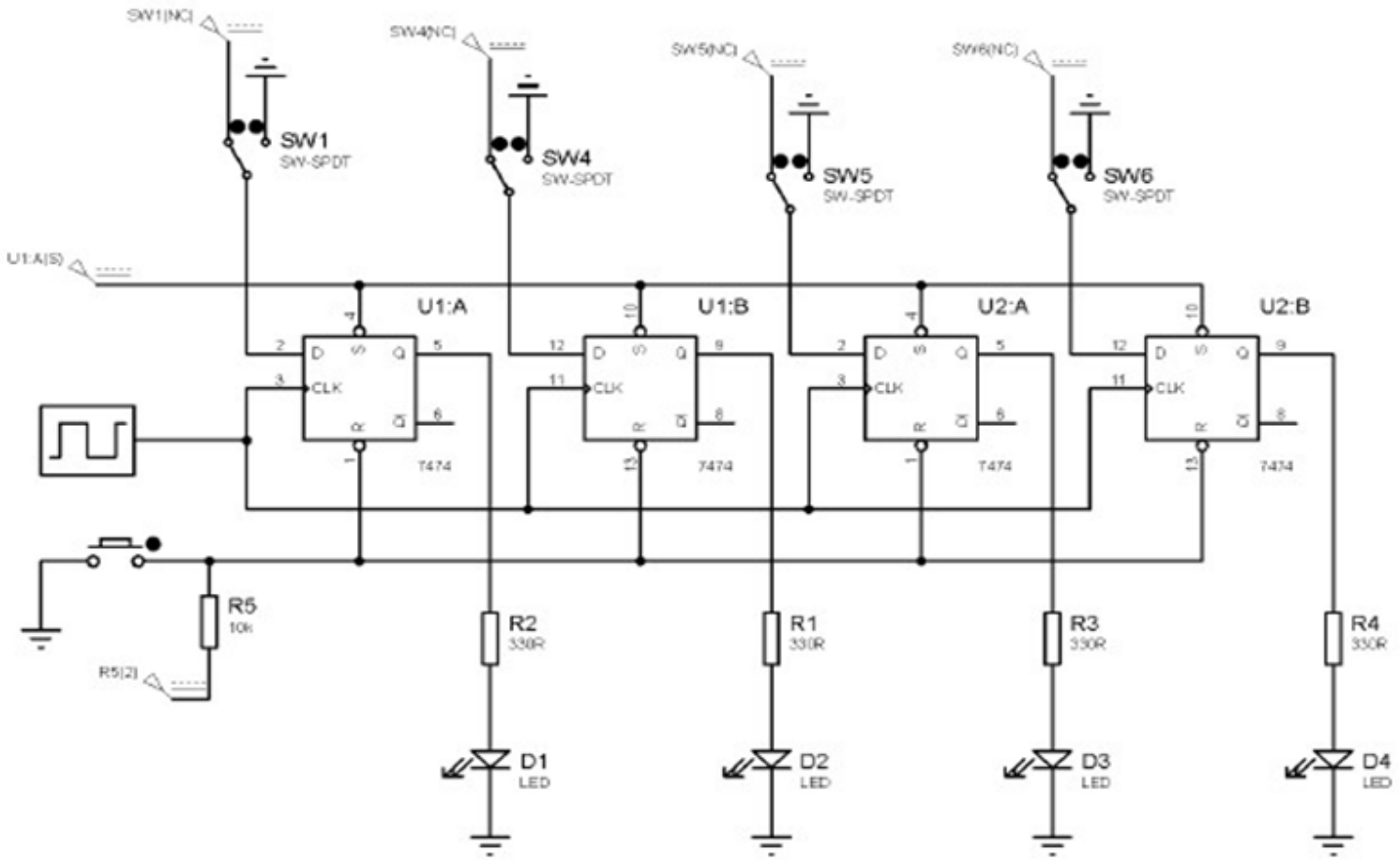
Timing Diagram



PIPO (Parallel In Parallel Out) / Buffer

- In this register, the input is given in parallel and the output also collected in parallel.
- The clear (CLR) signal and clock signals are connected to all the 4 flip flops.
- Data is given as input separately for each flip flop and in the same way, output also collected individually from each flip flop.
- This type of shift register also acts as a temporary storage device or as a time delay device

PIPO Practical Logic Diagram



PIPO Description

- In the above register, the inputs are given parallelly all at once and the outputs are also retrieved all at once.
- Once the register is clocked, all the data at the inputs appear at the corresponding outputs simultaneously.
- Let the desired data to be operated be 1101, then the functional table and timing diagram of the circuit will be:

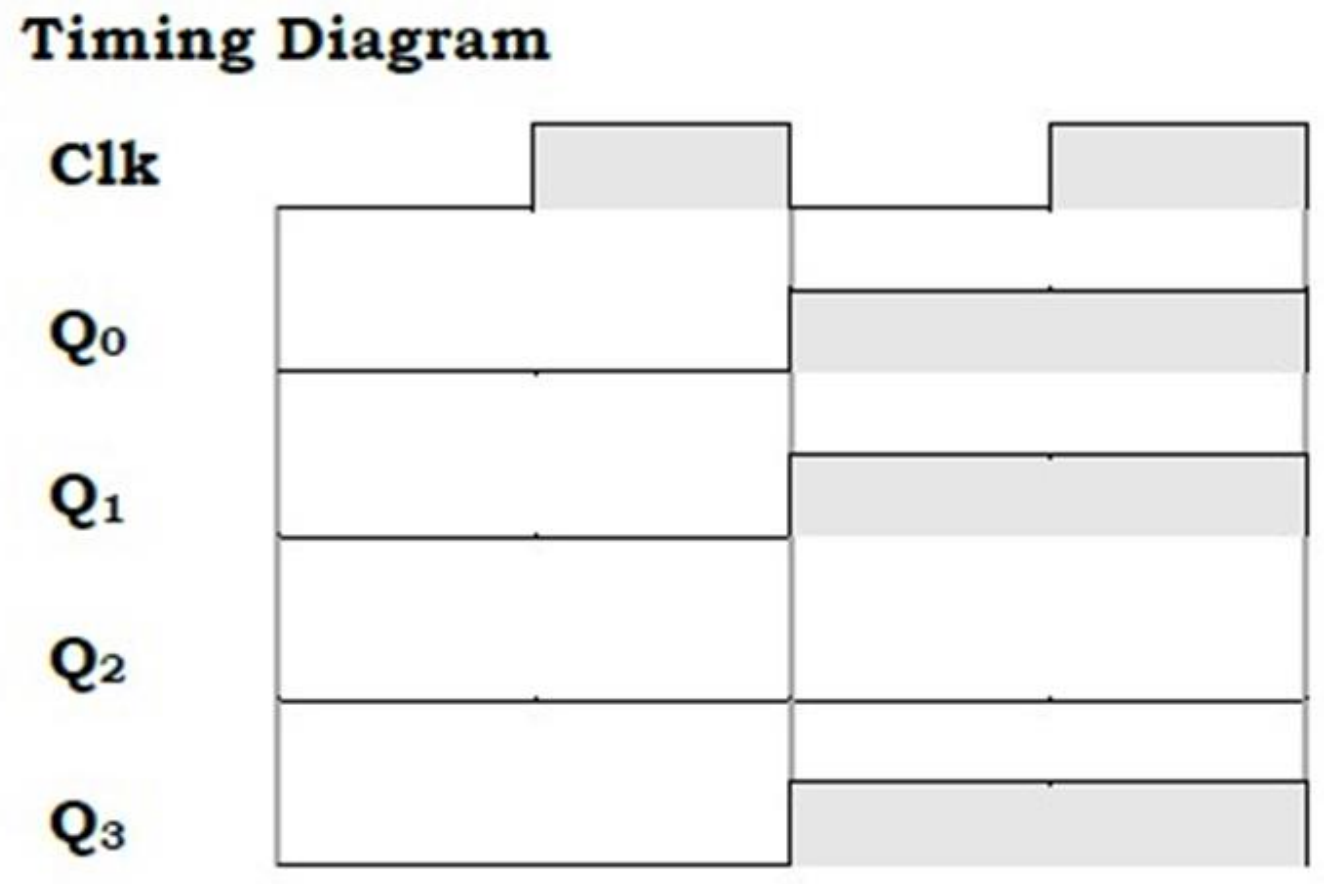
- PIPO Functional Table

Functional Table

Clk	Q_0	Q_1	Q_2	Q_3	
0	0	0	0	0	
1	1	1	0	1	→Data in parallelly
	1	1	0	1	

Data out parallelly

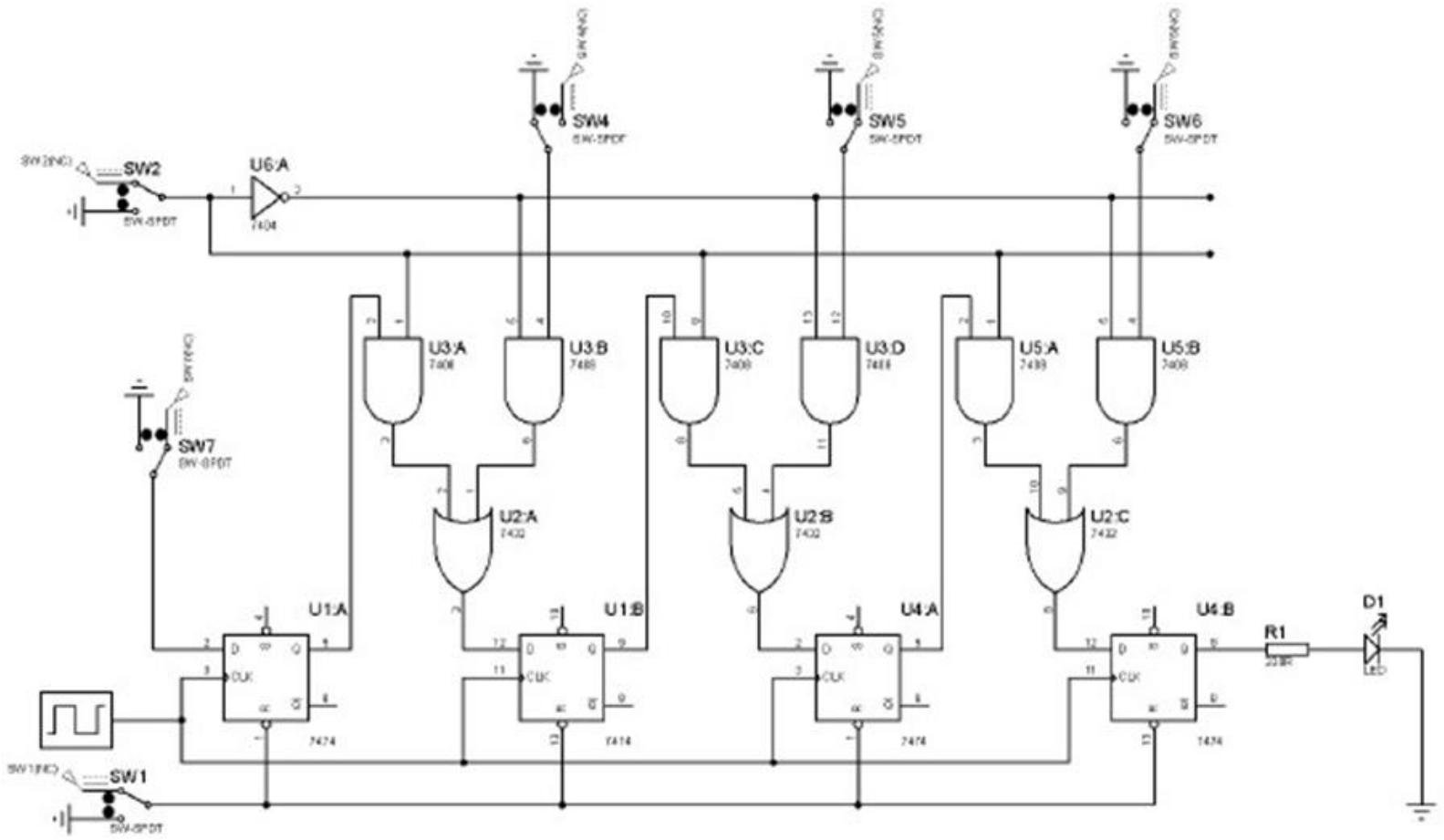
Timing Diagram



PISO (Parallel In Serial Out)

- In parallel in - serial out shift registers, all data bits are loaded on the flip-flops immediately .
- However, the outputs are retrieved bit by bit.
- The data once stored in the flip-flops starts to shift in the adjacent flip-flop and the data are retrieved from the LSB.
- In order to make the circuit load the data and shift them, mode control input (shift/load') is used .
- which directs the circuit whether to parallelly load the data or serially shift them with the help of combination circuit.
- This combinational circuit consist of a pair of AND gates connected to the OR gate .

PISO Practical logic Diagram



PISO Description

- In the above circuit, firstly the control input is made low.
- Then the AND gate connected with the input signals get active passing the user's input to the flip-flop.
- Once the input process is over, the control input is made high.
- Then the AND gate connected with the output of previous flip-flop gets active allowing the outputs of the flip-flops to pass to the next flip i.e. shift towards next flip-flop.
- Through this shifting process, the data is retrieved bit by bit in a single line.

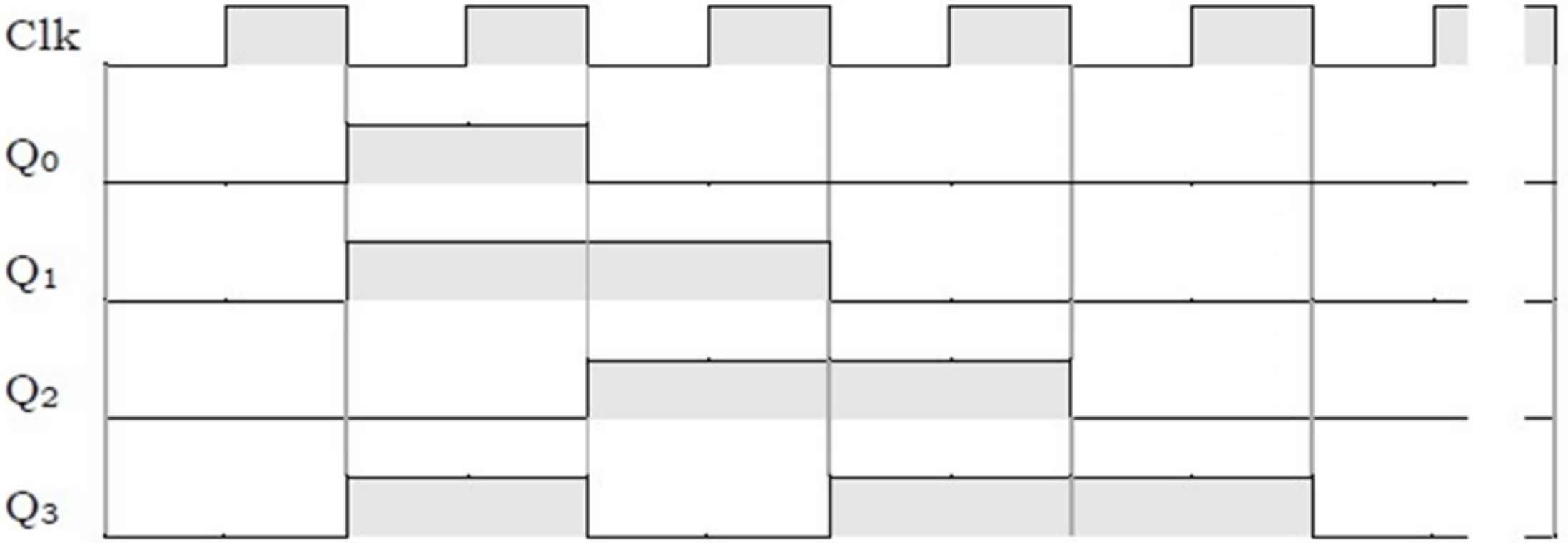
Functional Table

- Let the desired data to be operated be 1101, then the functional table and timing diagram of the circuit will be:

Functional Table

Clk	Q_0	Q_1	Q_2	Q_3	
0	0	0	0	0	
1	1	1	0	1	←Data entered parallelly
2	0	1	1	0	1
3	0	0	1	1	0 ←Data taken out serially
4	0	0	0	1	1
5	0	0	0	0	1

PISO Timing Diagram



Shift Register Counter

- Two of the most common types of shift register counters are the Ring counter and the Johnson counter.
- They are basically shift registers with the serial outputs connected back to the serial inputs .
- In order to produce particular sequences.
- These registers are classified as counters because they exhibit a specified sequence of states.

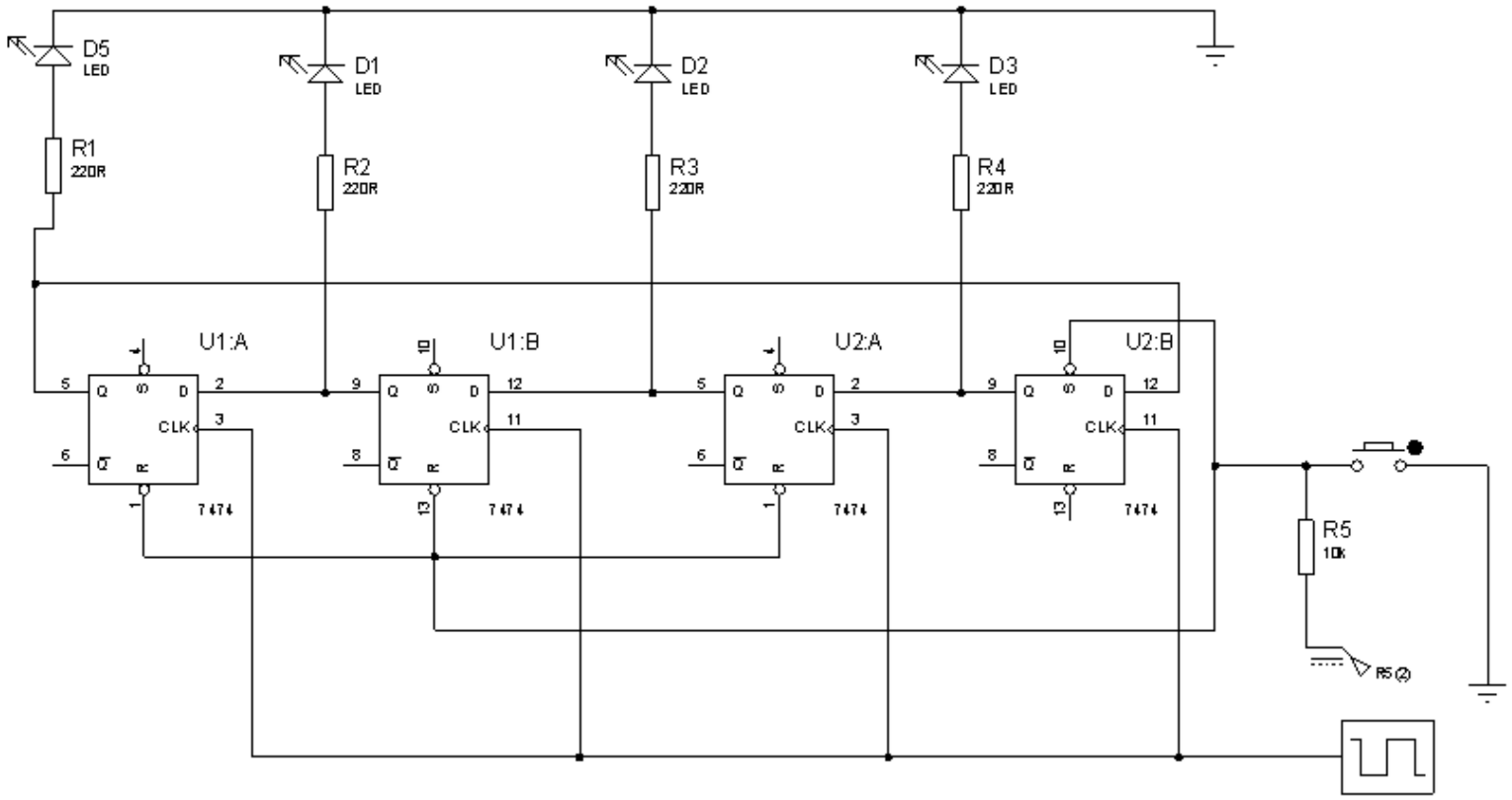
Ring Counter

- This circuit is basically a circulating shift register.
- The data moves in a ring.
- The output of the most significant stage i.e. last flip-flop is fed back to the input of the least significant stage i.e. first flip-flop.
- Initially before clock pulse, all the flip-flops except the first one are reset to 0 using clear and the first flip-flop is preset to 1 instead.
- An n-stage Ring counter yields a count sequence of length n, so it may be considered to be a mod-n counter.

Ring Counter Description

- The below 4-bit ring counter is constructed from four D flip-flops.
- The clock is provided in synchronous way in negative edge.
- The output of each stage is shifted into the next stage on the negative edge of a clock pulse serially.
- Initially, the ORI button is pushed which triggers the preset of 1st flip-flop and clear of rest flip-flops .
- The main advantage of this type of counter is that it is self-decoding.
- No extra decoding circuit is needed to determine what state the counter is in.

Ring Counter Practical Diagram



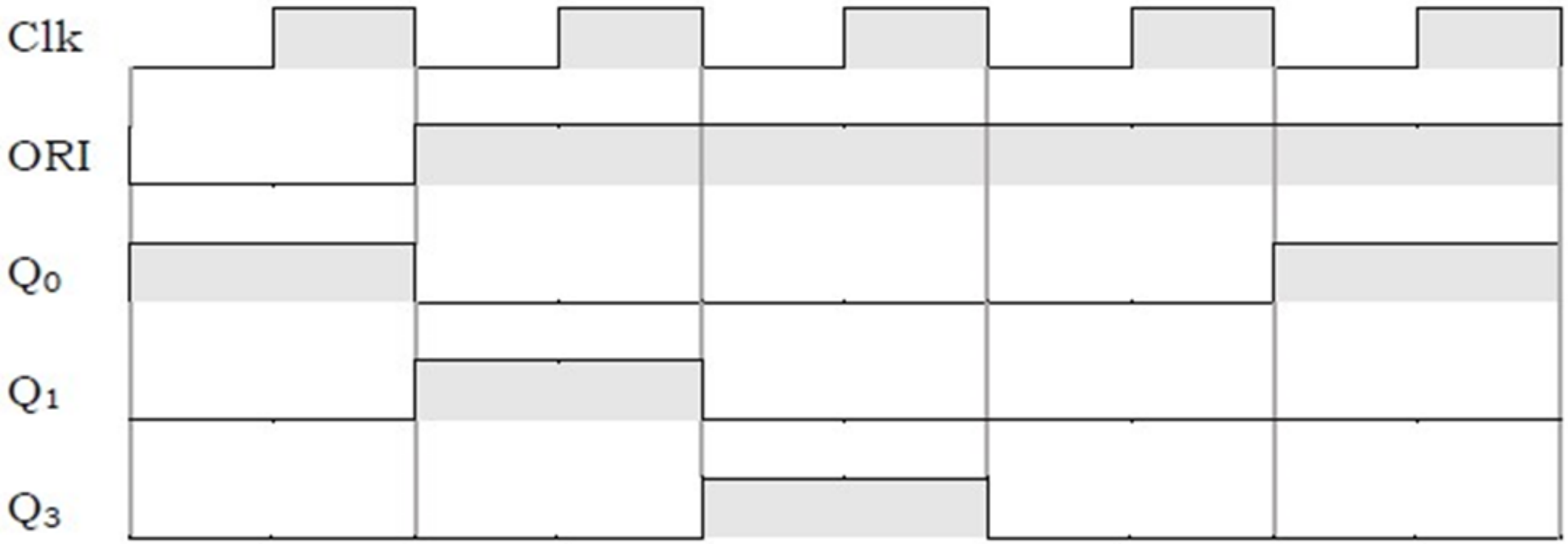
Functional Table

- •The functional table and timing diagram for the above 4-bit ring counter is as follows:

ORI	Clk	Q_0	Q_1	Q_2	Q_3
0	X	1	0	0	0
1	1	0	1	0	0
1	2	0	0	1	0
1	3	0	0	0	1
1	4	1	0	0	0

Timing Diagram

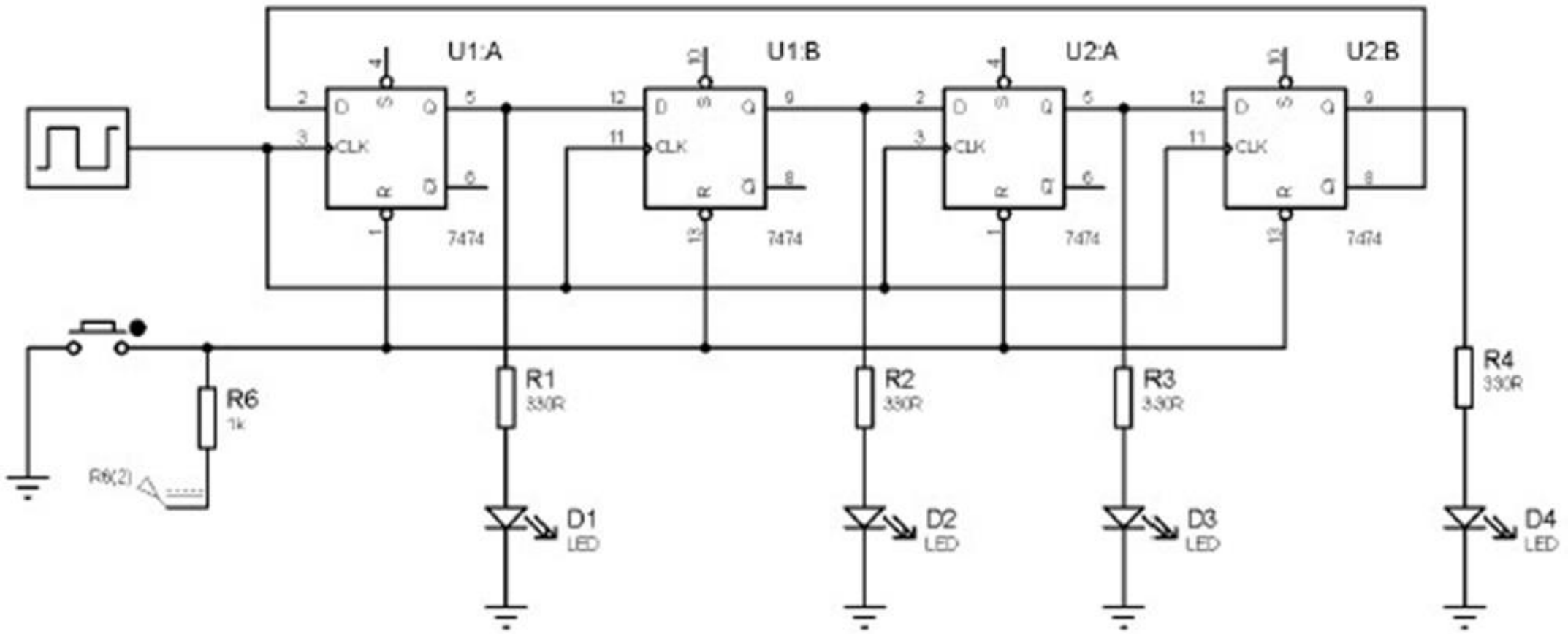
Ring Counter



Johnson Counter

- This circuit is also a circulating shift register.
- The data moves in a ring.
- These are a variation of standard ring counters, with the inverted output of the last stage fed back to the input of the first stage.
- They are also known as twisted ring counters.
- An n-stage Johnson counter yields a count sequence of length 2n, so it may be considered to be a mod-2n counter.

Johnson Counter Practical Logic Diagram



Johnson Counter description

- the above 4-bit Johnson counter is constructed from four D flip-flops.
- The clock is provided in synchronous way in negative edge.
- The output of each stage is shifted into the next stage on the negative edge of a clock pulse serially.
- Initially, the Clr button is pushed which triggers the clear of all flip-flops.
- This type of counter is also a self-decoding circuit.
- No extra decoding circuit is needed to determine what state the counter is in.

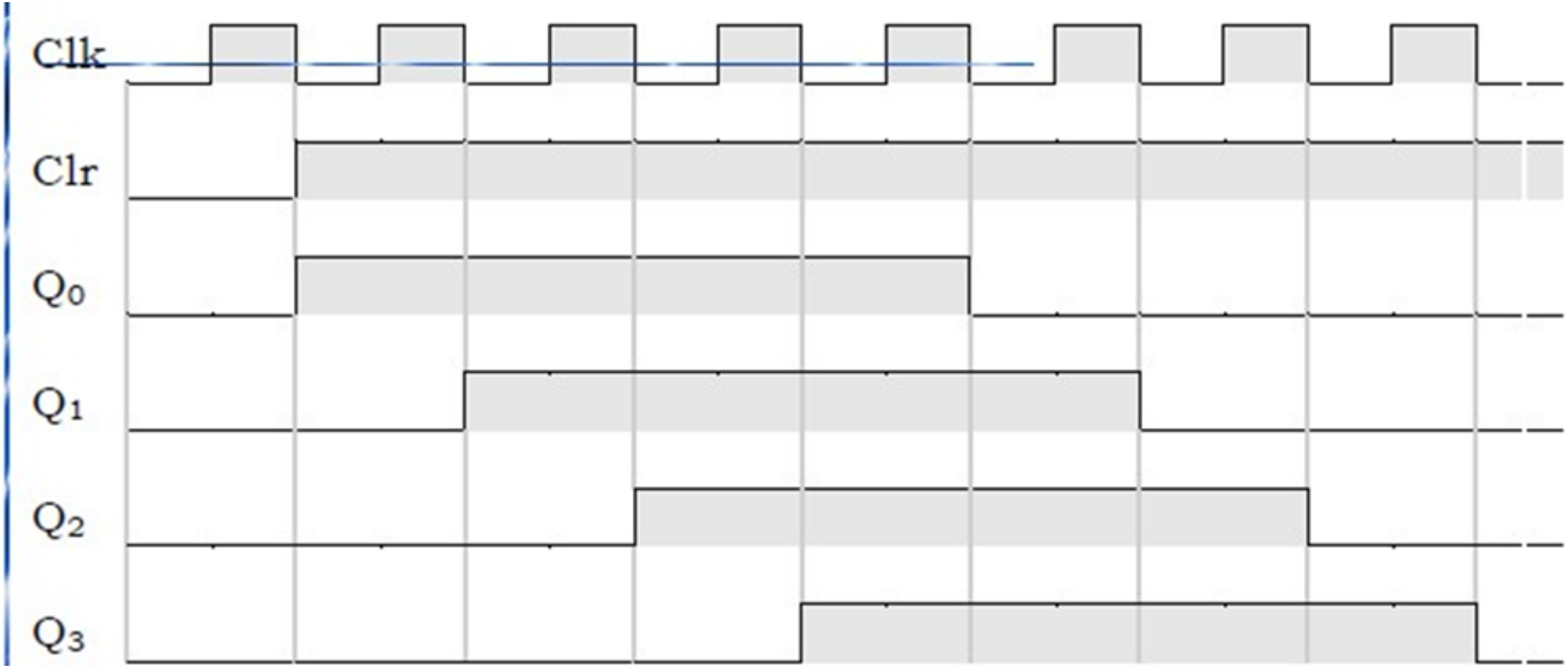
Functional Table

The functional table and timing diagram for the above 4-bit Johnson counter is as follows:

Functional Table

Clr	Clk	Q_0	Q_1	Q_2	Q_3
0	X	0	0	0	0
1	1	1	0	0	0
1	2	1	1	0	0
1	3	1	1	1	0
1	4	1	1	1	1
1	5	0	1	1	1
1	6	0	0	1	1
1	7	0	0	0	1

Timing Diagram



Applications of Shift Registers

Registers are used in digital electronic devices like computers as:

- ® Temporary data storage
- ® Data transfer
- ® Data manipulation
- ® As counters

Applications of Shift Registers (Contd)

- 1.Shift registers are used in computers as memory elements. All the digital systems need to store large amount of data, in an efficient manner; there we use storage elements like RAM and other type of registers.
- 2.Many of the digital system operations like division, multiplication, are performed by using registers. The data is transferred through serial shift registers and other type.

- Serial in – serial out registers are used for time delays.
- ® Serial in – parallel out registers are used for converting the data from serial form to parallel form.
- ® Parallel in – serial out registers are used for converting the data from parallel form to serial form.