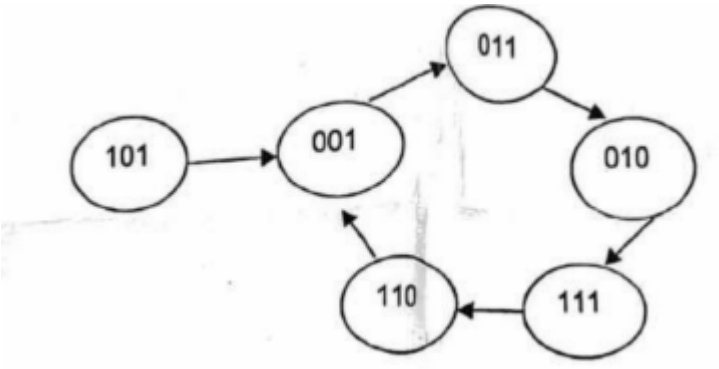
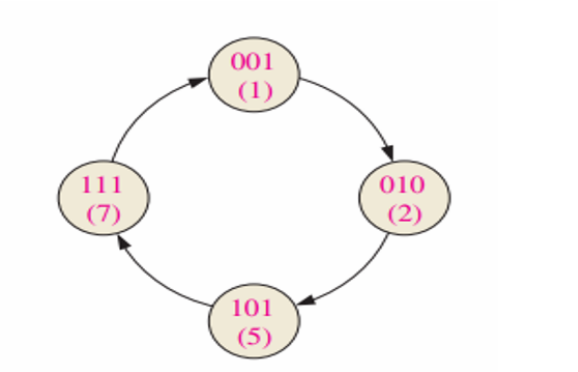
## Unit 6 (Assignment)/ BIM 2nd / Digital Logic

1. Compare the logic of synchronous counter and ripple counter.
2. Design a counter as shown in the state diagram below




3. Design a counter with the irregular binary count sequence as shown in the below state diagram. Use D flip-flops.




4. Describe about some application of counter and register in digital system. Design Decade counter using JK Flip-Flop.
5. Explain the Mealy and Moore models of Finite State Machines.
6. Explain briefly SISO, SIPO, PISO and PIPO register with its circuit diagram and working.