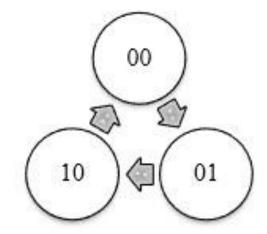
Mod Counter

- Binary counter previously introduced have 2n states.
- counters with states less than this number are also possible.
- These sequences are achieved by forcing the counters to recycle before going through all of its normal states.
- A common modulus for counter with truncated sequence is 10.
- A counter with 10 states in its sequence is called decade counter.

Verification of MOD-3 ripple up counter

- Flip-Flop used = JK
- No. of FF used = 2
- Total no. of states = 3
- Maximum count = 2

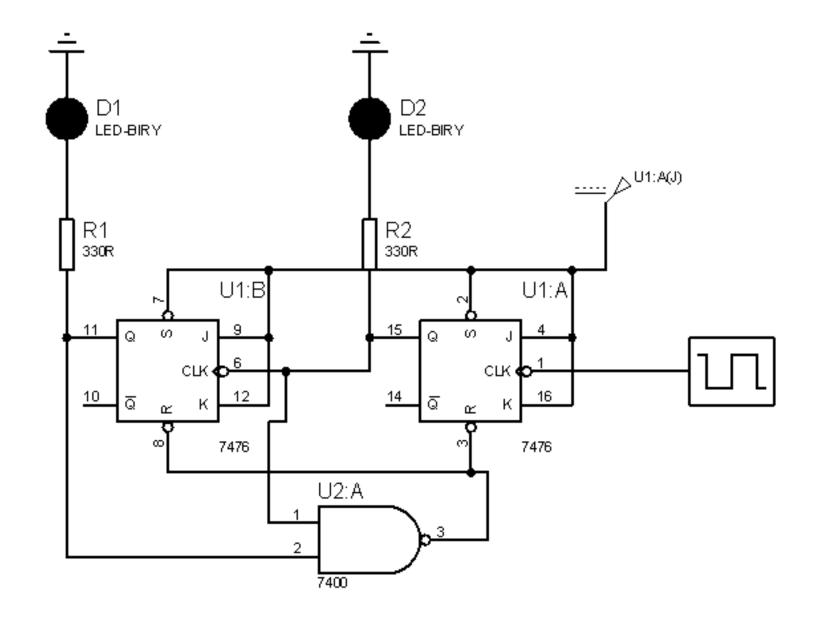


State Diagram Of Mod 3 ripple up counter

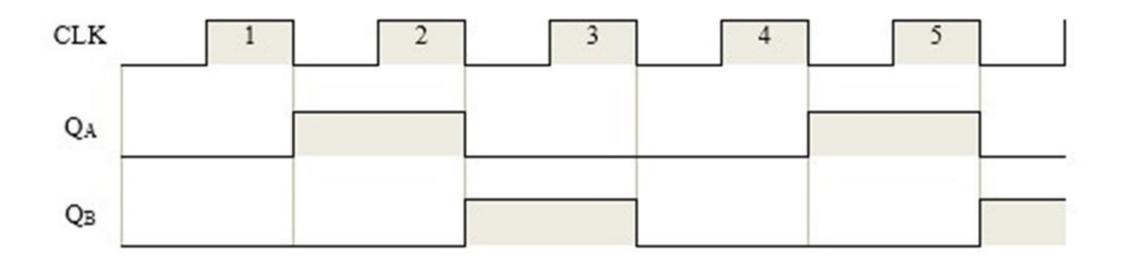
Count Sequence Table

Q_B	Q_A	D. E.
0	0	0
0	1	1
1	0	2
1	1	3

Practical
Logic
Diagram
(Mod 3 up
Counter)



Mod 3 up counter Timing Diagram



Verification of MOD-6 ripple up counter

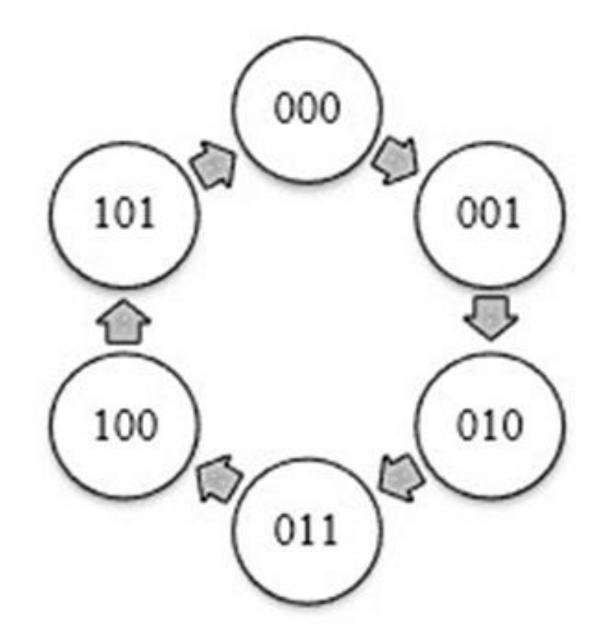
•Flip-Flop used = JK

•No. of FF used = 3

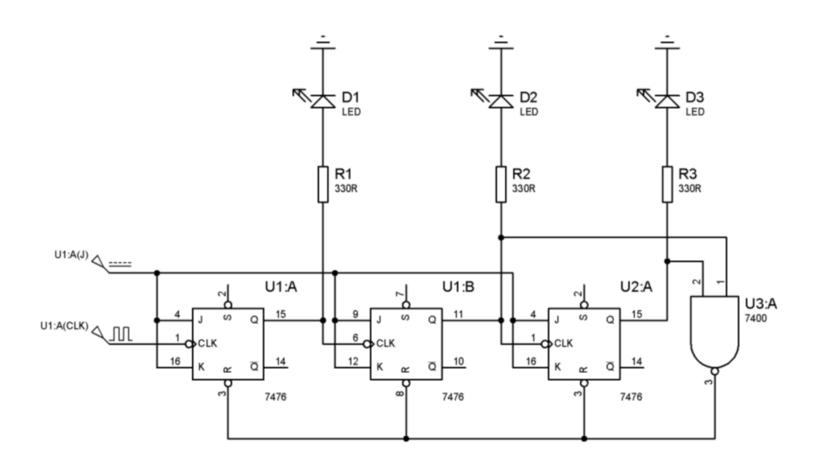
•Total no. of states = 6

•Maximum count = 5

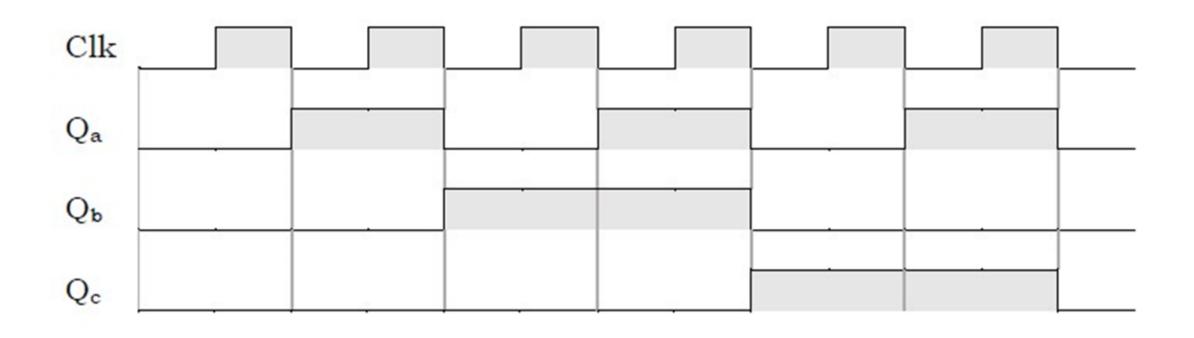
State
Diagram
Mod 6
counter



Mod 6 ripple up counter



Timing Diagram



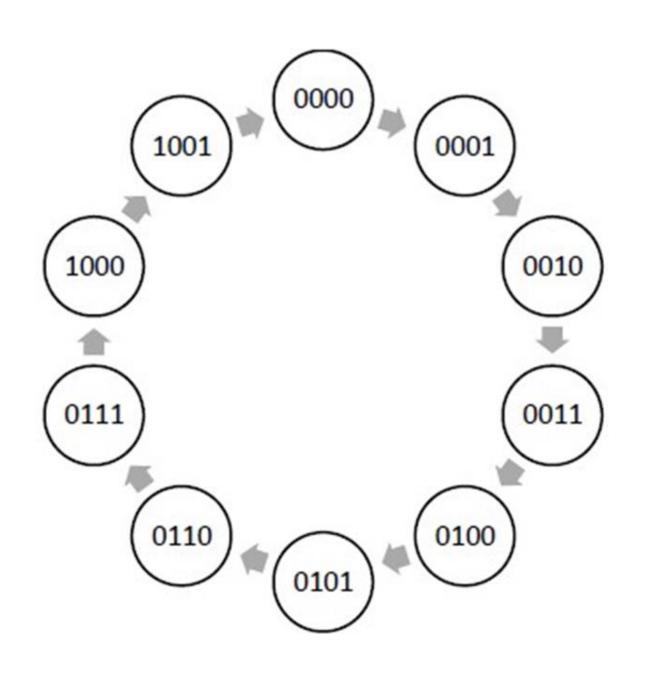
Mod 10 ripple up counter

Flip-Flopused = JK

•No. of FF used = 4

•Total no. of states = 10

•Max. count = 9



State Diagram

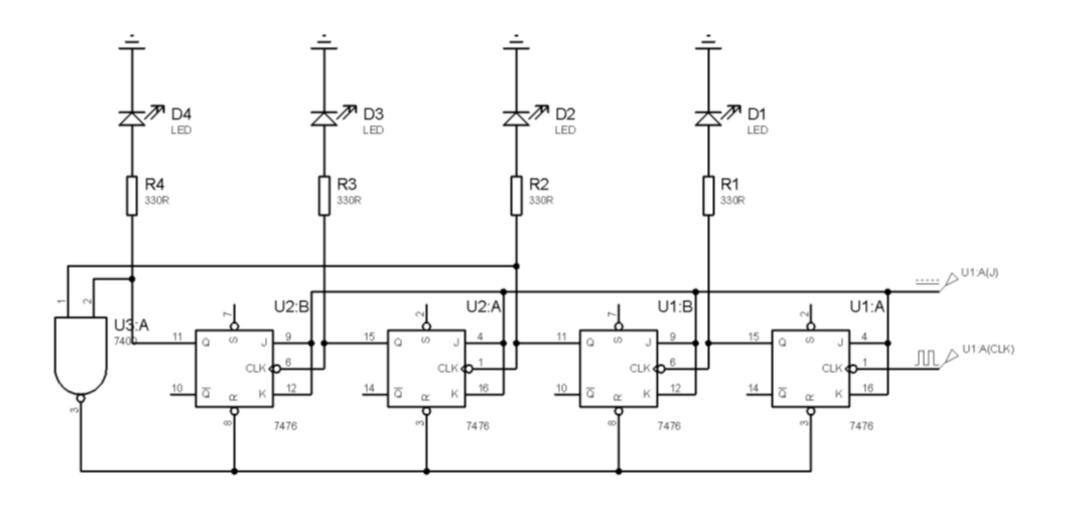
Count Sequence Table for mod 10 counter

Count Sequence Table

Q_d	Q _c	Qь	Qa	D.E
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10

Decade Counter Description

- •In the above count sequence table, the final combination (1,0,1,0) is the eleventh value given by the circuit.
- •However, we want the circuit to count till the combination (1,0,0,1). So, as soon as the shaded combination is realized, the circuit is forced recycled from moving any further.
- •We can force reset the circuit by connecting the high inputs of the shaded combination with the NAND gate connected to the clear input of each flip-flops.



Timing Diagram Decade Counter

