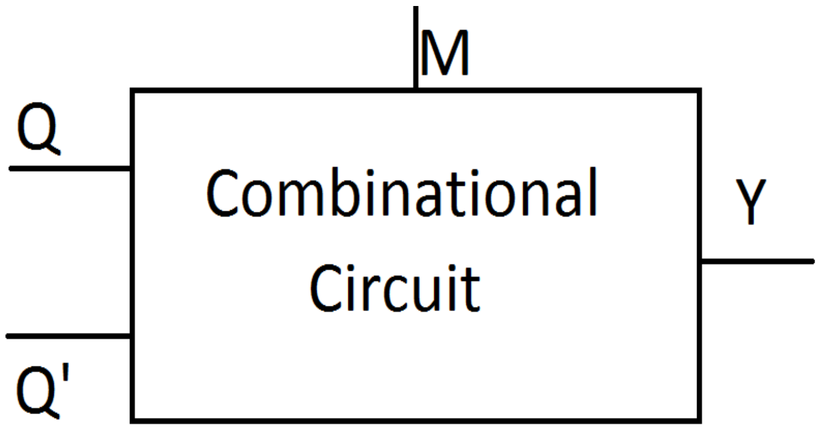
Up Down Counters

Counters continued

Ripple Up Down Counter

- This is the combination of both ripple up as well as down counter.
- The counter starts its count from 000 to 111 as well as form 111 back to 000.
- The circuit itself can’t perform up counting as well as down counting at the same time itself.
- Mode control input (M) is used to select either up mode or down mode.
- Combinational circuit is also required between each pair of flip-flop with accepts the output generated from previous flip-flop and mode control input as input.
- Then it generates output which is then fed to the clock of next flip-flop.

Illustration Up Down Counter with Mode



Let the circuit perform up count when M = 0 and down count when M = 1. That is, when M = 0, then the value of Y will be Q and when M = 1, then the value of Y will be Q’

Truth table of desire combinational circuit:

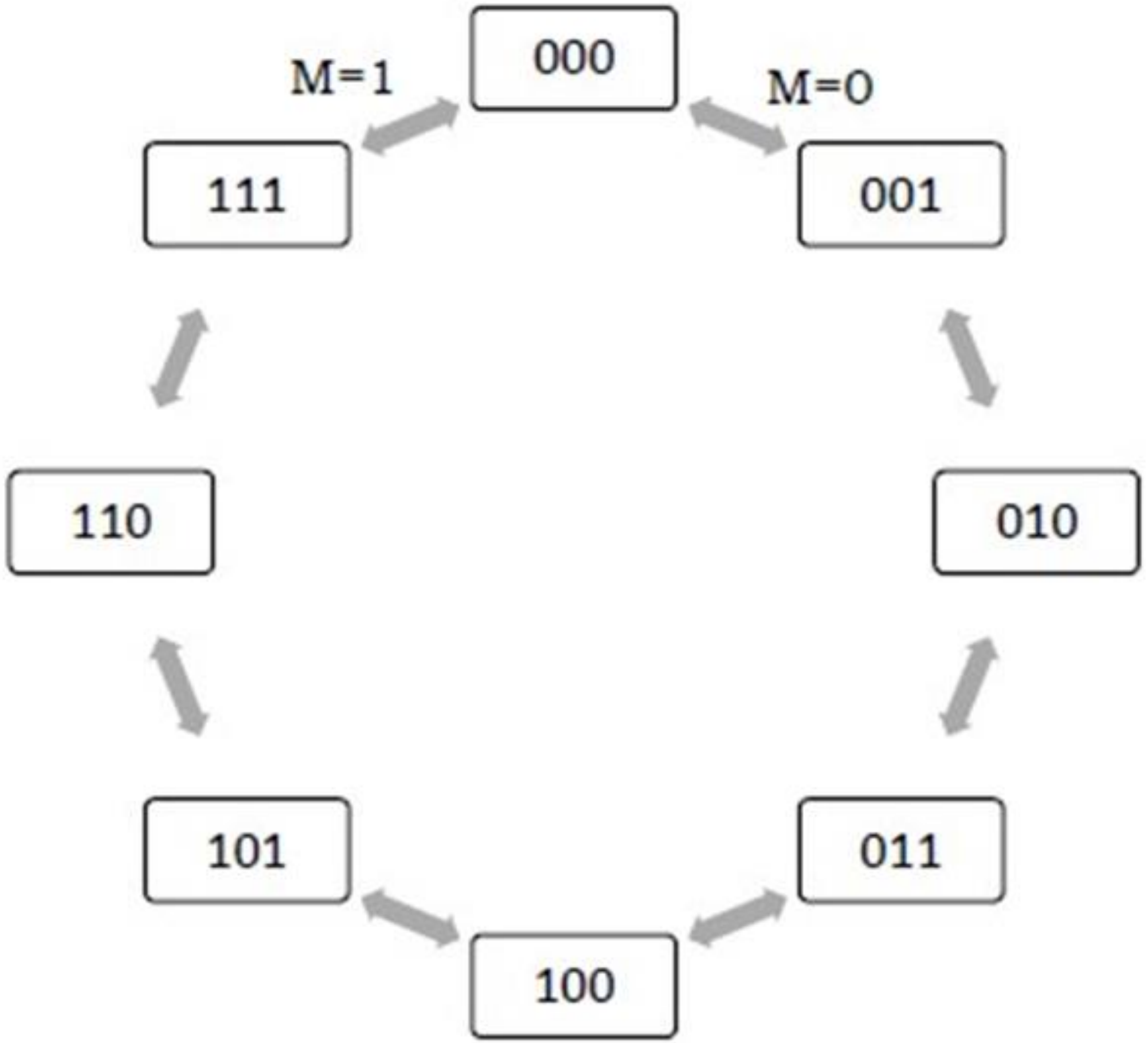
M	Q	Q’	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

K-Map for Y:

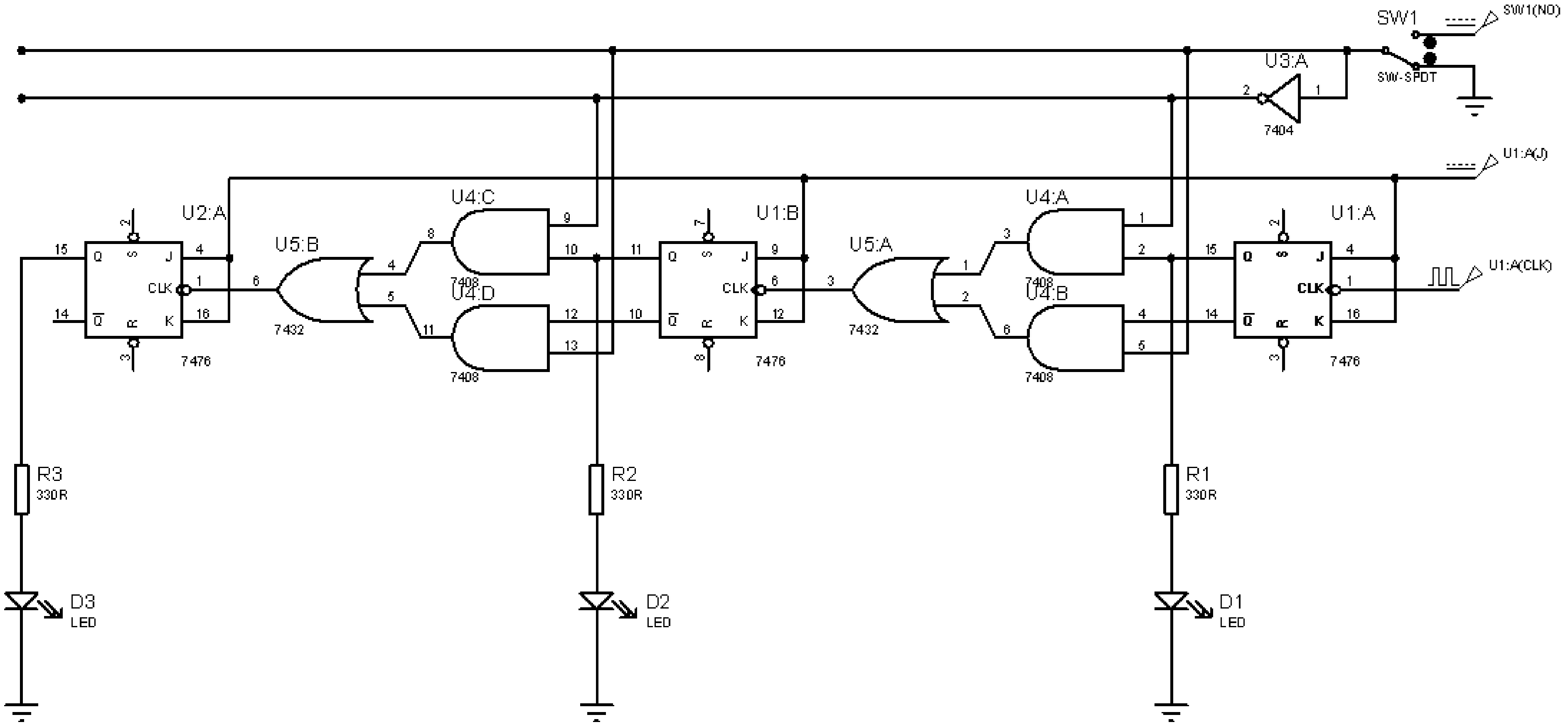
	Q’Q	Q’Q’	QQ’	QQ
M’	0	0	1	1
M	0	1	1	0

➔Y = M’Q + MQ’

State Diagram Ripple Up/Down Counter



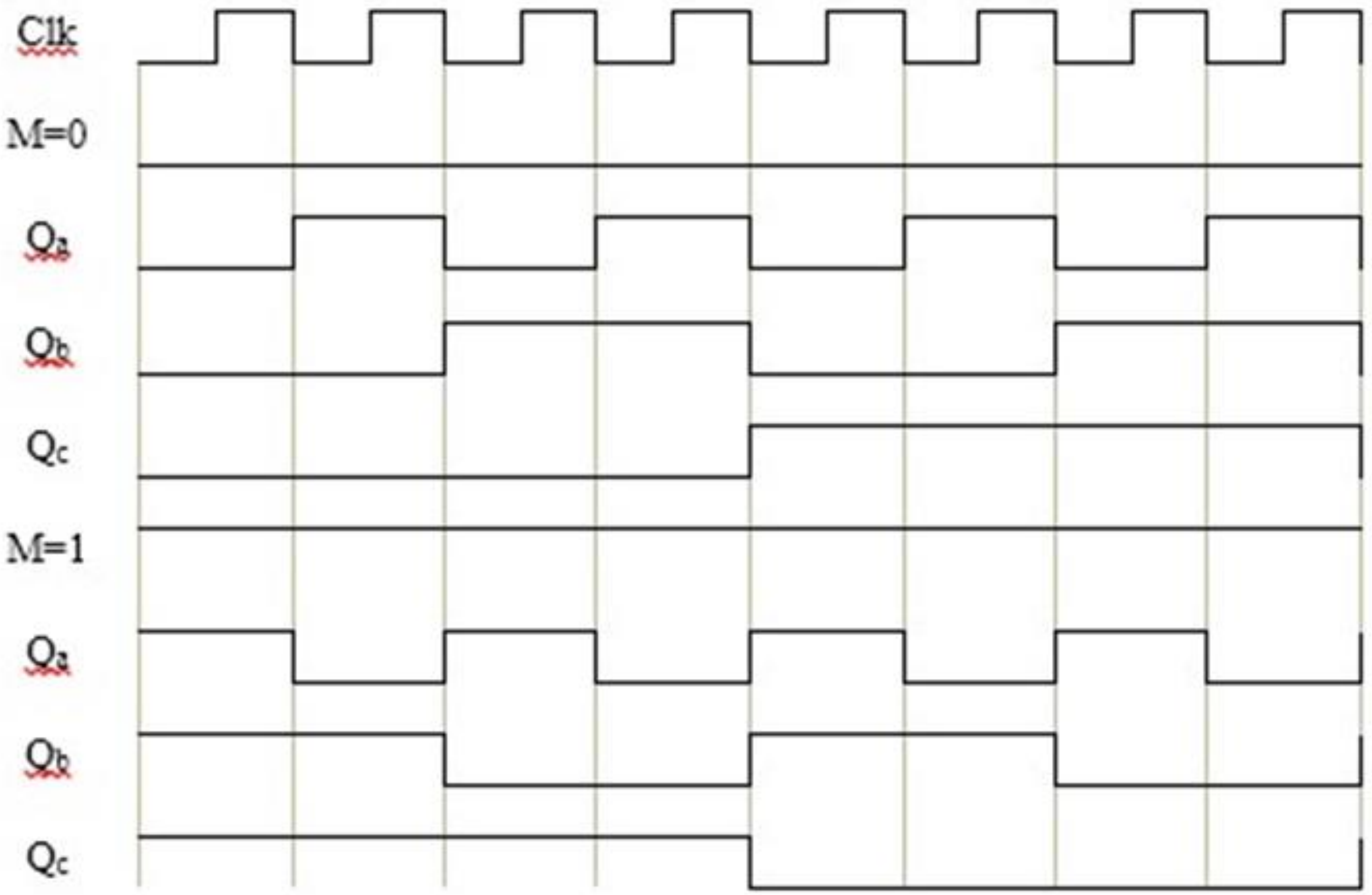
Up Down Counter



Count Sequence Table:

Clk	For M=0				For M=1			
	Q_c	Q_b	Q_a	D.E	Q_c	Q_b	Q_a	D.E
Initially	0	0	0	0	1	1	1	7
1 ↓	0	0	1	1	1	1	0	6
2 ↓	0	1	0	2	1	0	1	5
3 ↓	0	1	1	3	1	0	0	4
4 ↓	1	0	0	4	0	1	1	3
5 ↓	1	0	1	5	0	1	0	2
6 ↓	1	1	0	6	0	0	1	1
7 ↓	1	1	1	7	0	0	0	0

Timing Diagram Of Up Down Counter



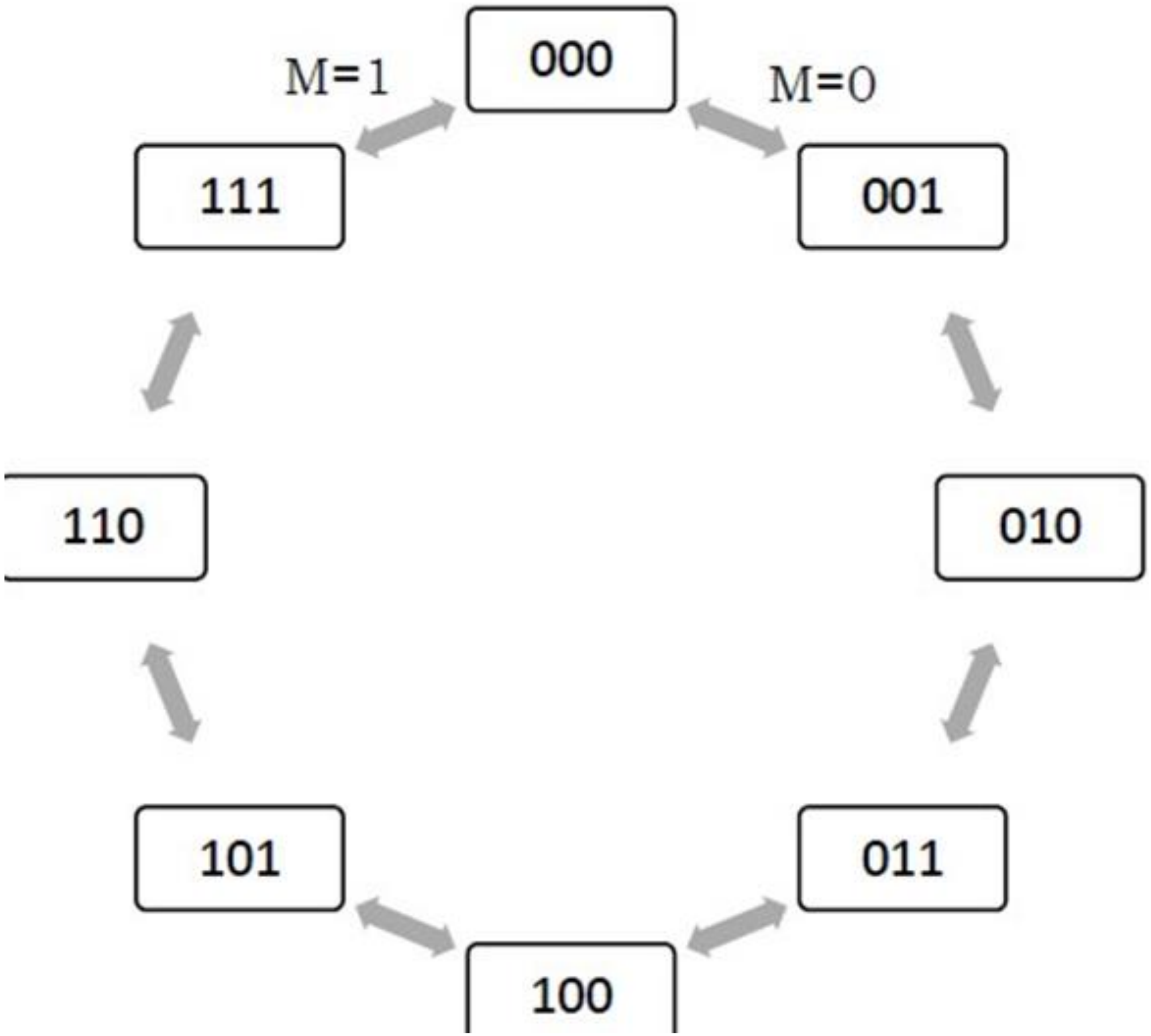
Construct 3-bit synchronous up/down counter

- In synchronous Count the clock input is same for the all flipflops used.
- For up Down Counting mode control input must be used to decide whether to up count or down count.
- **Flip-Flop used = JK**
- **Total no. of FF used = 3**

- **Excitation Table of the flip-flop used**

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

State Diagram synchronous up down counter



Circuit excitation table

Mode	Present State			Next State			Flip-Flop Excitation Table					
M	C	B	A	C^*	B^*	A^*	J_c	K_c	J_b	K_b	J_a	K_a
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	0
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	0
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	0
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	0
1	0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	1	0	0	0	0	X	0	X	X	0
1	0	1	0	0	0	1	0	X	X	1	1	X
1	0	1	1	0	1	0	0	X	X	0	X	0
1	1	0	0	0	1	1	X	1	1	X	1	X
1	1	0	1	1	0	0	X	0	0	X	X	0
1	1	1	0	1	0	1	X	0	X	1	1	X
1	1	1	1	1	1	0	X	0	X	0	X	0

map Synchronous UP Down

K – map for K_a

	B'A'	B'A	BA	BA'
M'C'	X	0	0	X
M'C	X	0	0	X
MC	X	0	0	X
MC'	X	0	0	X

➔ K_a = 1

K – map for K_b

	B'A'	B'A	BA	BA'
M'C'	X	X	1	0
M'C	X	X	1	0
MC	X	X	0	1
MC'	X	X	0	1

➔ K_b = M'A + MA'

K – map for J_a

	B'A'	B'A	BA	BA'
M'C'	1	X	X	1
M'C	1	X	X	1
MC	1	X	X	1
MC'	1	X	X	1

➔ J_a = 1

K – map for J_c

	B'A'	B'A	BA	BA'
M'C'	0	0	1	0
M'C	X	X	X	X
MC	X	X	X	X
MC'	1	0	0	0

➔ J_c = MB'A' + M'BA

K – map for J_b

	B'A'	B'A	BA	BA'
M'C'	0	1	X	X
M'C	0	1	X	X
MC	1	0	X	X
MC'	1	0	X	X

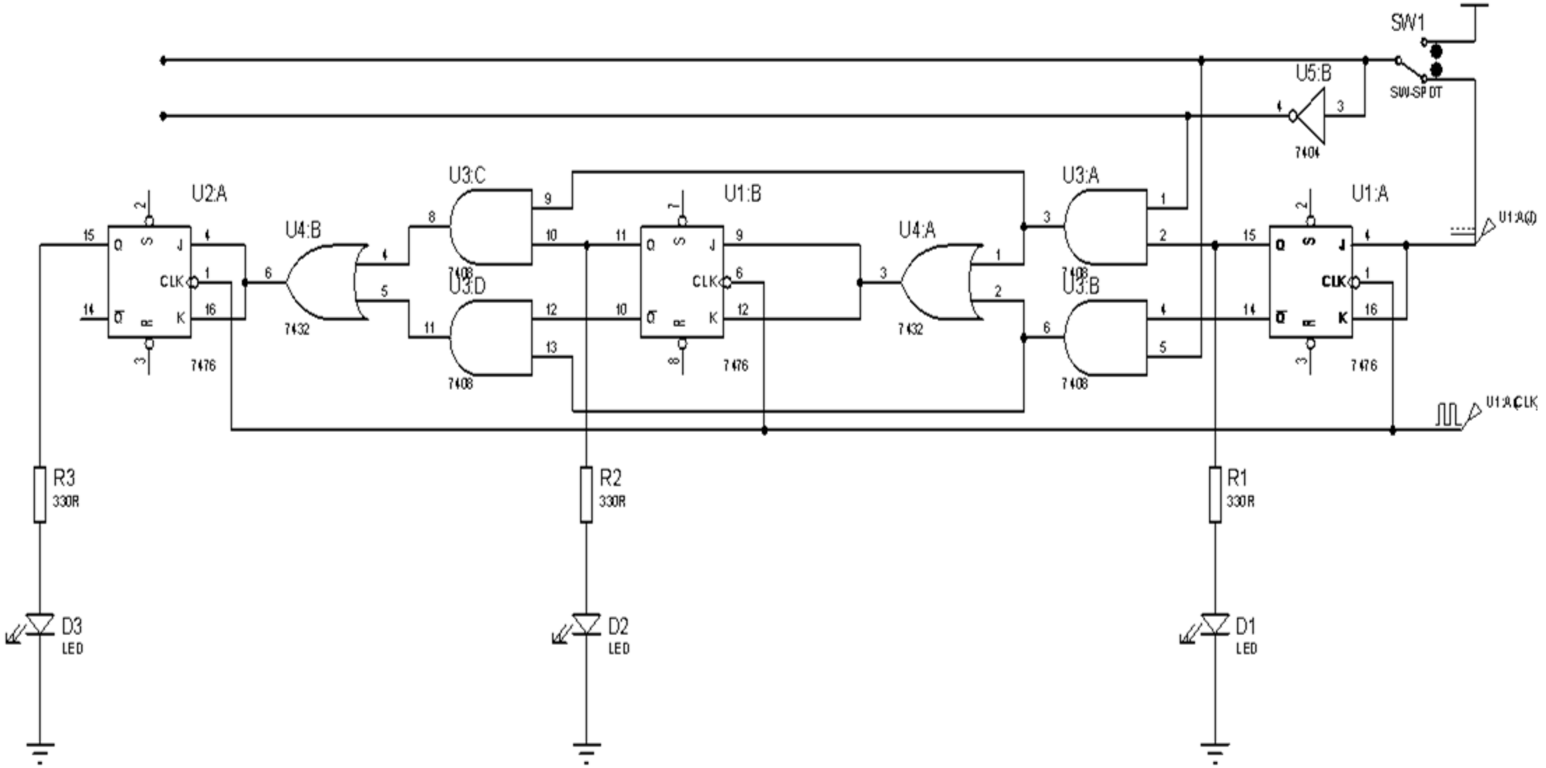
➔ J_b = M'A + MA'

K – map for K_c

	B'A'	B'A	BA	BA'
M'C'	X	X	X	X
M'C	0	0	1	0
MC	1	0	0	0
MC'	X	X	X	X

➔ K_c = MB'A' + M'BA

Synchronous Up Down Counter diagram



Count Sequence Table

Clock	M=0				M=1			
Clock Pulse	Q_C	Q_B	Q_A	Decimal Equivalent	Q_C'	Q_B'	Q_A'	Decimal Equivalent
Initially	0	0	0	0	1	1	1	7
1st	0	0	1	1	1	1	0	6
2nd	0	1	0	2	1	0	1	5
3rd	0	1	1	3	1	0	0	4
4th	1	0	0	4	0	1	1	3
5th	1	0	1	5	0	1	0	2
6th	1	1	0	6	0	0	1	1
7th	1	1	1	7	0	0	0	0

Timing Diagram