

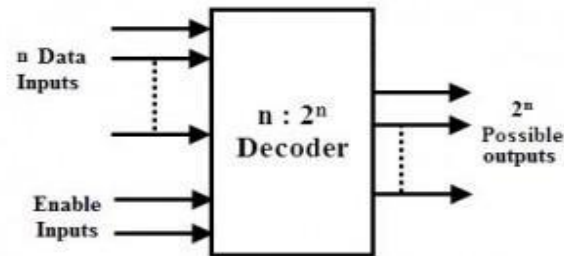
Combinational Logic Circuits

Decoder

DECODER

- A decoder is a multi-input, multi-output combinational circuit that converts a binary code of n input lines into a one out of 2^n output code. These are used when there is need to activate exactly one of 2^n output based on an n -bit input value. The figure below shows the general structure of decoder in which encoded information is accepted at n input lines and the output is produced at 2^n possible output lines. Generally, decoders are provided with enable inputs so as to activate the decoded output based on data inputs. As an example, in case of BCD code, the 4 bit combinations from 0000 through 1001 are enough to represent the decimal digits 0 to 9.

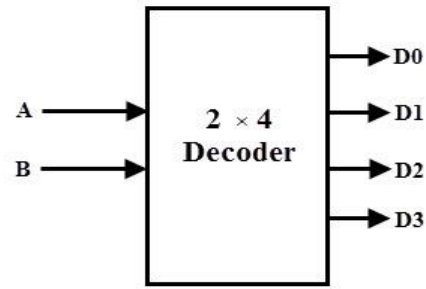
Decoder



- Depending on the number of input lines, the inputs of a binary code can be 2-bit or 3-bit or 4-bit codes. Upon the availability of 2^n lines, it activates the one of its output by deactivating (making logic 0) all other input whenever it receives n inputs. Usually the number of bits in output code is more than the bits in its input code. The most commonly used practical binary decoders are 2-to-4 decoder, 3-to-8 decoder and 4-to-16 line binary decoder.

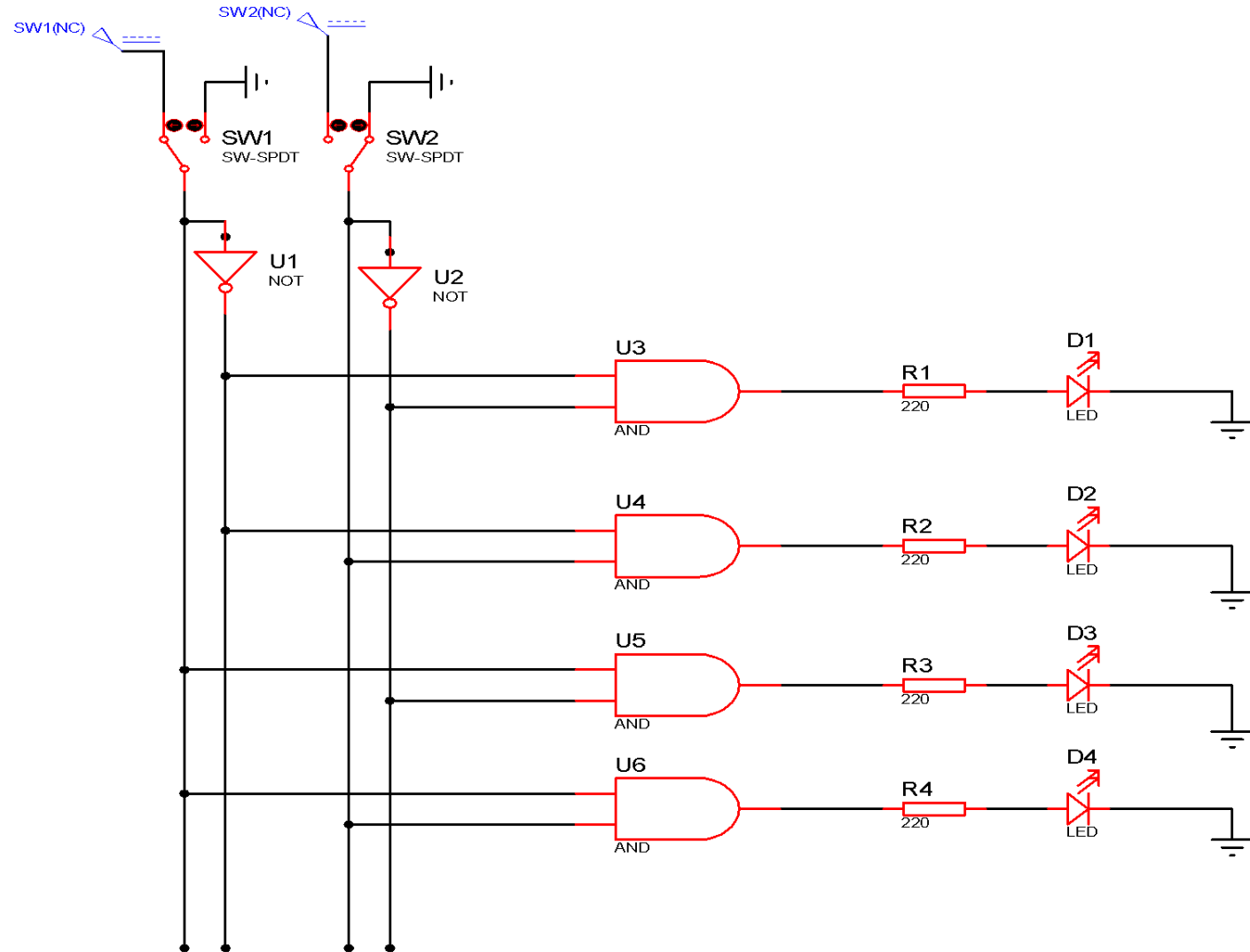
2 to 4-line Decoder

- In a 2-to-4 binary decoder, two inputs are decoded into four outputs hence it consists of two input lines and 4 output lines. Only one output is active at any time while the other outputs are maintained at logic 0 and the output which is held active or high is determined the two inputs A and B. The figure below shows the truth table for a 2-to-4 decoder.

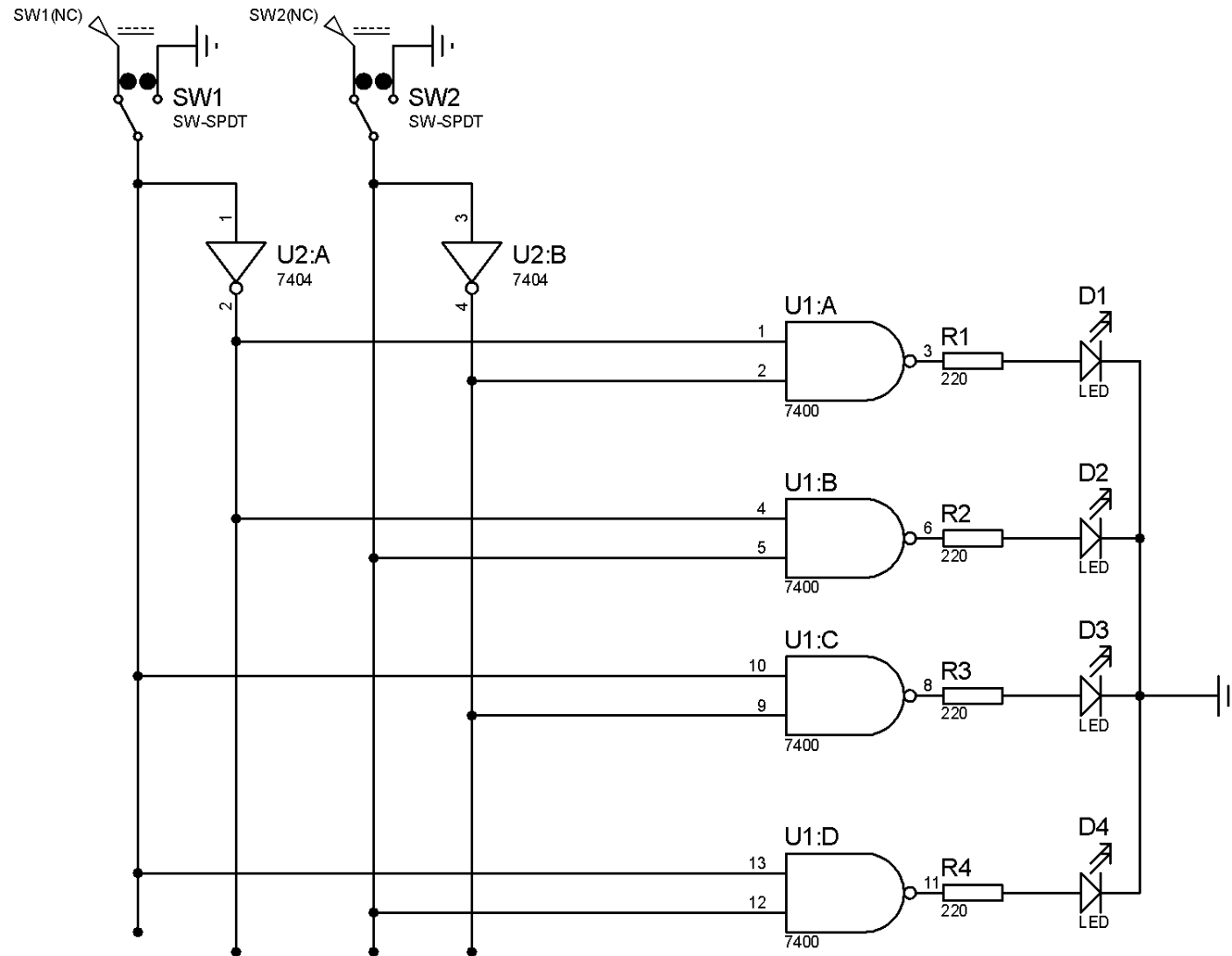


A	B	D0	D1	D2	D3
0	0	1	*	*	*
0	1	*	1	*	*
1	0	*	*	1	*
1	1	*	*	*	1

2 to 4-line Decoder Practical Logic Diagram

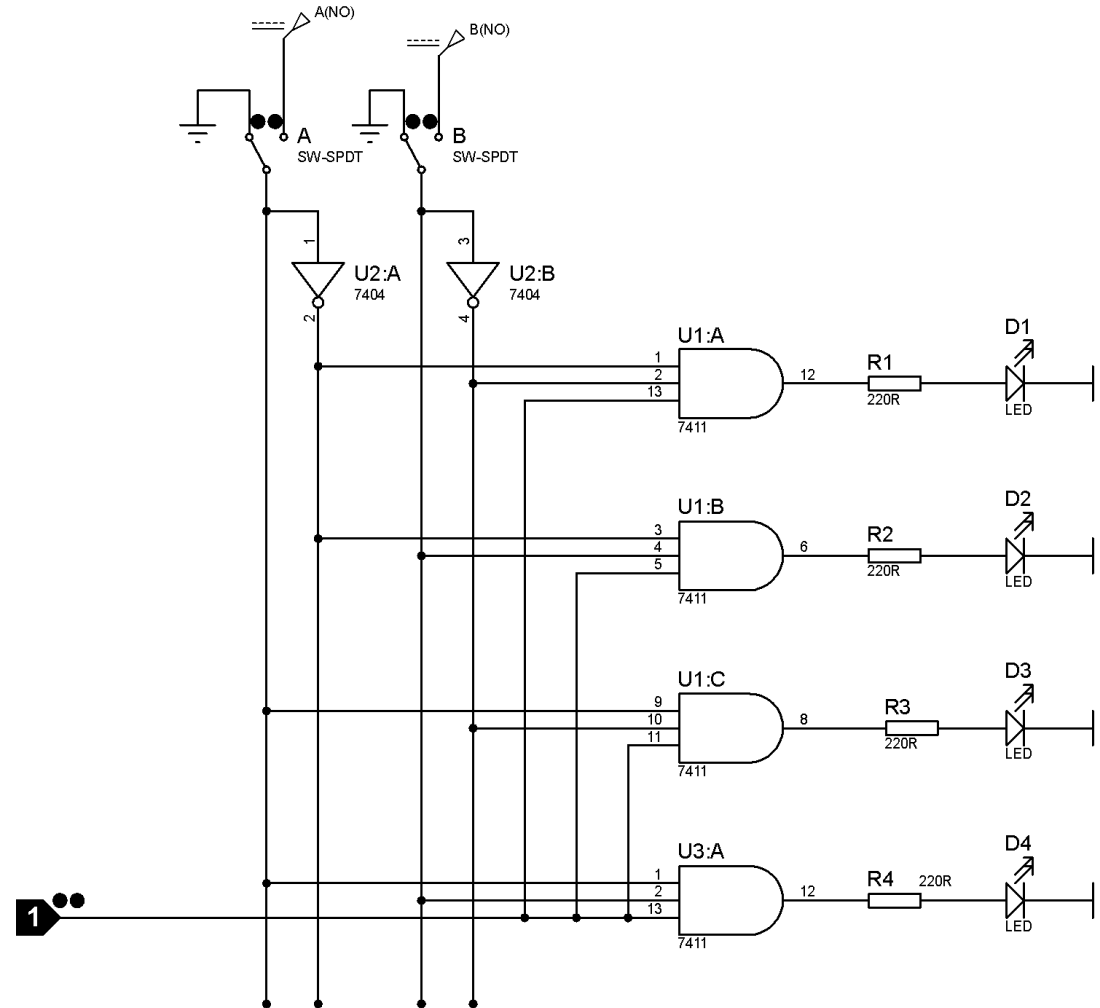


2 to 4 line Decoder using NAND



A	B	D0	D1	D2	D3
0	0	1	*	*	*
0	1	*	1	*	*
1	0	*	*	1	*
1	1	*	*	*	1

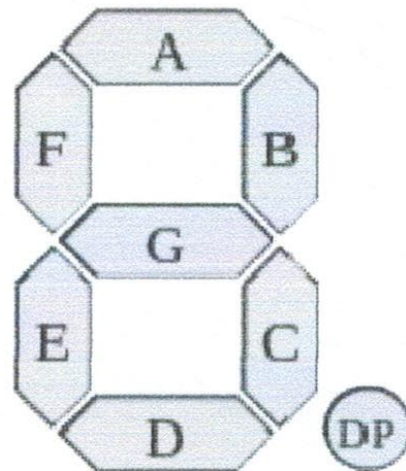
2 to 4 line Decoder with Enable



Seven Segment Display

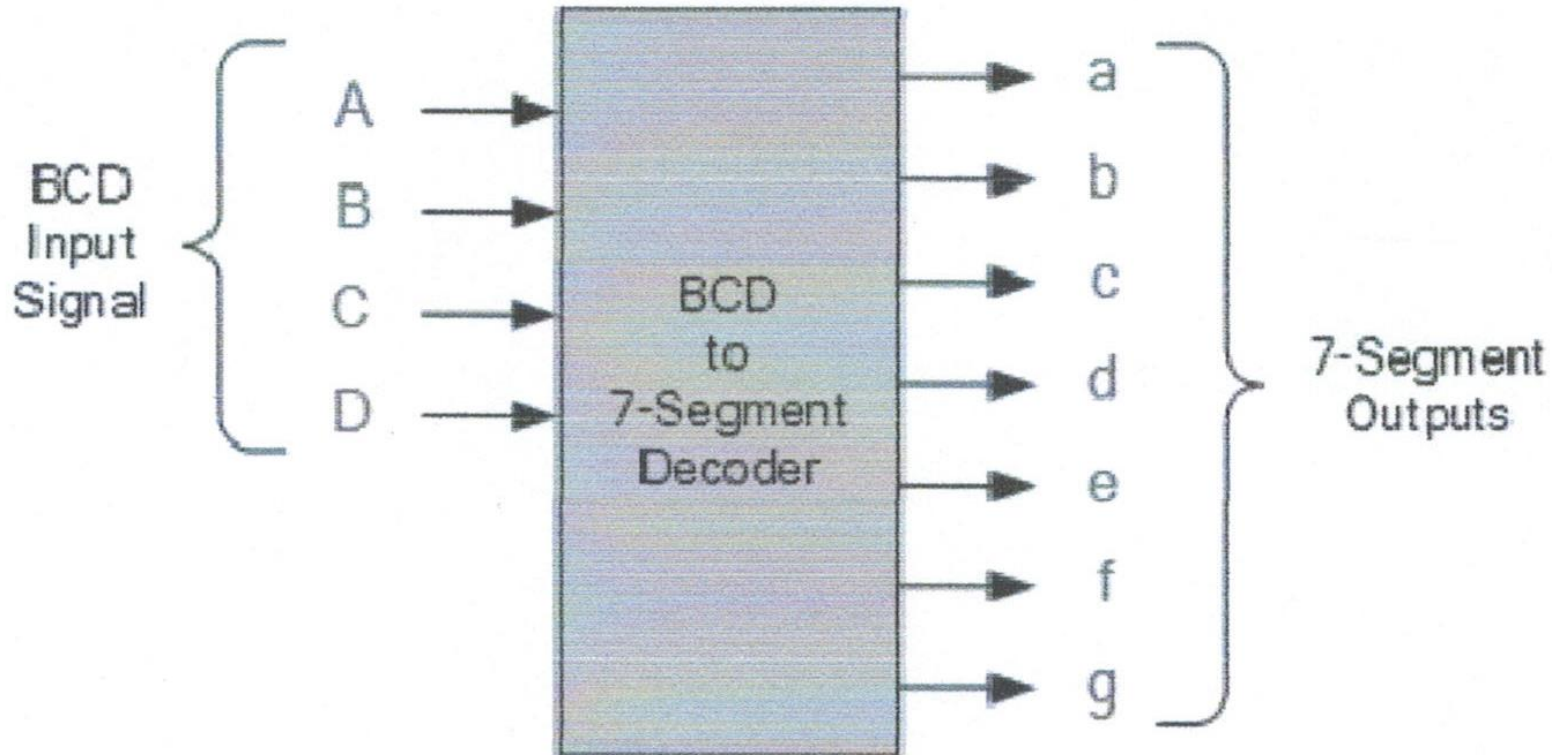
A seven-segment display (SSD), or seven-segment indicator, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot matrix displays. The seven segments are arranged as a rectangle of two vertical segments on each side with one horizontal segment on the top, middle, and bottom. Additionally, the seventh segment bisects the rectangle horizontally.

The segments of a 7-segment display are referred to by the letters A to G, where the optional decimal point (an "eighth segment", referred to as DP) is used for the display of non-integer numbers.



Seven Segment Decoder

It is a decoder used to convert a BCD or a binary code into a 7-segment code. It generally has 4 input lines and 7 output lines. Even though commercial BCD to 7 segment decoders are available, designing a display decoder using logic gates may prove to be beneficial from economical as well as knowledge point of view.



Truth Table For Seven Segment Display

Truth Table

BCD Inputs				Segments							Display
A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9

Segment 'a'

K-map for a

	CD'	CD	CD	CD'
$A'B'$	1	0	1	1
$A'B$	0	1	1	1
AB	x	x	x	x
AB'	1	1	x	x

$\rightarrow a = A + C + BD + B'D'$

Segment 'b'

K-map for b

	$C'D'$	$C'D$	CD	CD'
$A'B'$	1	1	1	1
$A'B$	1	0	1	0
AB	x	x	x	x
AB'	1	1	x	x

→ $b = B' + CD + C'D'$

Segment 'c'

K-map for c

	CD'	CD	CD	CD'
$A'B'$	1	1	1	0
$A'B$	1	1	1	1
AB	x	x	x	x
AB'	1	1	x	x

$$\rightarrow c = B + C' + D$$

Segment 'd'

K-map for d

	$C'D'$	$C'D$	CD	CD'
$A'B'$	1	0	1	1
$A'B$	0	1	0	1
AB	x	x	x	x
AB'	1	1	x	x

$$\rightarrow d = A + CD' + B'C + B'D' + BCD$$

Segment 'e'

K-map for e

	$C'D'$	CD	CD	CD'
$A'B'$	1	0	0	1
$A'B$	0	0	0	1
AB	x	x	x	x
AB'	1	0	x	x

$\rightarrow e = CD' + B'D'$

Segment 'f'

K-map for f

	$C'D'$	$C'D$	CD	CD'
$A'B'$	1	0	0	0
$A'B$	1	1	0	1
AB	x	x	x	x
AB'	1	1	x	x

$$\rightarrow f = A + BD' + BC' + C'D'$$

Segment 'f'

K-map for f

	$C'D'$	$C'D$	CD	CD'
$A'B'$	1	0	0	0
$A'B$	1	1	0	1
AB	x	x	x	x
AB'	1	1	x	x

$$\rightarrow f = A + BD' + BC' + C'D'$$

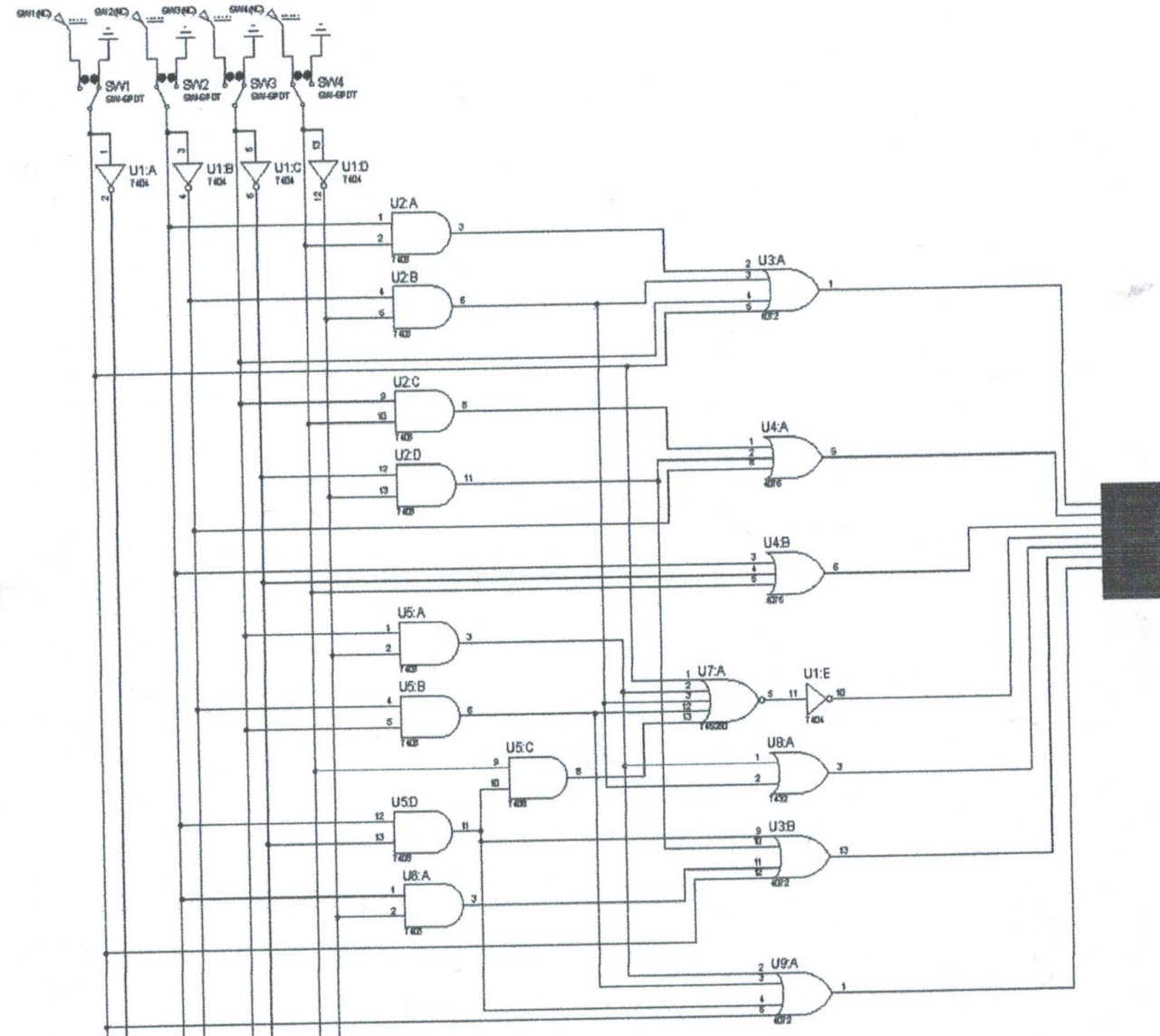
Segment 'g'

K-map for g

	$C'D'$	$C'D$	CD	CD'
$A'B'$	0	0	1	1
$A'B$	1	1	0	1
AB	x	x	x	x
AB'	1	1	x	x

$$\rightarrow g = A + CD' + B'C + BC'$$

Practical Logic Diagram For Seven Segment Display

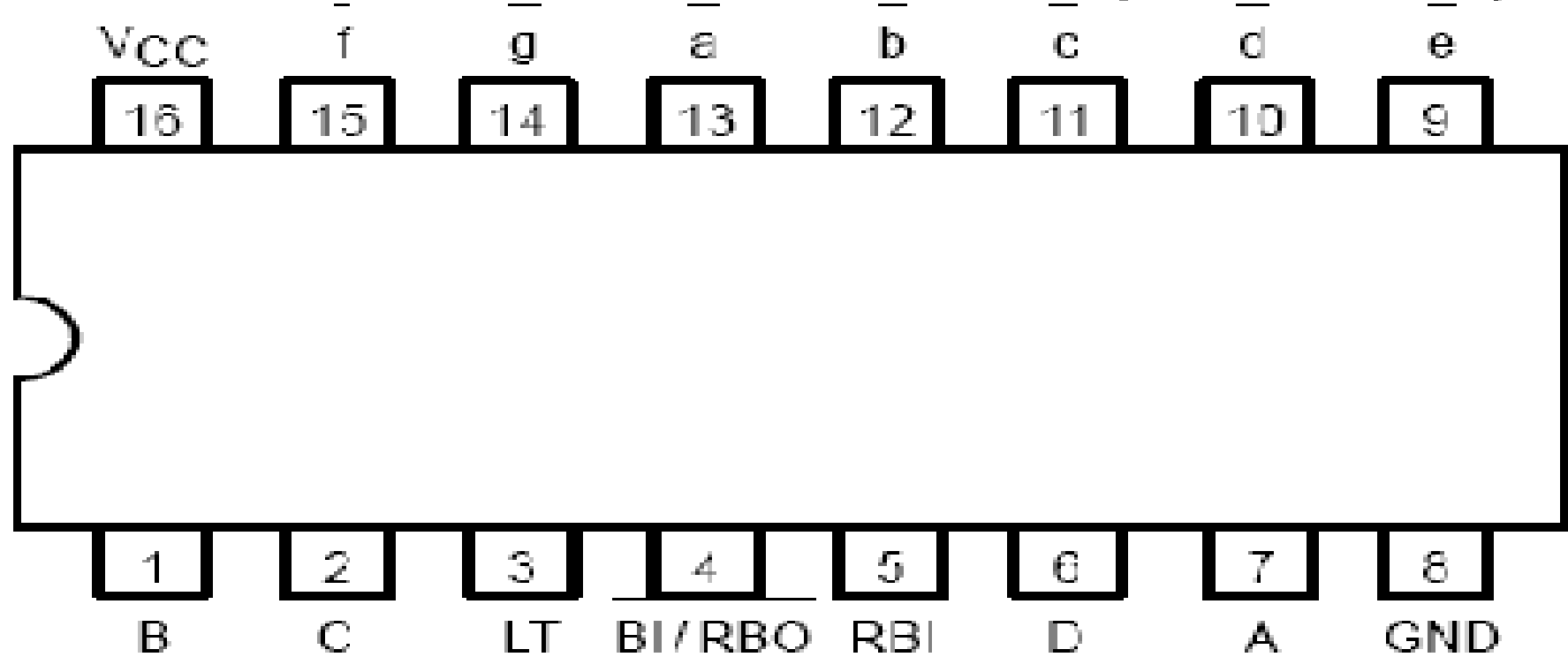


74xx47 BCD to Seven-segment display

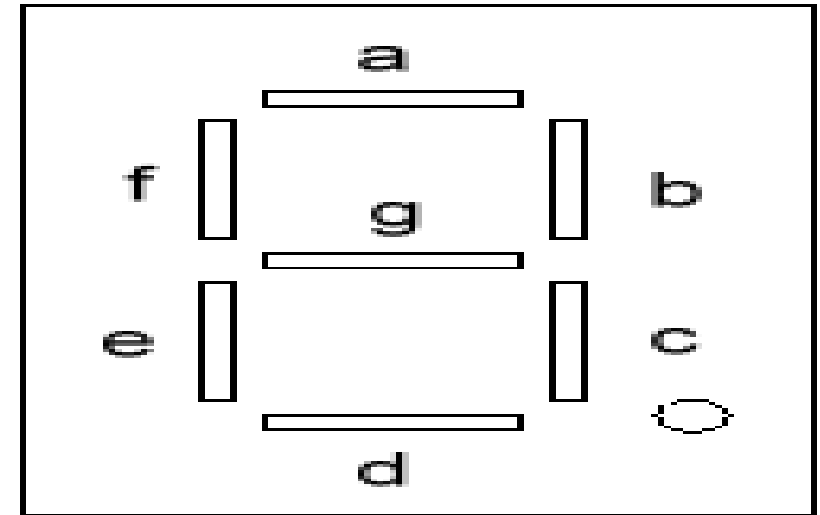
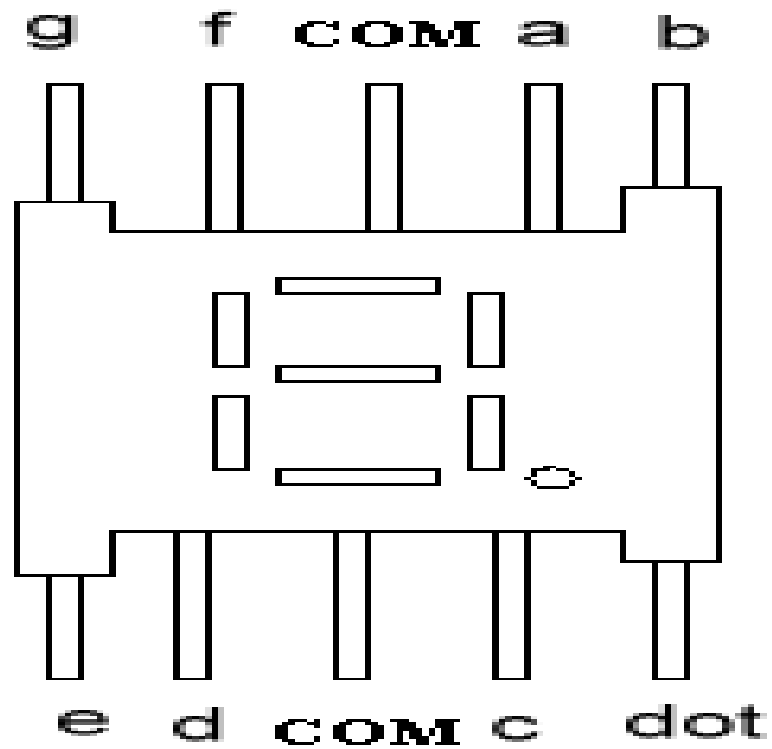
- The 74xx47 chip is used to drive 7 segment display.
- You must use the 74xx47 with a **common anode 7-segment display**.
- The input to the 74xx47 is a binary number **DCBA** where D is 8s, C is 4s, B is 2s and A is 1s.
- The display is only sensible if the binary number is between DCBA=0000 (0) and DCBA=1001 (9).
- That is why it is called BCD decoder If the number is larger than 9 you get a strange output on the display.

7447

CONNECTION DIAGRAM DIP (TOP VIEW)



7 segment display pin outs



Seven-Segment Display

Seven segment using 7447

