
COUNTER

Objectives

- To construct and verify 4-bit ripple up counter.
- To construct and verify 4-bit ripple down counter.
- To construct and verify 3-bit ripple up/down counter.
- To construct and verify 3 bit synchronous up/down counter.
- To construct and verify mod 3 ripple up counter.
- To construct and verify mod 5 ripple up counter.
- To construct and verify mod 10 ripple up counter.

Equipment Required

- Personal computer with ***simulation*** software for simulation of logic circuit installed,
- Digital Logic Trainer kit with following:
- Power supply unit,
- SPDT switches,
- LEDs,
- Clock input,
- Quad two input AND gates (7408),
- Quad two input OR gate (7432),
- Hex inverter (7404),
- Quad two input NAND gate (7400),
- Dual positive edge triggered D Flip-Flop (7474 IC),
- Dual JK Flip-Flop (7476 IC),
- Required numbers of connecting wire.

Counters

- Counters are defined as “The digital circuit which is used to count the number of pulses”.
- Counter circuits are the best example for the flip flop applications.
- Counters are designed by grouping of flip flops.
- counters are those, which have the group of storage elements like flip flops to hold the count.
- Broadly There are two types of counters available for digital circuits, they are:
- **Synchronous counters**
- **Asynchronous counters**

Asynchronous counters

- The counters in which the change in transition doesn’t depend upon the clock signal.
- In these counters, the first flip flop is connected to the external clock signal.
- The rest are clocked by the state outputs (Q & Q’) of the previous flip flop.

Synchronous counters

- The counters which use clock signal to change their transition are called “Synchronous counters”.
- Synchronous counters depends on their clock input to change state values.
- All flip flops in the synchronous counters are triggered by same clock signal.

Differences

SYNCHRONOUS COUNTERS

- •The propagation delay is very low.
- •Its operational frequency is very high.
- •Large number of logic gates are required to design
- •Standard logic packages available for synchronous.
- •High cost.

ASYNCHRONOUS COUNTERS

- •Propagation delay is higher than that of synchronous counters.
- •The maximum frequency of operation is very low.
- •Less number of logic gates required.
- •For asynchronous counters, Standard logic packages are not available.
- •Low cost.

Applications of Counters

- For suppose, in our kitchen appliances, we use microwave ovens. In that we set some temperature to heat the food item kept in it. Internally the counter calculates the increase or decrease in temperature and time. If it reaches the pre-set temperature, then it prevents from further heating and spoiling of that food item.

- Washing machines: We use counters in washing machines also. Similar to the counting operation in microwave oven, the counter in washing machine counts the time which we set it to operate.

- In both microwave oven and washing machine, we set the device to particular time, and it starts decreasing for every second. When the value of counter becomes zero, it activates the switch ON / OFF. Thus, the operation of the device is controlled by counters.

Construction and verification of 4-bit ripple up counter.

- The 4-bit ripple up counter starts its count from 0000 to 1111. That is, it counts from 0 to 15.

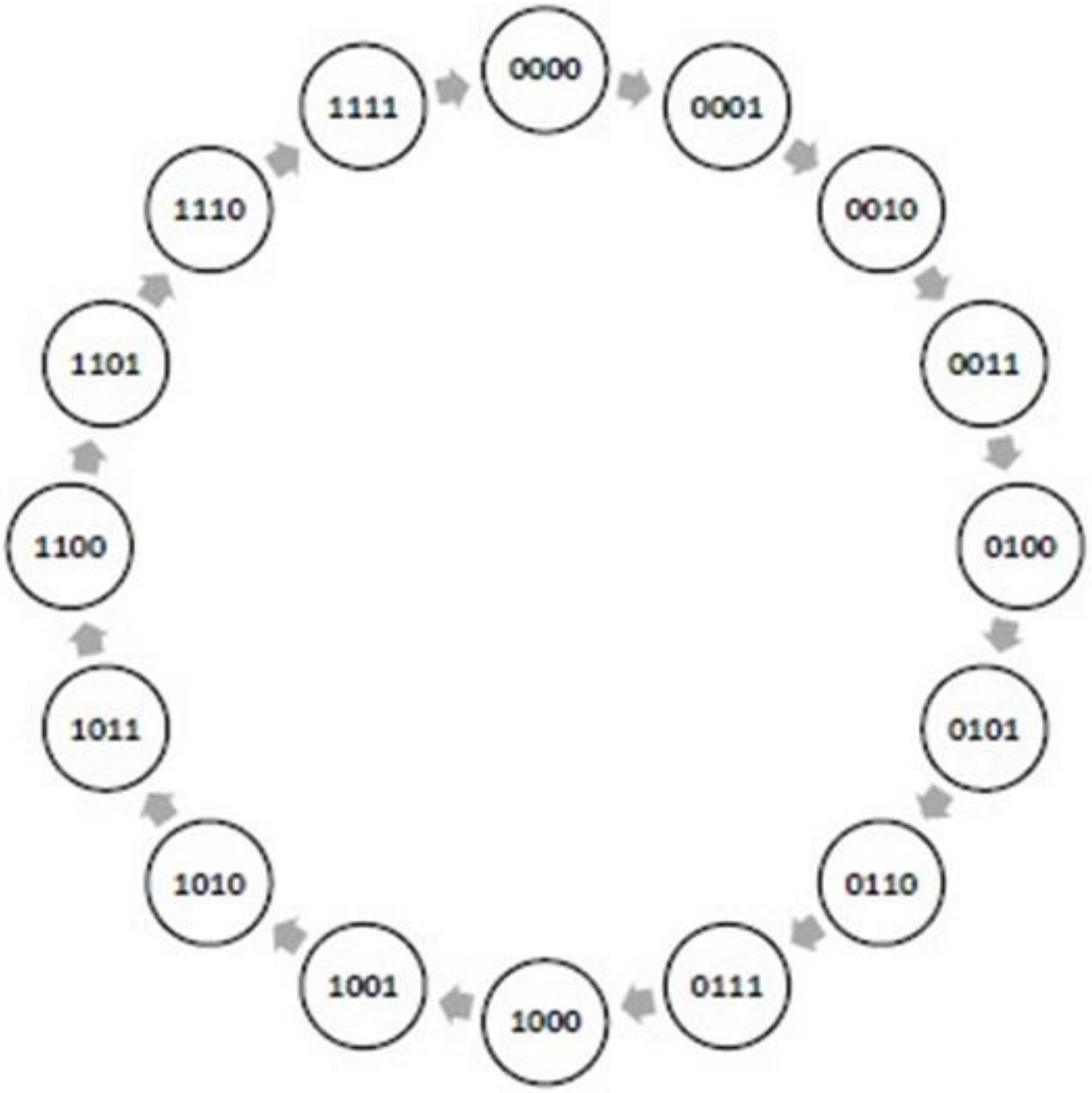
- **Name of Flip-Flop used:** JK

- **Number of Flip-Flop used:** 4

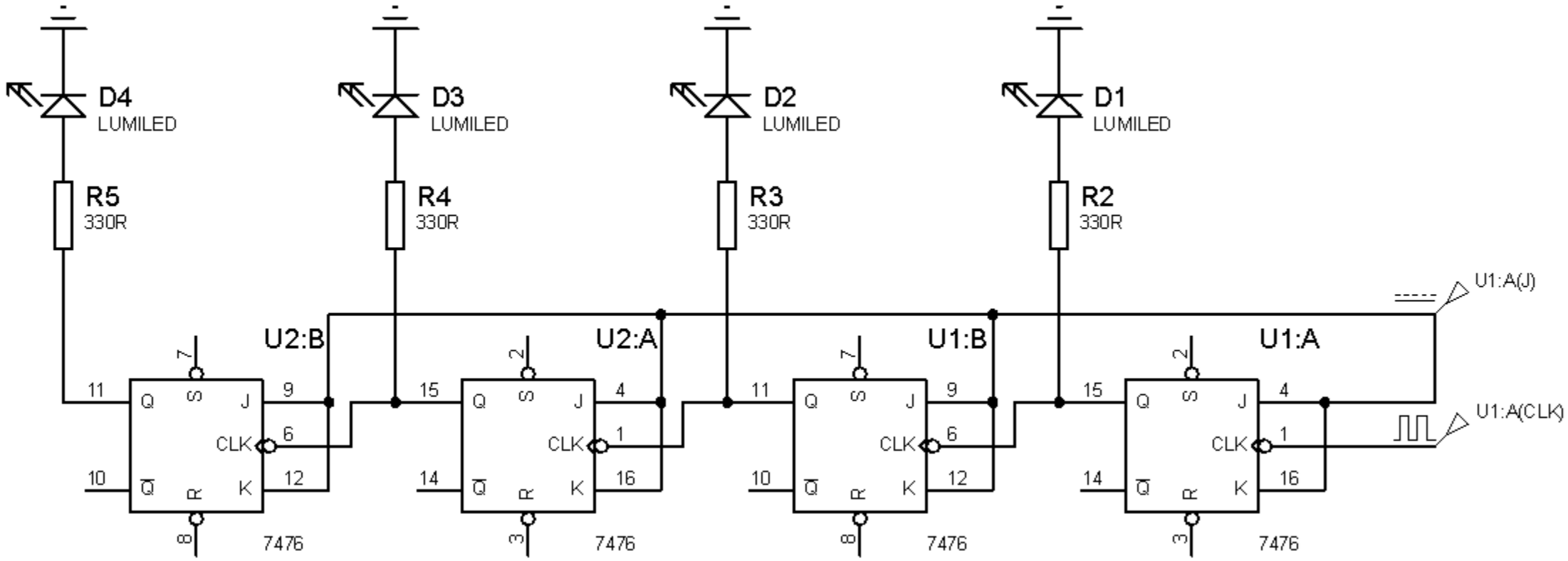
Asynchronous Ripple Up Counter

- 4 bit binary up counter (Ripple counter) In this circuit all FFs are clocked by Q output of the preceding FF.
- A ripple counter comprising of n FF is used to count up to 2^n pulses.
- A circuit with four FF gives a maximum count of 2^4 =16.
- The counter gives a natural count from 0 to 15 and resets on 16 th pulse.
- With application of the first clock pulse Q0 changes from 0 to 1 Q1, Q2, Q3 remain unaffected.
- With second clock pulses Q0 become 0 and Q1 become 1. At the 16thclockpulse all Q output resets and repeat the cycle.

State Diagram for 4-bit ripple up counter.



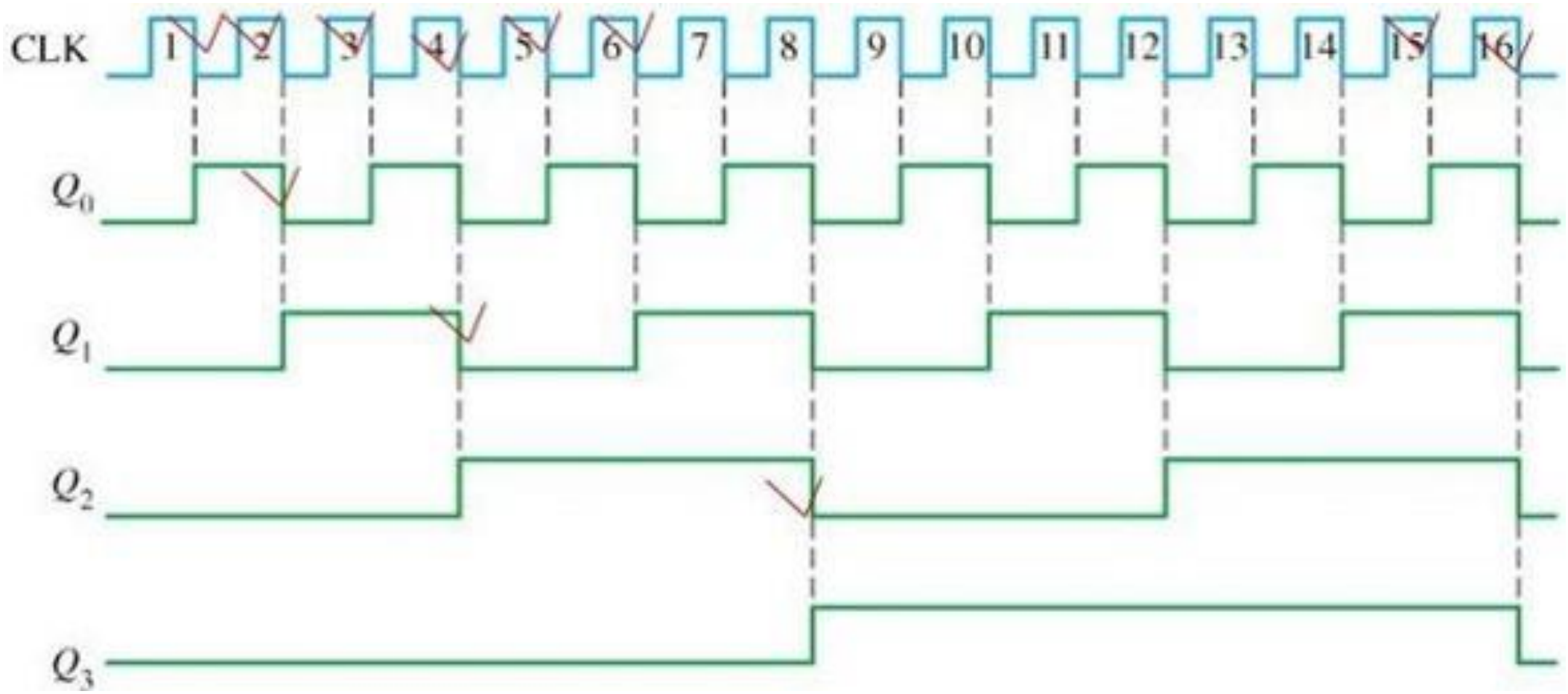
Circuit Diagram for 4-bit ripple up counter.



Count Sequence Table

Clk	Q_d	Q_c	Q_b	Q_a	D.E
Initially ↓	0	0	0	0	0
1 ↓	0	0	0	1	1
2 ↓	0	0	1	0	2
3 ↓	0	0	1	1	3
4 ↓	0	1	0	0	4
5 ↓	0	1	0	1	5
6 ↓	0	1	1	0	6
7 ↓	0	1	1	1	7
8 ↓	1	0	0	0	8
9 ↓	1	0	0	1	9
10 ↓	1	0	1	0	10
11 ↓	1	0	1	1	11
12 ↓	1	1	0	0	12
13 ↓	1	1	0	1	13
14 ↓	1	1	1	0	14
15 ↓	1	1	1	1	15

Timing Diagram For Ripple up Counter



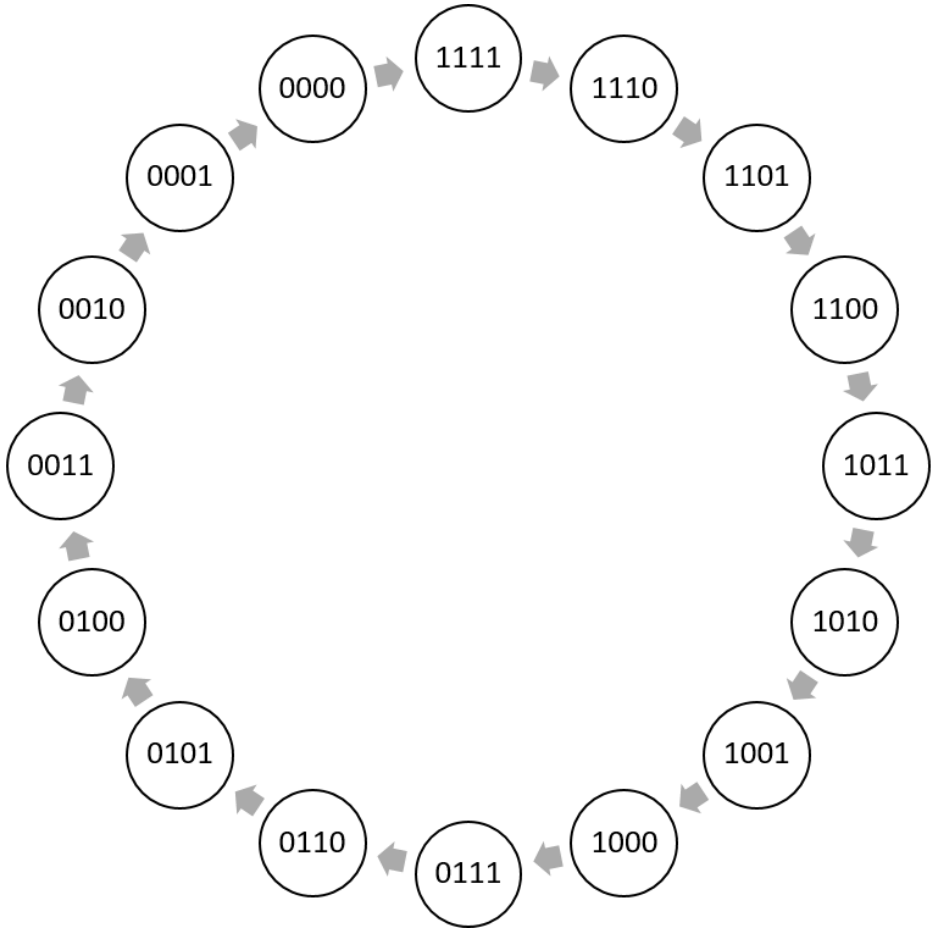
Verification of 4-bit ripple down counter.

- The 4-bit ripple down counter starts its count from 1111 to 0000. That is, it counts backwards from 15 to 0.

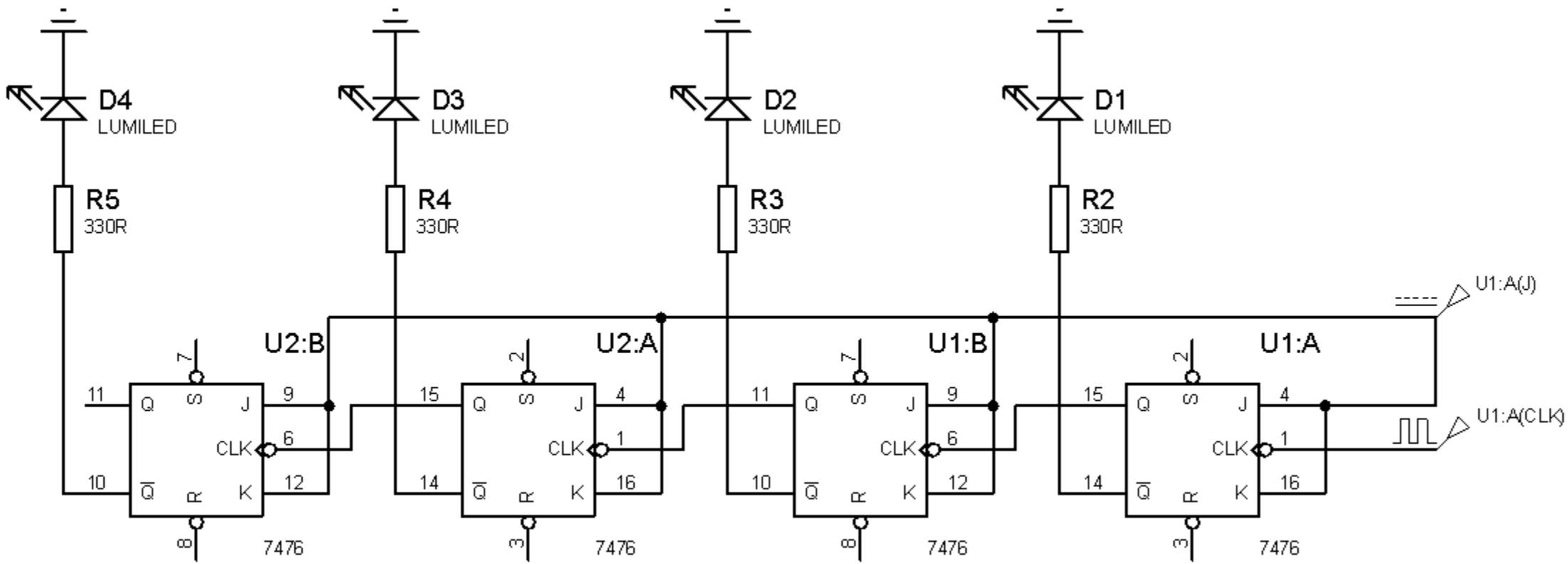
- **Name of Flip-Flop used:** JK

- **Number of Flip-Flop used:** 4

State Diagram Down Counter



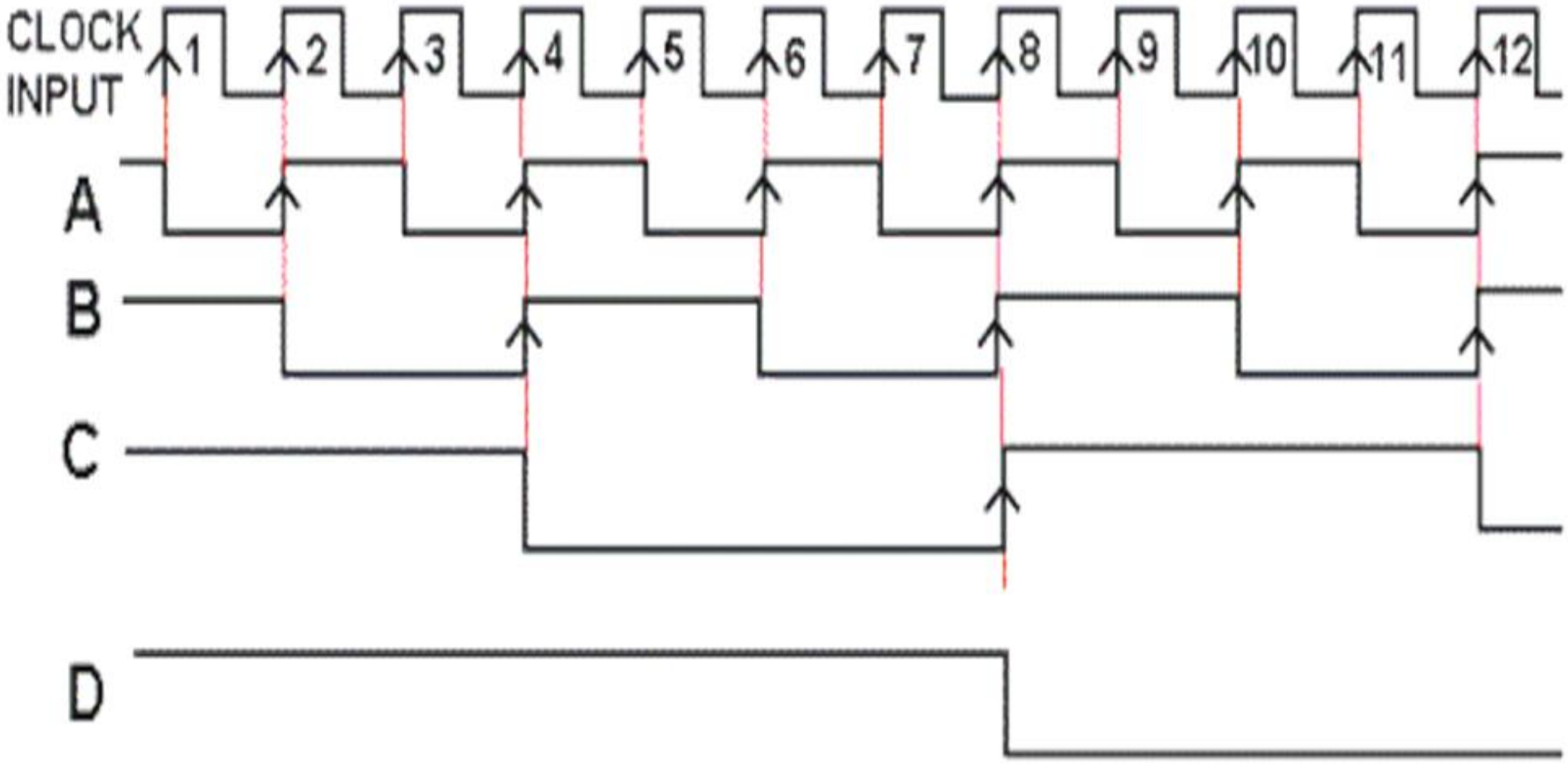
Circuit Diagram for 4-bit ripple Down counter.



Time Sequence Table

Clk	Q_d	Q_c	Q_b	Q_a	D.E
Initially	1	1	1	1	15
1 ↓	1	1	1	0	14
2 ↓	1	1	0	1	13
3 ↓	1	1	0	0	12
4 ↓	1	0	1	1	11
5 ↓	1	0	1	0	10
6 ↓	1	0	0	1	9
7 ↓	1	0	0	0	8
8 ↓	0	1	1	1	7
9 ↓	0	1	1	0	6
10 ↓	0	1	0	1	5
11 ↓	0	1	0	0	4
12 ↓	0	0	1	1	3
13 ↓	0	0	1	0	2
14 ↓	0	0	0	1	1
15 ↓	0	0	0	0	0

Timing Diagram Down Counter



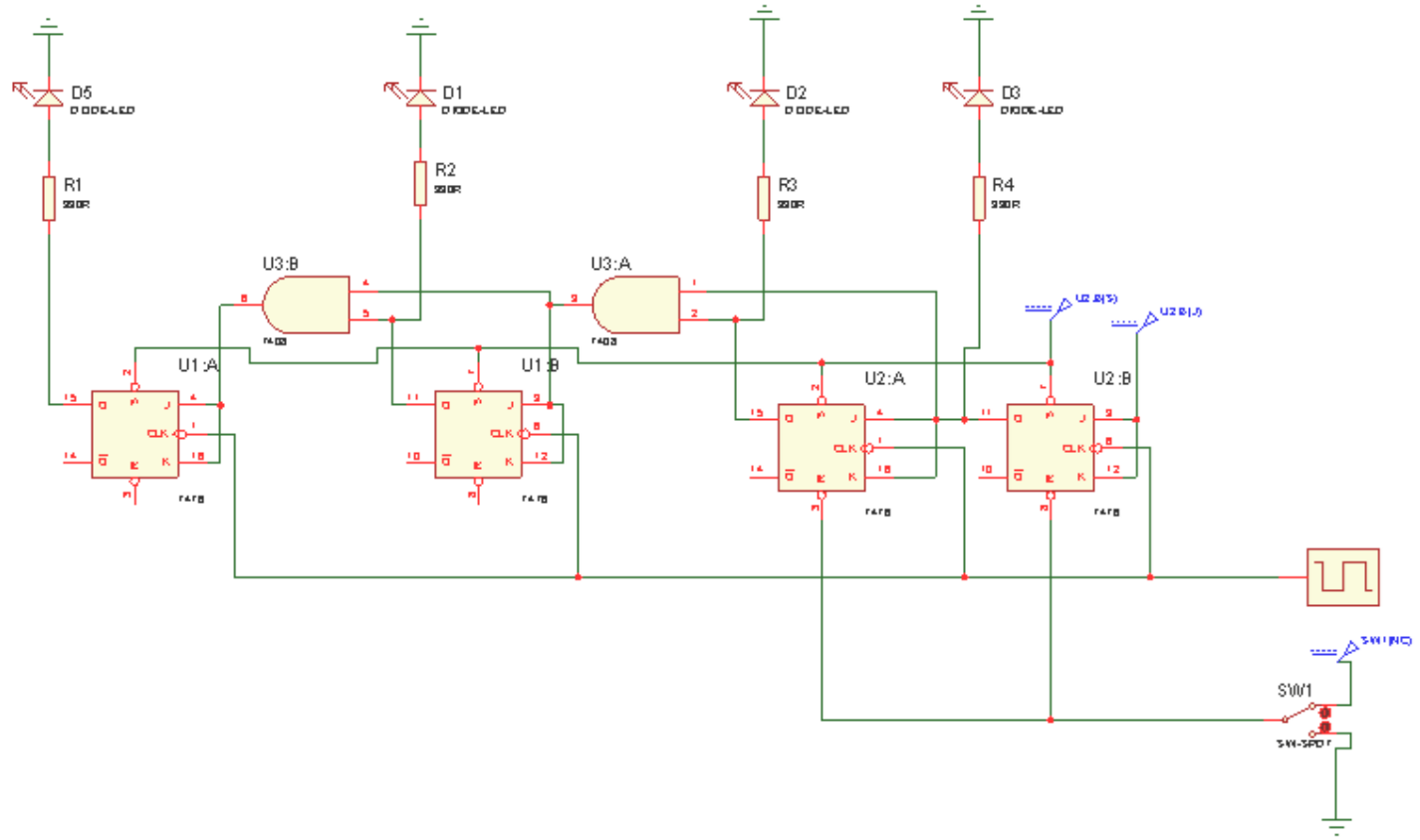
NOTE:

- Although both up and down counters can be built, using the asynchronous method for propagating the clock, they are not widely used as counters as they become unreliable at high clock speeds, or when a large number of flip-flops are connected together to give larger counts, due to the clock ripple effect.

SYNCHRONOUS COUNTERS

- •Synchronous counters are such counters where the counter is clocked in such way that each flip flop in the counter is triggered At the same time. This is accomplished by connecting the clock line to each stage of counter. Eg :- Synchronous up/down counters.

Synchronus



Ripple Up Down Counter

- •This is the combination of both ripple up as well as down counter.
- •The counter starts its count from 000 to 111 as well as form 111 back to 000.
- •The circuit itself can’t perform up counting as well as down counting at the same time itself.
- •Mode control input (M) is used to select either up mode or down mode.
- •Combinational circuit is also required between each pair of flip-flop with accepts the output generated from previous flip-flop and mode control input as input.
- •Then it generates output which is then fed to the clock of next flip-flop.

Illustration Up Down Counter with Mode

- Let the circuit perform up count when M = 0 and down count when M = 1. That is, when M = 0, then the value of Y will be Q and when M = 1, then the value of Y will be Q’