* DIRECT MEMORY ACCESS (DMA)

→ DMA is an I/O technique commonly used for high-speed data transfer.

Ex- Transfer b/w system memory & a floppy disk.

→ In status check I/O & interrupt I/O, the data transfer is relatively slow because each instruction needs to be fetched & executed.

→ In DMA, the MPU releases the control of the buses to a device called a DMA Controller.

→ The Controller manages the data transfer b/w memory and a peripheral under its control, thus bypassing the MPU.

→ During DMA operation, two signals of 8085 will be used.

↳ HOLD

↳ HLDA (Hold Acknowledge)

HOLD

→ This is an active high input signal to the 8085.

→ After receiving the HOLD request, the MPU relinquish the buses in the following machine cycle.

→ All buses are tri-stated and the Hold Acknowledge (HLDA) signal is sent out.

→ The MPU regains the control of the Buses after HOLD goes low.

HLDA

↳ This is an active high o/p signal indicating that the MPU is relinquishing control of the Buses.

* 8237 DMA Controller

→ It is a programmable ~~DMA~~ 40-pin package IC.

→ It has four independent channels with each channel capable of transferring 64K bytes.

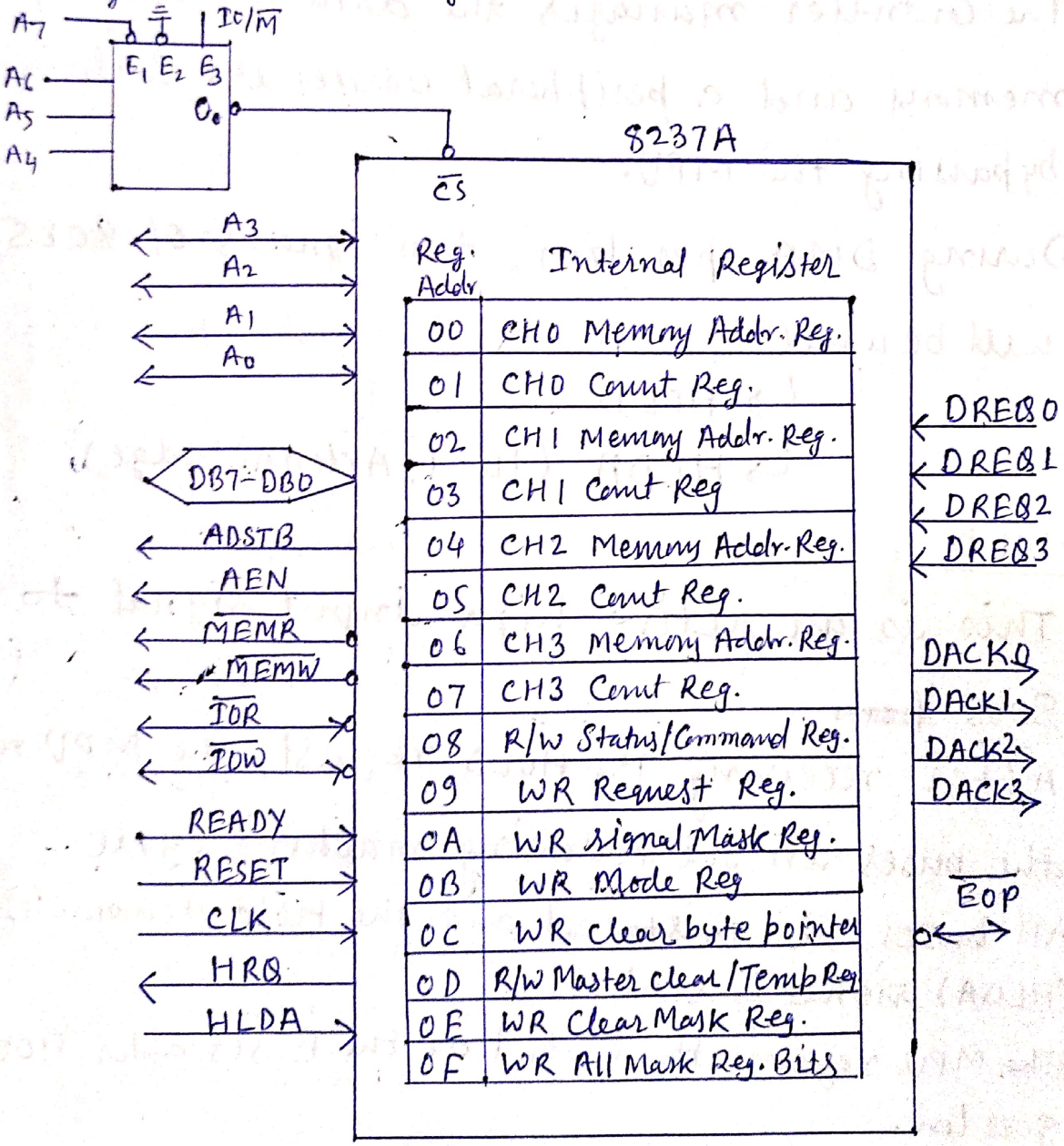
→ It must interface with two types of devices.

↳ MPU (Microprocessor Unit)

↳ Peripherals

DMA Channels And Interfacing

→ Figure shows a logical pin out & internal registers of 8237.

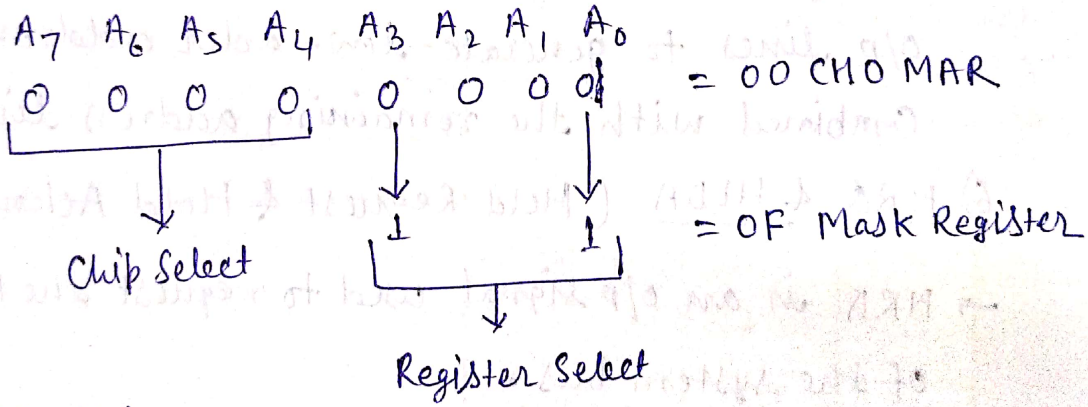


→ The 8237 has four independent channel
  - ↳ CH0
  - ↳ CH1
  - ↳ CH2
  - ↳ CH3

→ Internally, two 16-bit registers are associated with each channel.
  - ↳ One is used to load a starting Address of the byte to be Copied.
  - ↳ Second is used to load a count of the no. of bytes to be Copied.

→ The addresses of these registers are determined by four Address lines, (A_3 to A_0) & Chip Select ($\overline{CS}$) signal (A_7 to A_4).

→ Address of internal registers range from 00 to 0F H as follows:



DMA SIGNALS

→ There are various signals are available as follows.

1) DREQ0 - DREQ3 (DMA Request)

→ These are four independent, asynchronous input signals to the DMA channels from peripherals (floppy disk / Hard disk).

→ To obtain DMA service, a request is generated by activating the DREQ line of the channel.

2) DACK0 - DACK3 - (DMA Acknowledge)

→ These are o/p lines to inform the individual peripherals that a DMA is granted.

→ DREQ & DACK are equivalent to handshake signals in I/O devices.

3) AEN and ADSTB (Address Enable & Address Strobe):

→ These are active high o/p signals that are used to latch a high-order address byte to generate a 16-bit address.

4) $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ (Memory Read & Memory Write)

→ These are o/p signals used during DMA cycle to write and Read from memory.

5) A_3-A_0 & A_7-A_4 Addresses

→ A_3-A_0 are bidirectional address lines.

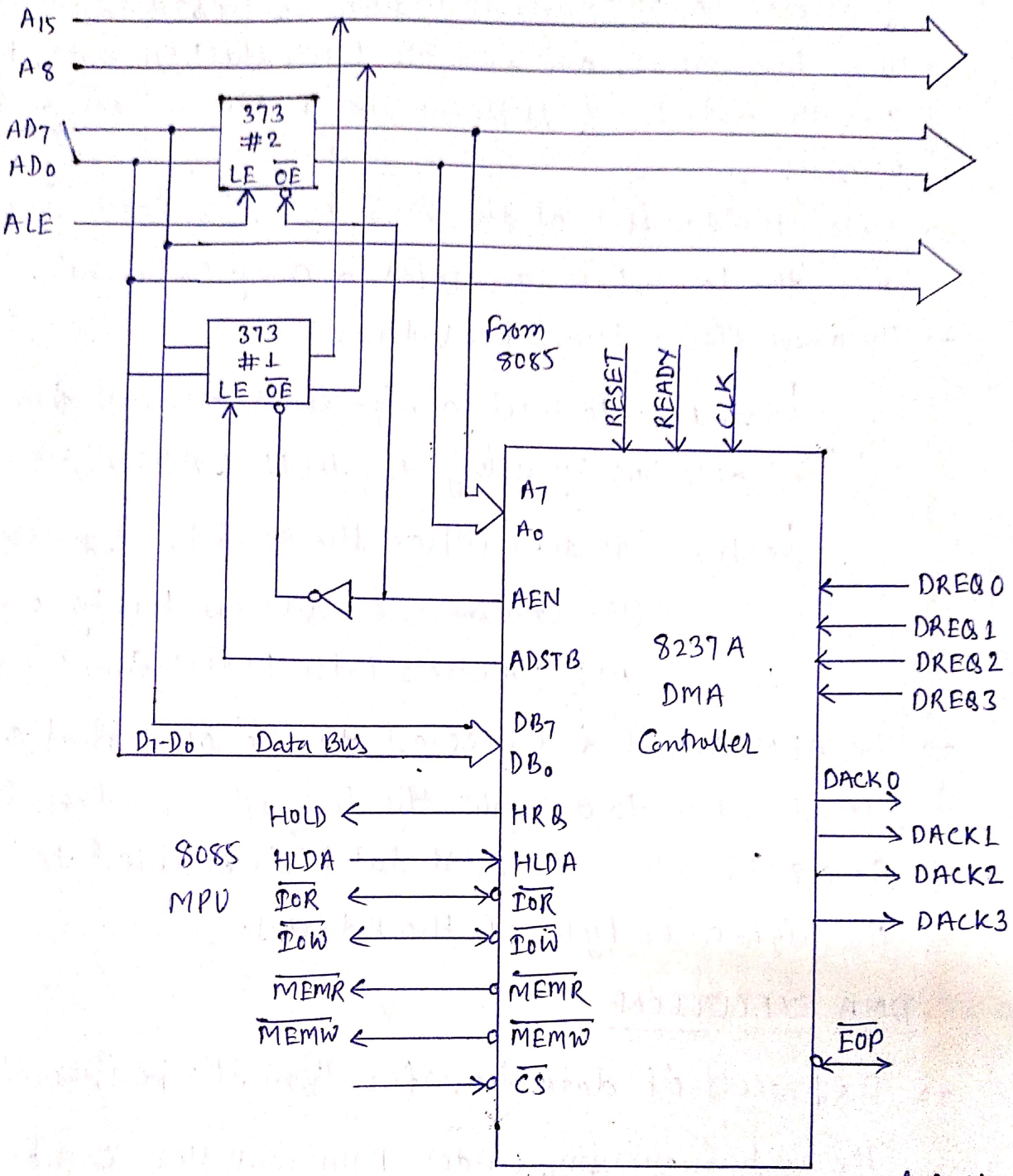
→ During the DMA cycle, these lines are used as o/p lines to generate low-order address that is combined with the remaining address lines A_7-A_4.

6) HRQ & HLDA (Hold Request & Hold Acknowledge)

→ HRQ is an o/p signal used to request the MPU control of the system bus.

→ After receiving the HRQ, the MPU completes the bus cycle in process & issues the HLDA signal.

SYSTEM INTERFACE



→ The DMA is used to transfer data bytes b/w I/O & system memory at high speed.

→ It includes
- ↳ 8 data lines
- ↳ four control signal ($\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ & $\overline{MEMW}$)
- ↳ 8-Address lines (A_7-A_0)

→ It needs 16 address lines to access 64k bytes, therefore an additional eight lines must be generated as shown in fig.