Synchronous & Asynchronous Sequential Circuits

Unit: 4

DIGITAL LOGIC & CIRCUIT DESIGN

SUBJECT CODE: ACSE0304

B Tech 3rd Semester

Mohammad Raza

Assistant Professor

Department of Electronics and Communication Engineering

Course Contents / Syllabus

UNIT-I: Digital System and Binary Numbers: Number System and its arithmetic, Signed binary numbers, Binary codes, Cyclic codes, Hamming Code, Simplification of Boolean Expression: K-map method up to five variable, SOP and POS Simplification Don't Care Conditions, NAND and NOR implementation, Quine Mc-Clusky Method (Tabular Method).

UNIT II : Combinational Logic: Combinational Circuits: Analysis Procedure, Design Procedure, Code Converter, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders Multiplexers, Demultiplexers.

UNIT III: Sequential Logic and Its Applications: Storage elements: Latches & Flip Flops, Characteristic Equations of Flip Flops, Excitation Table of Flip Flops, Flip Flop Conversion, Registers, Shift Registers, Ripple Counters, Synchronous Counters, Other Counters: Johnson & Ring Counter.

UNIT IV: Synchronous & Asynchronous Sequential Circuits: Analysis of clocked Sequential Circuits with State Machine Designing, State Reduction and Assignments, Design Procedure. Analysis procedure of Asynchronous Sequential Circuits, Circuit with Latches, Design Procedure, Reduction of State and flow Table, Race-free State Assignment, Hazards.

UNIT-V: Memory & Programmable Logic Devices: Basic concepts and hierarchy of Memory, Memory Decoding, RAM: SRAM, DRAM, ROM: PROM, EPROM, Auxiliary Memories, PLDs: PLA, PAL; Circuit Implementation using ROM, PLA and PAL; CPLD and FPGA..

Branch wise Application

- Shift registers

- Flip flops

- Analog to digital and digital to analog converters

- Counters

- Clocks

- Used as registers inside microprocessors and controllers to store temporary information

- Applied in programmable devices such as CPLD, PLD, and FPGA

- This course is intended to provide the students with a comprehensive understanding of the fundamental of digital logic circuit. The design of circuits and systems whose input and outputs are represented as discrete variables. These variables are commonly binary i.e.., two states in nature. Design at the circuit level is usually done with truth table and state tables. Students will be able to analyze design and implement combinational and sequential circuits.

https://www.youtube.com/watch?v=BoIOLczVulQ&list=PLyqSpQzTE6M_dZdF7Bd-UncI5_L_1VkXF

https://www.youtube.com/watch?v=oNh6V91zdPY&list=PLbRMhDVUMnge4gDT0vBWjCb3Lz0HnYKkX

https://www.youtube.com/watch?v=CeD2L6KbtVM&list=PL803563859BF7ED8C

Synchronous & Asynchronous Sequential Circuits: Analysis of clocked Sequential Circuits with State Machine Designing, State Reduction and Assignments, Design Procedure. Analysis procedure of Asynchronous Sequential Circuits, Circuit with Latches, Design Procedure, Reduction of State and flow Table, Race-free State Assignment, Hazards..

• Implement the Design procedure of Synchronous Sequential Circuits

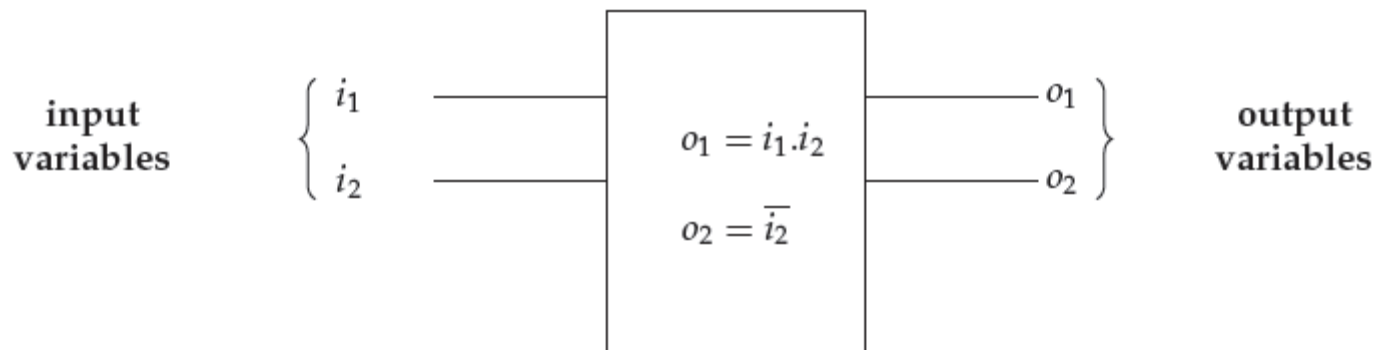• Implement the Design procedure of Asynchronous Sequential Circuits

Topic Objective/Topic outcome

- **Topic**: Analysis of clocked Sequential Circuits with State Machine Designing, State Reduction and Assignments, Design Procedure

- **CO Covered :** CO4
- **Topic Objective :** The objective of clocked Sequential Circuits to Design synchronous Sequential Circuits.

- **Topic outcome:** At the end of the course, the student will be able to Design synchronous Sequential Circuits.

Combinational circuits

- Consists only of logic gates
- The output are determined by the present value of input
- Circuit behavior specified by a set of Boolean functions, Truth-tables,
- K-maps
- We have learned techniques to analyze and synthesize such circuits

Examples: Adder, Multiplexers, Encoders, Decoders, etc.

input variables $\begin{cases} i_1 \\ i_2 \end{cases}$ $\quad\quad o_1 = i_1.i_2 \quad\quad o_2 = \overline{i_2}$ $\quad\quad \left.\begin{matrix} o_1 \\ o_2 \end{matrix}\right\}$ output variables

- FSM is a calculation model that can be executed with the help of hardware otherwise software.

- This is used for creating sequential logic as well as a few computer programs.

- FSMs are used to solve the problems in fields like mathematics, games, linguistics, and artificial intelligence.
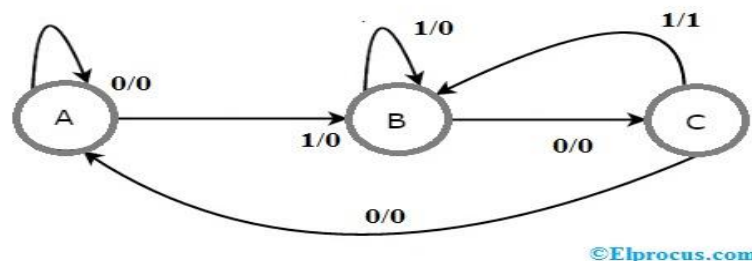
Types of Finite State Machine

- The finite state machines are classified into two types such as Mealy state machine and Moore state machine.

- Mealy State Machine

- When the outputs depend on the current inputs as well as states, then the FSM can be named to be a mealy state machine.

- The mealy state machine block diagram consists of two parts namely combinational logic as well as memory.
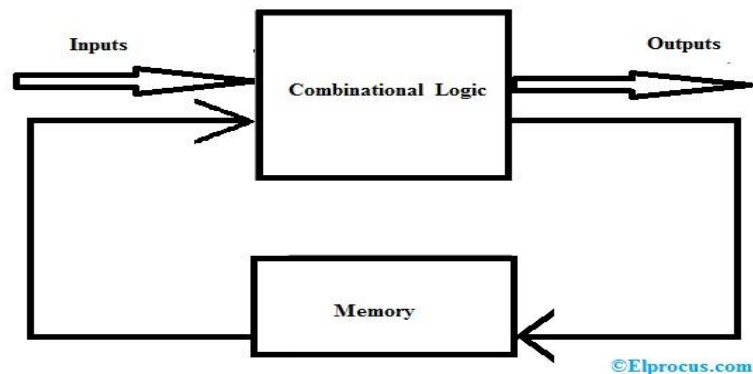
Based on the current inputs as well as states, this machine can produce outputs. Thus, the outputs can be suitable only at positive otherwise negative of the CLK signal.
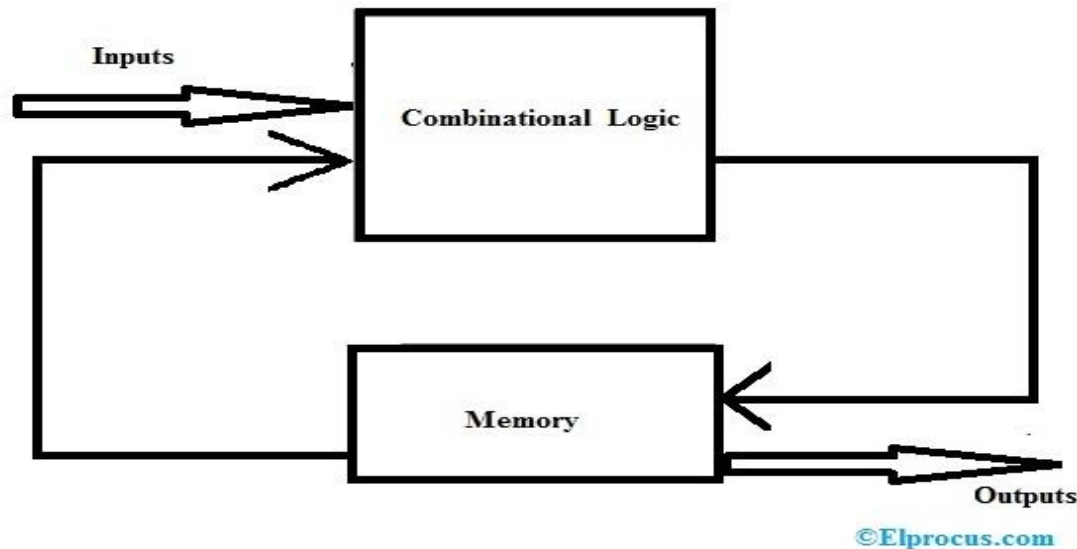
The mealy state machine's state diagram is shown below.

Moore State Machine

- When the outputs depend on current states then the FSM can be named as Moore state machine.

- The Moore state machine's block diagram is shown below.

- The Moore state machine block diagram consists of two parts namely combinational logic as well as memory.

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- In this case, the current inputs, as well as current states, will decide the next states.

- Thus, depending on further states, this machine will generate the outputs.

- So, the outputs of this will be applicable simply after the conversion of the state.

- The Moore state machine state diagram is shown below.

- The diagram includes four states like a mealy state machine namely A, B, C, and D, the four states as well as individual outputs are placed in the ci

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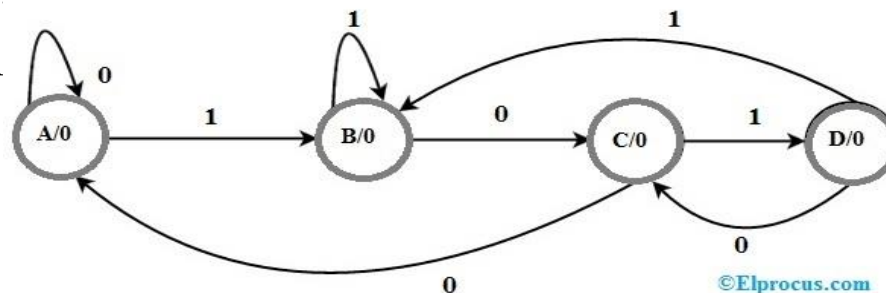
Video Links

- https://www.youtube.com/watch?v=AkO20k_my6k&ab_channel=NesoAcademyNesoAcademyVerified

- https://www.youtube.com/watch?v=Qa6csfkK7_I&ab_channel=NesoAcademy

- https://www.youtube.com/watch?v=0_OZKWdCixw&ab_channel=NesoAcademy

- The logic circuits whose outputs at any instant of time depends only on the state is called:

a) Mealy Machine
b) Moore's Machine

- How many types of sequential circuits are?
  a) 2
  b) 3
  c) 4
  d) 5

- The sequential circuit is also called _____
  a) Flip-flop
  b) Latch
  c) Strobe
  d) Adder

- Discuss Mealy and Moore FSM. What do you mean by excitation table?

- What do you mean by finite state machine?

- Following are the two types of sequential circuits −Asynchronous sequential circuits, Synchronous sequential circuits
  - If some or all the outputs of a sequential circuit do not change affect with respect to active transition of clock signal, then that sequential circuit is called as **Asynchronous sequential circuit**.
  - If all the outputs of a sequential circuit change affect with respect to active transition of clock signal, then that sequential circuit is called as Synchronous sequential circuit.
- The finite state machines are classified into two types such as Mealy state machine and Moore state machine.
- When the outputs depend on the current inputs as well as states, then the FSM can be named to be a mealy state machine.

Analysis of Clocked (Synchronous) Sequential Circuits

Topic Objective	Topic Outcomes	Mapping with CO
To have a basic understanding of state table, state diagram and state reduction.	Student will able to understanding of state table, state diagram and state reduction.	CO3
To analyze clocked synchronous sequential circuits.	Student will able to analyze clocked synchronous sequential circuits.	CO3

Prerequisite:

• Basic knowledge of latches & flip flops.

Analysis of Clocked (Synchronous) Sequential Circuits

State Table:

- The state table representation of a sequential circuit consists of three sections labeled present state, next state and output.

- The present state designates the state of flip-flops before the occurrence of a clock pulse.

- The next state shows the states of flip-flops after the clock pulse

- The output section lists the value of the output variables during the present state.

| Present State	Next State		Present Output
	X=0	X=1	
a	d	c	0
b	d	c	0
c	d	a	0
d	d	c	1

State Diagram:

- The information available directly from the state table can be represented graphically in a state diagram or state diagram is a pictorial view of state transitions.

  - State of flip-flop is represented by circle.

  - transition between states is indicated by directed line connecting the circles.

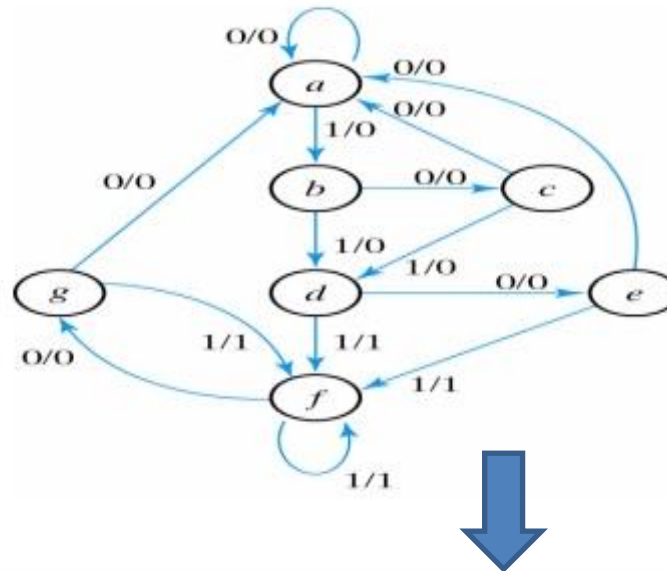 - Direct line connecting a circle with itself indicates that no change of state occur.
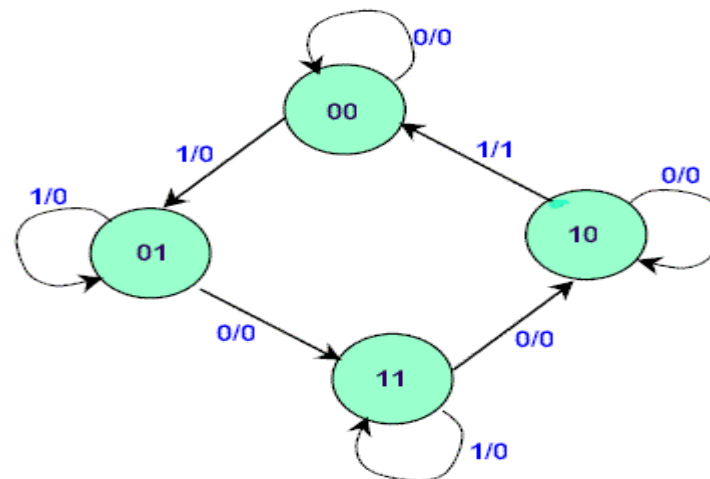
State Reduction: Suppose a sequential circuit is specified by the following seven-state diagram: An algorithm for the state reduction quotes that:
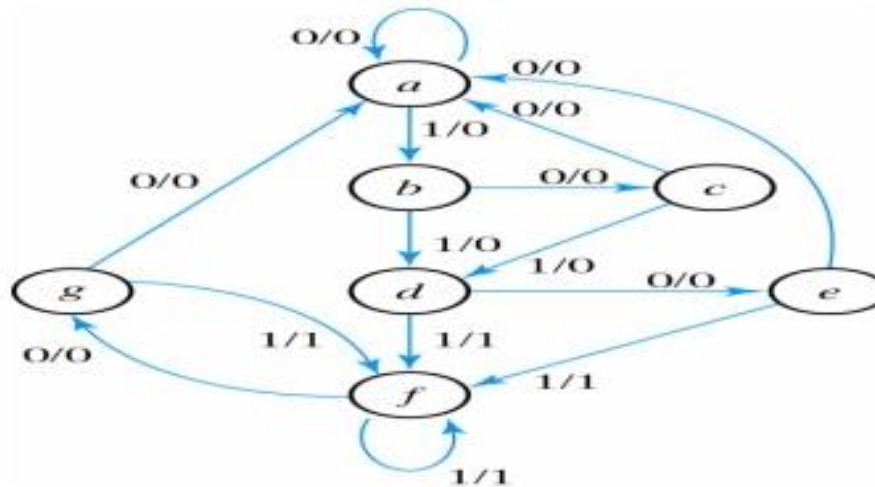
- "Two states are said to be equivalent if, for each member of the set of inputs, they give exactly the same output and send the circuit either to the same state or to an equivalent state."

- Now apply this algorithm to the state table of the circuit:

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

States g and e both go to states a and f and have outputs of 0 and 1 for x = 0 and x = 1, respectively. So replace the state g by e .

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

- Present state f now has next states e and f and outputs 0 and 1 for x= 0 and x = 1. Therefore, states f and d are equivalent and can be removed and replaced with d
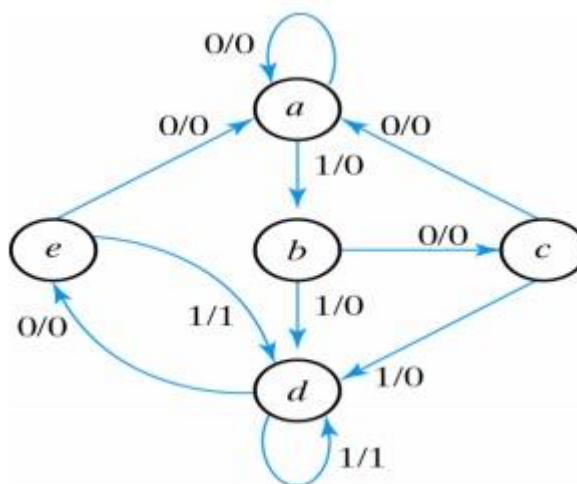
Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

- The final reduced state table is:

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

- The state diagram for the above reduced table is

Analysis of Synchronous Sequential Circuits

- We have a basic procedure for analyzing a clocked sequential circuit:

  - Write down the **equations** for the **outputs** and the **flip-flop inputs**.

  - Using these equations, derive a **state table** which describes the next state.

  - Obtain a **state diagram** from the **state table**.

- It is the state table and/or state diagram that specifies the **behavior** of the circuit.

- Notes:
  - The **flip-flop input equations** are sometimes called the **excitation equations**.
  - The **state table** is sometimes called a **transition table**.

Eg . Consider the following circuit. Draw the state table and the state diagram.

$$A_{(n+I)} = A_n x + B_n x$$
$$B_{(n+I)} = \overline{A_n} x$$
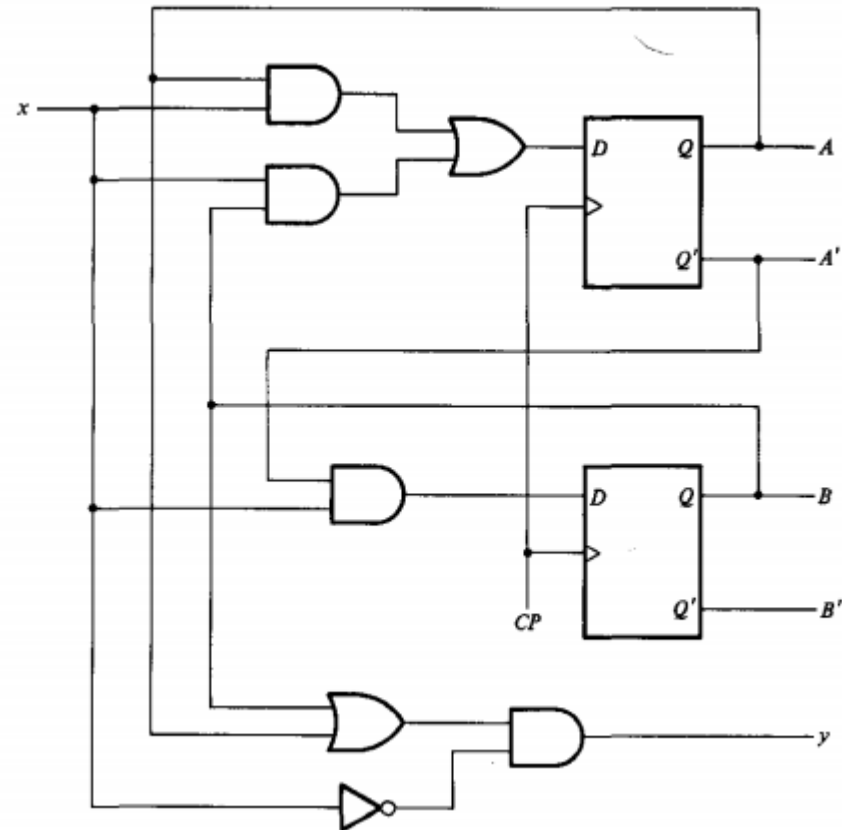
- Similarly, the present-state value of the output can be expressed algebraically as follows:

$$y = [A + B]x'$$

- The derivation of a state table consists of first listing all possible binary combinations of present state and inputs. In this case, we have eight binary combinations from 000 to 111.

- The next-state values are then determined from the logic diagram or from the state equations.

- The next state of flip-flop A must satisfy the state equation $A_{n+1} = Ax + Bx$.

TABLE 6-1
State Table for the Circuit of Fig. 6-16

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Analysis of Synchronous Sequential Circuits

TABLE 6-1
State Table for the Circuit of Fig. 6-16

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

TABLE 6-2
Second Form of the State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
AB	AB	AB	y	y
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0
11	00	10	1	0

- The information available in a state table can be represented graphically in a state diagram. In this type of diagram, a state is represented by a circle, and the transition between states is line

TABLE 6-2
Second Form of the State Table

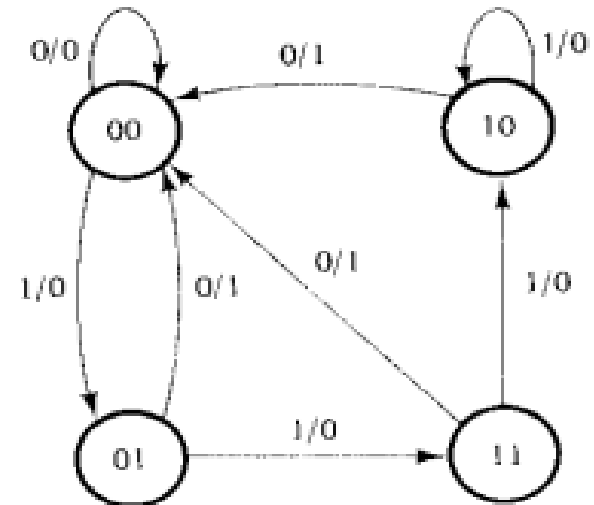| Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
AB	AB	AB	y	y
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0
11	00	10	1	0
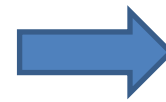
FIGURE 6-17
State diagram of the circuit of Fig. 6-16

Daily Quiz

- The table consists of present state and next state at input side and flipflop inputs at output side of the table is called:
  a) Truth Table

  b) Characteristic table

  c) Excitation table.

- Characteristics equation of S_R flip flop is:

  a) $Qn+1 = S + R \, Qn$

  b) $Qn+1 = S' + R \, Qn$

  c) $Qn+1 = S + R'Qn$

  d) $Qn+1 = S'+ R'Qn$

- What you understand by the term state table and state diagram?

- Why state reduction is done?

Old Questions

- Write the basic steps for analysis of clock sequential synchronous circuit.

- Derive the state table and state diagram of the synchronous sequential circuit shown below (X is an input to the circuit). Explain the circuit function.

Video Link

- https://nptel.ac.in/courses/117/106/117106086/
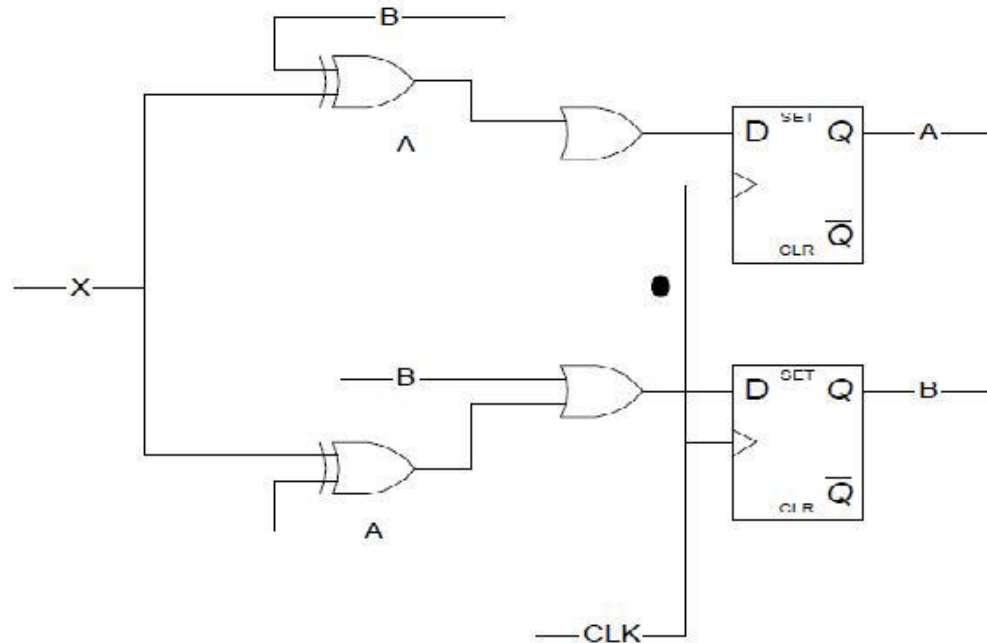
- https://www.youtube.com/watch?v=ntiv1g7G_C4&ab_channel=NesoAcademy

- https://www.youtube.com/watch?v=6jteVyUcAQU&ab_channel=NesoAcademy

Recap

- Basic procedure for analysis is:

  - Write down the **equations** for the **outputs** and the **flip-flop inputs**.

  - Using these equations, derive a **state table** which describes the next state.

  - Obtain a **state diagram** from the **state table**.

- It is the state table and/or state diagram that specifies the **behavior** of the circuit.

Design of Sequential Circuits

Topic Objective	Topic Outcome	Mapping with CO
To design clocked synchronous sequential circuits.	Student will able to design clocked synchronous sequential circuits.	CO3

Design of Sequential Circuits

Prerequisite:

• Basic knowledge of latches & flip flops.

Design of Sequential Circuits

Design of Sequential Circuits

- The design of a synchronous sequential circuit starts from a set of specifications in a logic diagram or a list of Boolean functions from which a logic diagram can be obtained. In contrast to a combinational logic, which is fully specified by a truth table, a sequential circuit requires a state table for its specification. The first step in the design of sequential circuits is to obtain a state table or an equivalence representation, such as a state diagram.

- A synchronous sequential circuit is made up of flip-flops and combinational gates. The design of the circuit consists of choosing the flip-flops and then finding the combinational structure which, together with the flip-flops, produces a circuit that fulfils the required specifications. The number of flip-flops is determined from the number of states needed in the circuit.
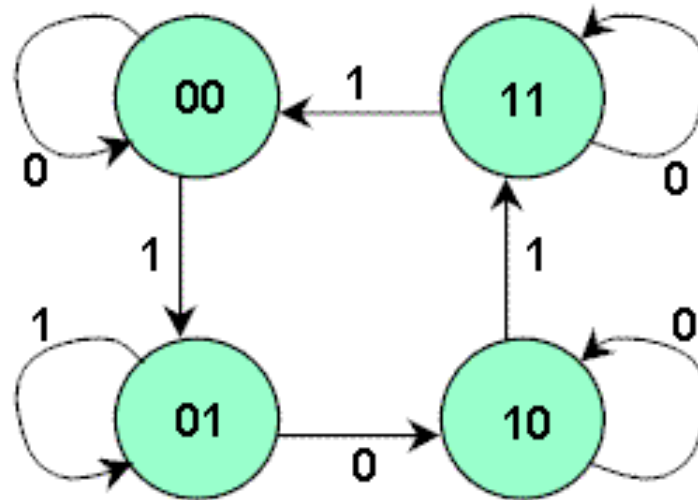
Design of Sequential Circuits

Example 1: Design a synchronous sequential circuit whose state diagram is shown in Figure. The type of flip-flop to be use is J-K.
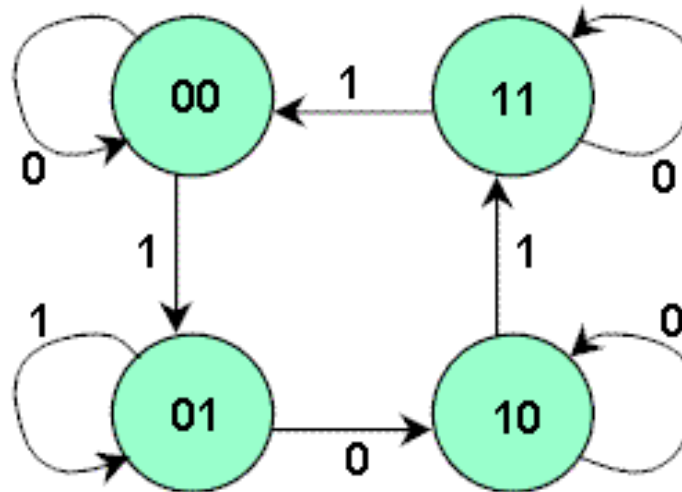
- From the state diagram, we can generate the state table shown in Table. Note that there is no output section for this circuit. Two flip-flops are needed to represent the four states and are designated $Q_0 Q_1$. The input variable is assumed as x.

Design of Sequential Circuits

State Table is derived from the state diagram

Present State	Next State	
$Q_0 Q_1$	x = 0	x = 1
0 0	0 0	0 1
0 1	1 0	0 1
1 0	1 0	1 1
1 1	1 1	0 0

Design of Sequential Circuits

We shall now derive the excitation table and the combinational structure. The table is now arranged in a different form where the present state and input variables are arranged in the form of a truth table.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table of JK flipflop

Design of Sequential Circuits

The combined table from the state table and excitation table is:

Present state	Next state	
Q_0Q_1	X=0	X=1
00	00	01
01	10	01
10	10	11
11	11	00

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Present State $Q_0 Q_1$	Next State $Q_0 Q_1$	Input x	Flip-flop Inputs J_0K_0	J_1K_1
0 0	0 0	0	0 X	0 X
0 0	0 1	1	0 X	1 X
0 1	1 0	0	1 X	X 1
0 1	0 1	1	0 X	X 0
1 0	1 0	0	X 0	0 X
1 0	1 1	1	X 0	1 X
1 1	1 1	0	X 0	X 0
1 1	0 0	1	X 1	X 1

Design of Sequential Circuits

The simplified Boolean functions for the combinational circuit can now be derived. The input variables are Q_0, Q_1, and x; the output are the variables J_0, K_0, J_1 and K_1. The information from the truth table is plotted on the Karnaugh maps shown in Figure
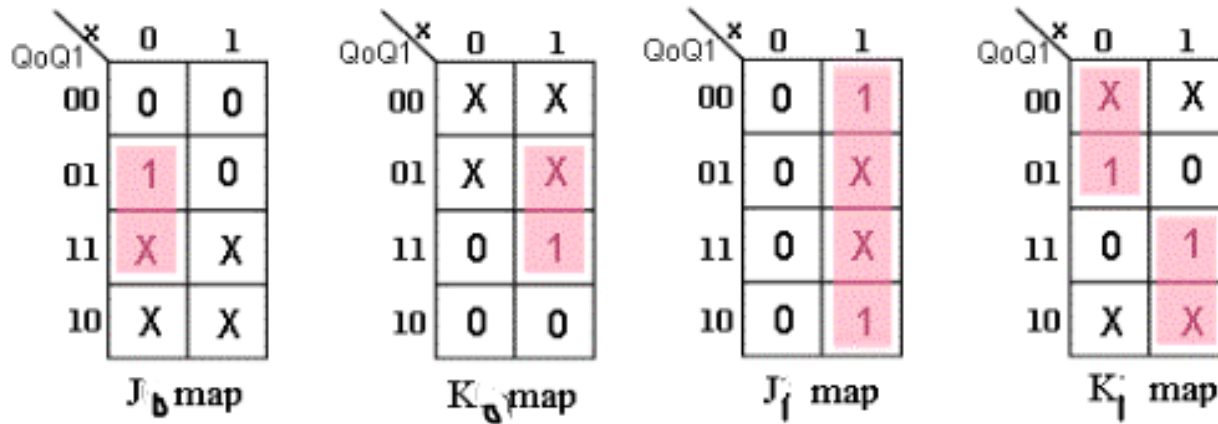
- The flip-flop input functions are derived:

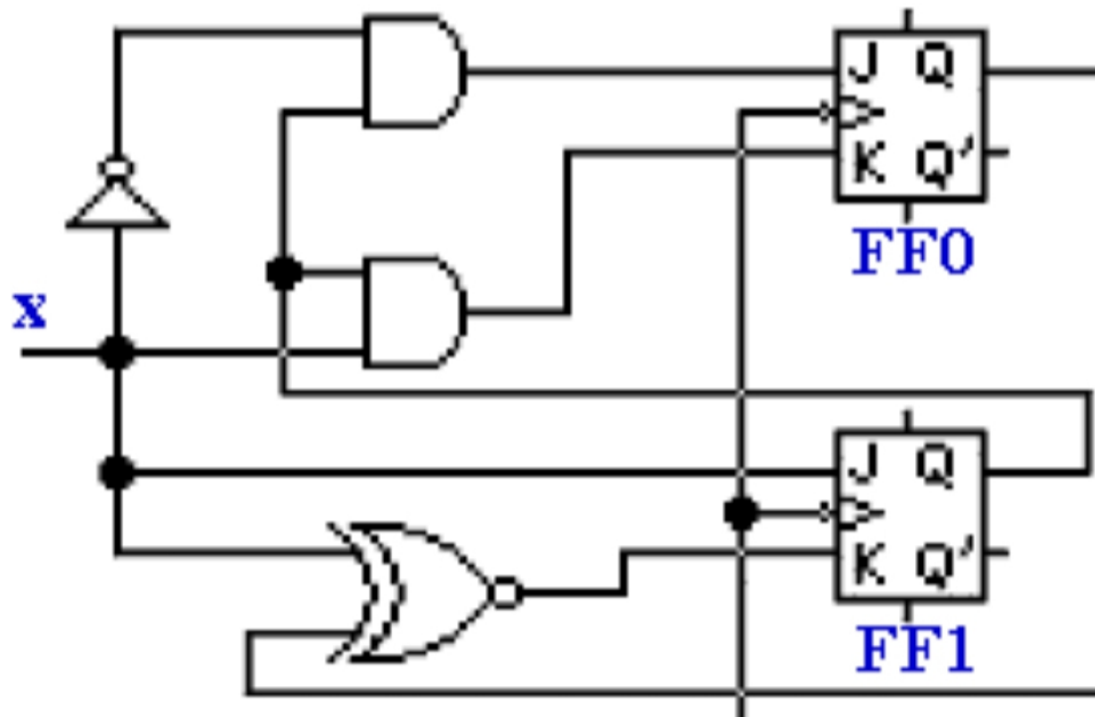$$J_0 = Q_1 \cdot x' \qquad K_0 = Q_1 \cdot x$$

$$J_1 = x \qquad K_1 = Q_0' \cdot x' + Q_0 \cdot x = Q_0 \odot x$$

Design of Sequential Circuits

- The logic diagram can be drawn from the given boolean equations:

$$J_0 = Q_1 \cdot x' \qquad K_0 = Q_1 \cdot x$$

$$J_1 = x \qquad K_1 = Q_0' \cdot x' + Q_0 \cdot x = Q_0 \odot x$$

Design of Sequential Circuits

Example 2: Design a synchronous sequential circuit whose state table is shown in Figure. The type of flip-flop to be use is D.

Present State $Q_0 Q_1$		Next State		Output	
		x = 0	x = 1	x = 0	x = 1
0 0		0 0	0 1	0	0
0 1		0 0	1 0	0	0
1 0		1 1	1 0	0	0
1 1		0 0	0 1	0	1

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

- As we have to use D flip-flop, the excitation table of D Flip-flop is:

Design of Sequential Circuits

The combined table from the state table and excitation table is:

Present State	Next State		Output	
$Q_0 Q_1$	x = 0	x = 1	x = 0	x = 1
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	1 1	1 0	0	0
1 1	0 0	0 1	0	1

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State	Next State	Input	Flip-flop Inputs		Output
$Q_0 Q_1$	$Q_0 Q_1$	x	D_0	D_1	Z
0 0	0 0	0	0	0	0
0 0	0 1	1	0	1	0
0 1	0 0	0	0	0	0
0 1	1 0	1	1	0	0
1 0	1 1	0	1	1	0
1 0	1 0	1	1	0	0
1 1	0 0	0	0	0	0
1 1	0 1	1	0	1	1

The simplified Boolean functions for the combinational circuit can now be derived. The input variables are Q_0, Q_1, and x; the output are the variables J_0, K_0, J_1 and K_1. The information from the truth table is plotted on the Karnaugh maps shown in Figure
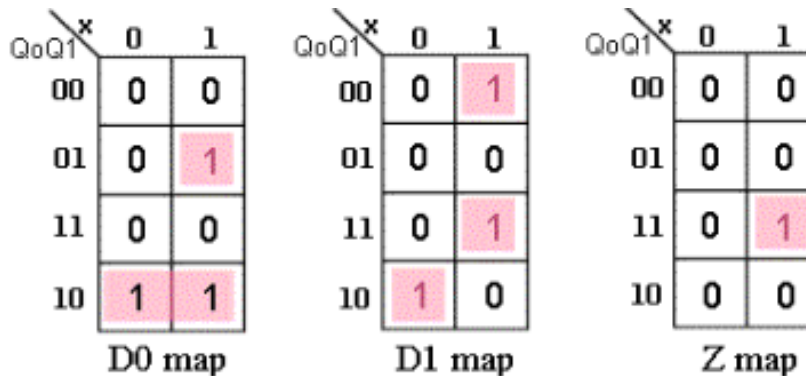

Karnaugh maps

- The flip-flop input functions are derived:

$$D_0 = Q_0 . Q_1' + Q_0' . Q_1 . x$$

$$D_1 = Q_0' . Q_1' . x + Q_0 . Q_1 . x + Q_0 . Q_1' . x'$$

$$Z = Q_0 . Q_1 . x$$

Design of Sequential Circuits

- The logic diagram can be drawn from the given boolean equations:

$$D_0 = Q_0 \cdot Q_1' + Q_0' \cdot Q_1 \cdot x$$

$$D_1 = Q_0' \cdot Q_1' \cdot x + Q_0 \cdot Q_1 \cdot x + Q_0 \cdot Q_1' \cdot x'$$
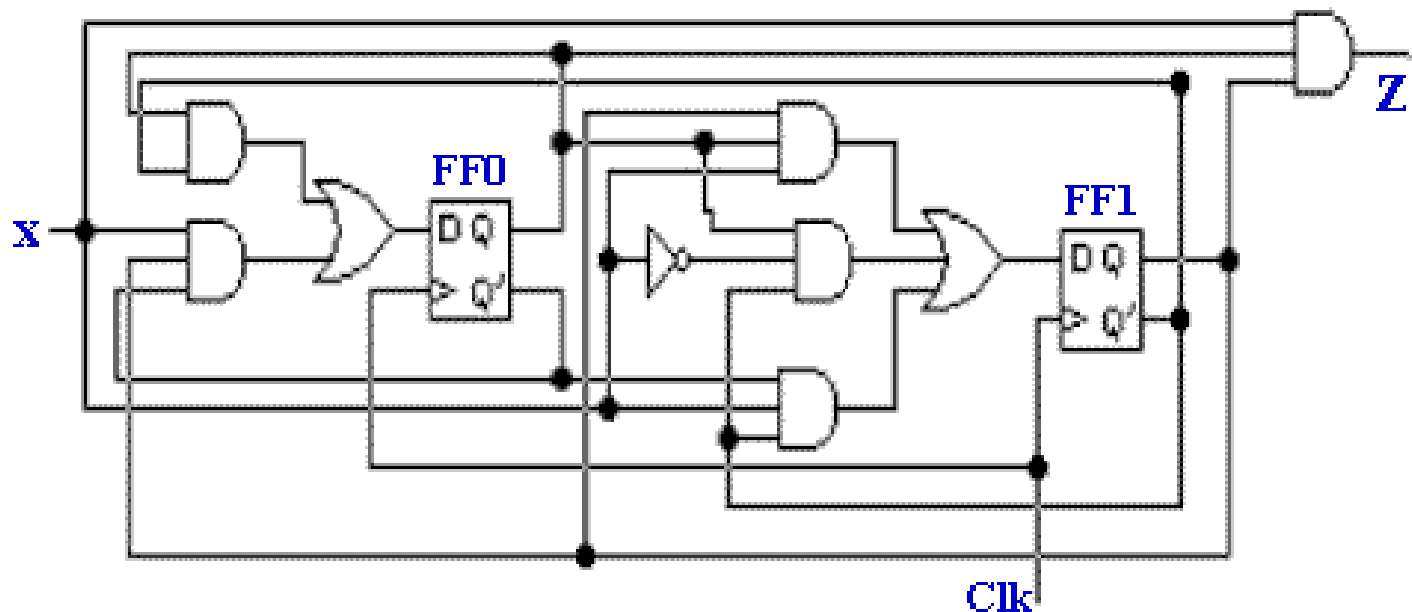
$$Z = Q_0 \cdot Q_1 \cdot x$$

Daily Quiz

- The table consists of present state and next state at input side and flipflop inputs at output side of the table is called:
  a) Truth Table

  b) Characteristic table

  c) Excitation table.

- Characteristics equation of S_R flip flop is:

  a) $Q_{n+1} = S + R\ Q_n$

  b) $Q_{n+1} = S' + R\ Q_n$

  c) $Q_{n+1} = S + R'Q_n$

  d) $Q_{n+1} = S'+ R'Q_n$

- What you understand by the term state table and state diagram?

Daily Assignment

- Write the basic steps for designing of clock sequential synchronous circuit.

- Design a sequential circuit with two flip flop A and B and one input x. When x=0 the state of the circuit remains the same when x = 1 the circuit passes through the state transition from 00 to 01 to 11 to 10 and back to 00 and repeat.

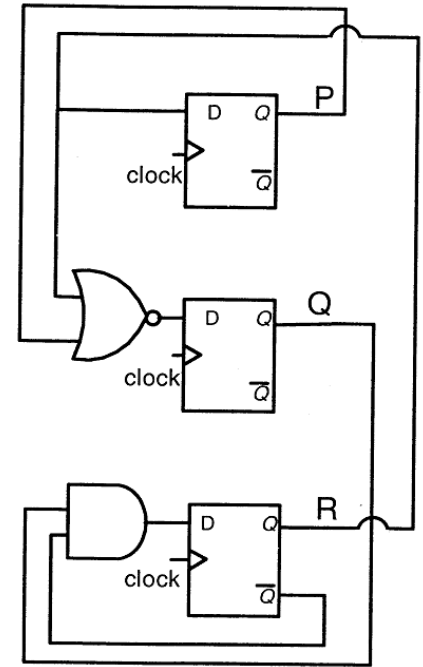- Design a sequential circuit for a given state diagram

Video Link

- https://nptel.ac.in/courses/117/106/117106086/
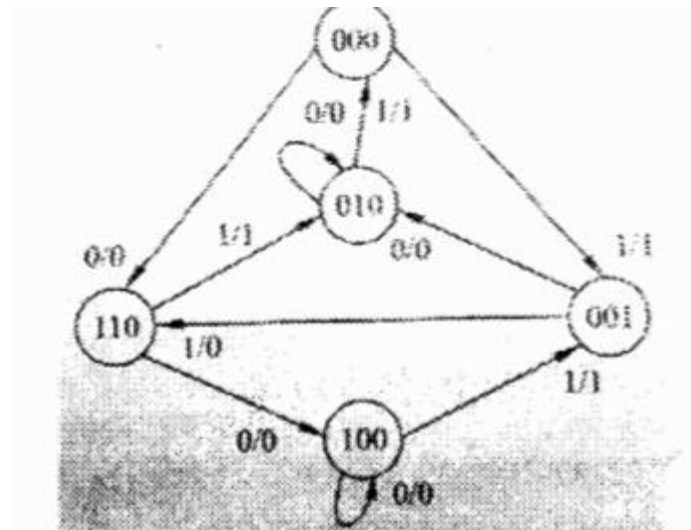
- https://www.youtube.com/watch?v=OGgLiGXHrsw&ab_channel=RajaramStudy

- https://www.youtube.com/watch?v=NbON135lf60&ab_channel=NesoAcademy

- Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.

- Design a sequential circuit for the given state diagram using JK flip flops.
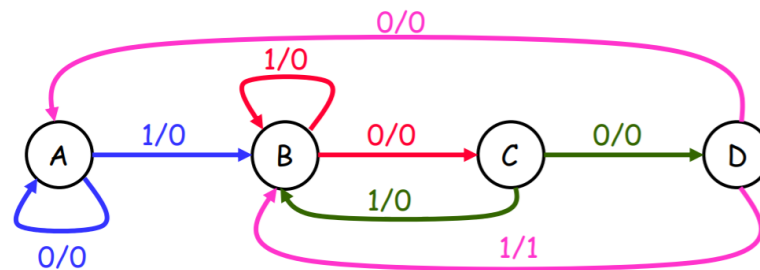
Recap

- The design of a synchronous sequential circuit starts from a set of specifications in a logic diagram or a list of Boolean functions from which a logic diagram can be obtained.

- The first step in the design of sequential circuits is to obtain a state table or an equivalence representation, such as a state diagram.

- A synchronous sequential circuit is made up of flip-flops and combinational gates.

- The design of the circuit consists of choosing the flip-flops and then finding the combinational structure which, together with the flip-flops, produces a circuit that fulfils the required specifications.

- The number of flip-flops is determined from the number of states needed in the circuit.

The procedure for designing synchronous sequential circuits:

1. From the word description and specification of the desired operation, derive a state diagram for the circuit.
2. Reduce the number of states if necessary.
3. Assign binary values to the states.
4. Obtain the binary-coded state table.
5. Choose the type of flip-flops to be used.
6. Derive the simplified flip-flop input equations and output equations.
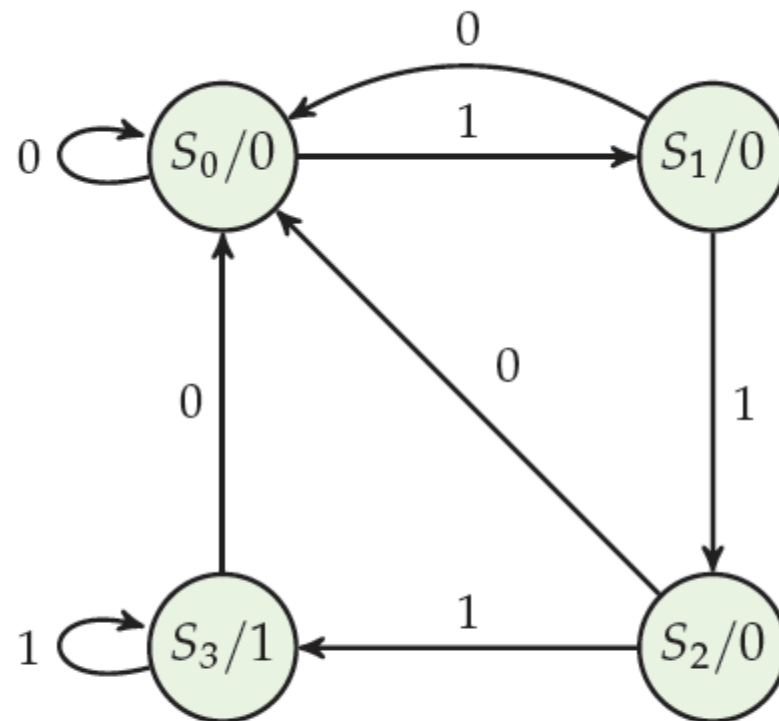7. Draw the logic diagram.

Derive state diagrams for the following problems:

1. **Sequence Detector: Design a circuit that detects a sequence of three** of more consecutive 1's.
2. **Binary Counter: Design a circuit for three-bit binary counter.**
3. **Binary Counter: Design a circuit for three-bit binary counter with one** input w such that if w = 0 the count remains, and if w = 1 the count is incremented.
4. **Up-and-Down Binary Counter: Design a circuit for three-bit binary** counter with one input w such that if w = 0 the count is decremented, and if w = 1 the count is incremented.
5. **Even-Parity Checker: Design a circuit for even-parity checker with** two inputs w and reset, and one output z such that z = 1 if the number of times sigma w has been 1's since the previous reset is even.
6. Outputs 1 whenever the input bit sequence has exactly two 0s in the last three input bits.
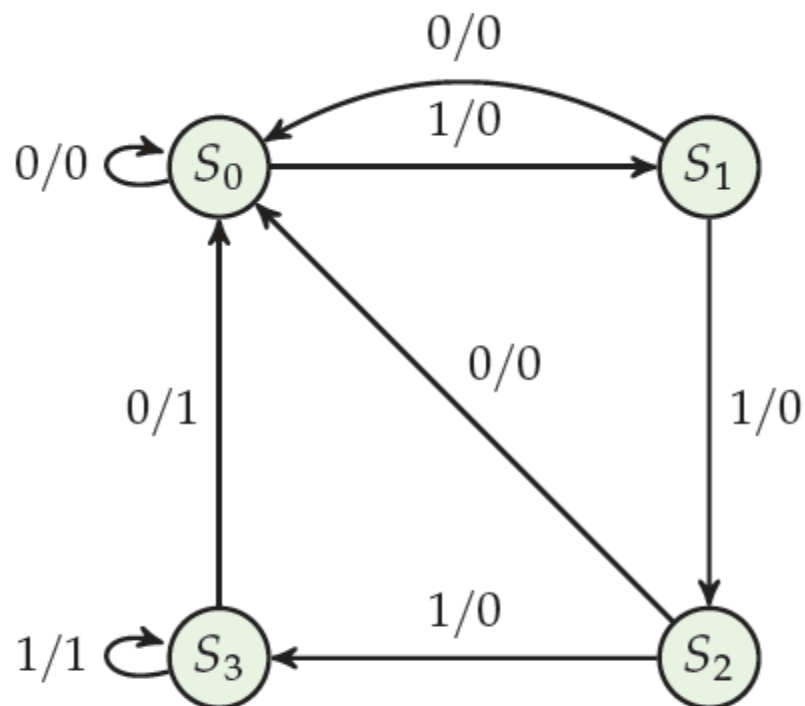
a) Mealy machine

b) Moore machine

State reduction is desirable since it may reduces the number of
flip-flop required to implement the circuit.

– Two states are said to be equivalent if, for each member of the set of
input, they give exactly same output and send the circuit either to
same state or to an equivalent state.

– When two states are equivalent, one of them can be removed without
changing the function of the circuit.

– It is difficult to tell whether two states are equivalent, but slightly
easy to tell when they are not equivalent.

– Assign unique binary values to states

– For n states we need at least $\lceil log_2(n) \rceil$ variables to encode the states.

– Three possible binary state assignments:

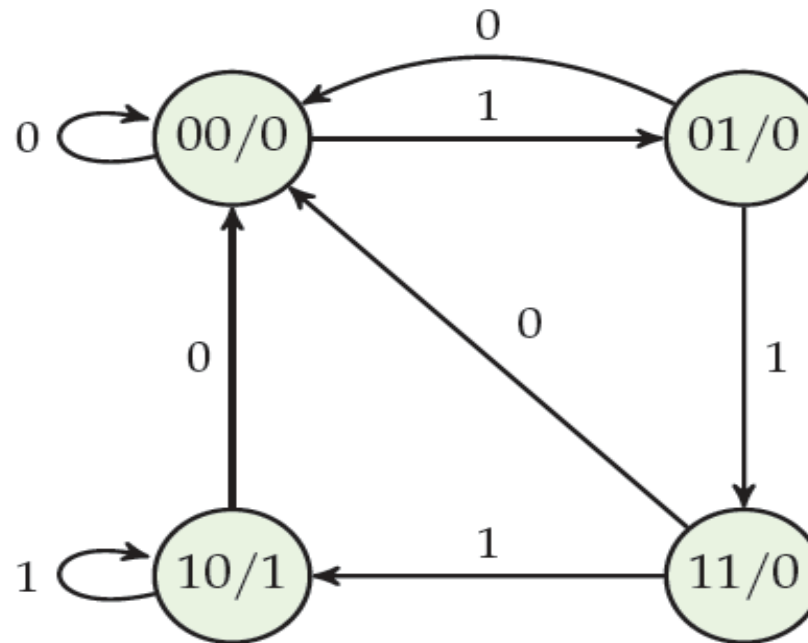| State	Binary	Gray Code	One-Hot
a	000	000	00001
b	001	001	00010
c	010	011	00100
d	011	010	01000
e	100	110	10000

– In which situations you would prefer binary, gray, or one-hot encoding?

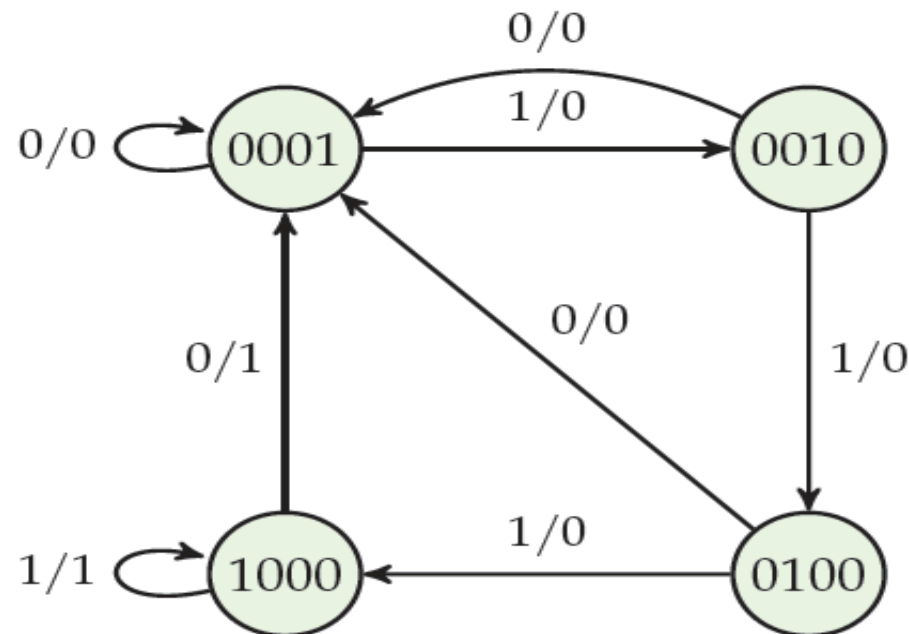# Example 1: Sequence Detector
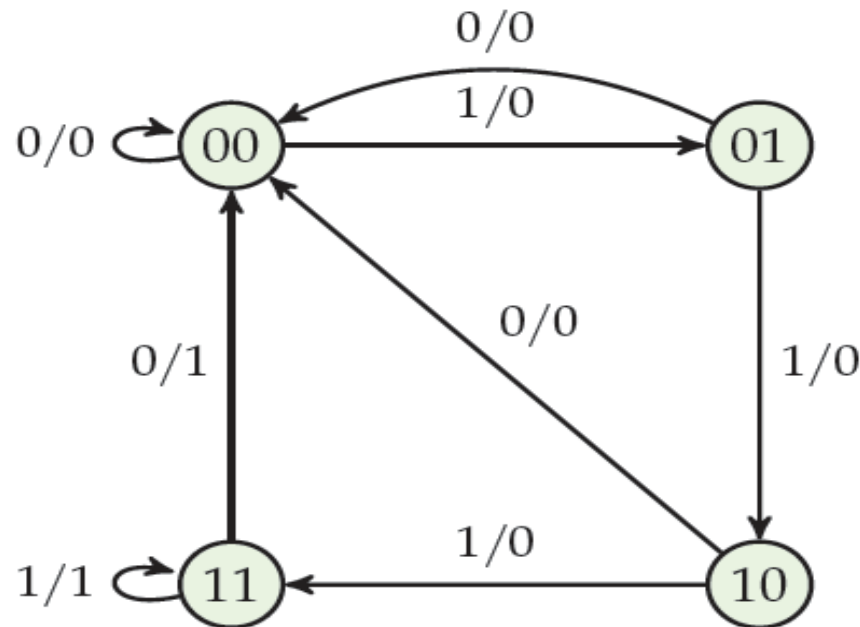
a) Mealy machine with Binary Assignment

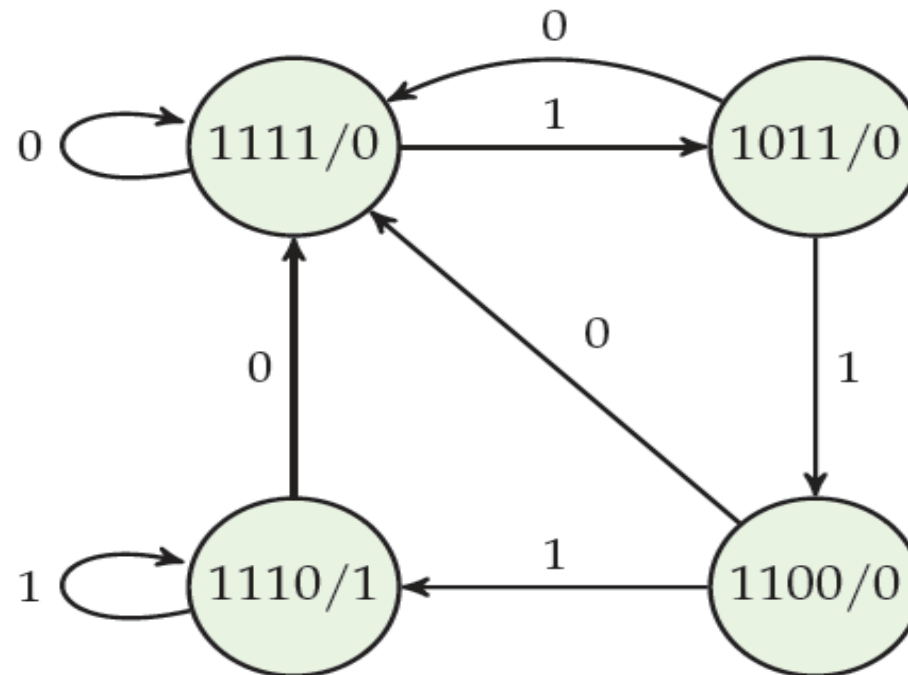# Example 1: Sequence Detector

b) Moore machine with Gray Code Assignment

Example 1: Sequence Detector

c) Mealy machine with One-Hot Assignment

Example 1: Sequence Detector

d) Moore machine with Arbitrary Assignment

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

– We need to store each state as a flip-flop such as D, J-K or T flip flops.

– We need to compute input logic for our flip-flops in order to properly change the state.

– A excitation table defines the logical properties of the input of a flip-flop in order to make a desired change in the input.

– J-K Flip-flop

$Q(t)$	$Q(t+1)$	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

– T Flip-flop

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

– D Flip-flop

- Using excitation table and state table, derive state table for
- corresponding flip-flop inputs
- – Using K-maps simplify the flip-flop input equations and the output
- equations
- – Draw the logic diagram.

- The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____
- Combinational circuits
- Sequential circuits
- Latches
- Flip-flops

- Whose operations are more faster among the following?
- Combinational circuits
- Sequential circuits
- Latches
- Flip-flops

- What is a trigger pulse?
- A pulse that starts a cycle of operation
- A pulse that reverses the cycle of operation
- A pulse that prevents a cycle of operation
- A pulse that enhances a cycle of operation

- Reset is a signal that is used for the initialization of the hardware.(T/F)

- Synchronous reset is a fast reset. (T/F)

- The reduction of flip-flops in a sequential circuits are referred as state reduction. (T/F)

- What do you mean by state-transition diagram?

- What is the necessity of reducing the number of states?

- Explain the categories of state machines.

- Explain state table and state diagram with the help of an example

- Explain the rules for state assignment of synchronous sequential circuit.

- https://www.youtube.com/watch?v=MiuMYEn3dpg

- https://www.youtube.com/watch?v=ibQBb5yEDlQ

- https://www.youtube.com/watch?v=NfXkffUivKQ

Topic Objective/Topic outcome

- **Topic**: Analysis procedure of Asynchronous Sequential Circuits
-

- **CO Covered :** CO4
- **Topic Objective :** The objective of asynchronous Sequential Circuits to Design and analysis of asynchronous Sequential Circuits.

- **Topic outcome:** At the end of the course, the student will be able to analyze and design asynchronous Sequential Circuits.

Synchronous vs. Asynchronous

- **Asynchronous sequential circuits ,,**

- Internal states can change at any instant of time when there is a change in the input variables ,,

- No clock signal is required

- Have better performance but hard to design due to timing problems

- **Synchronous sequential circuits ,,**

- Synchronized by a periodic train of clock pulses ,,

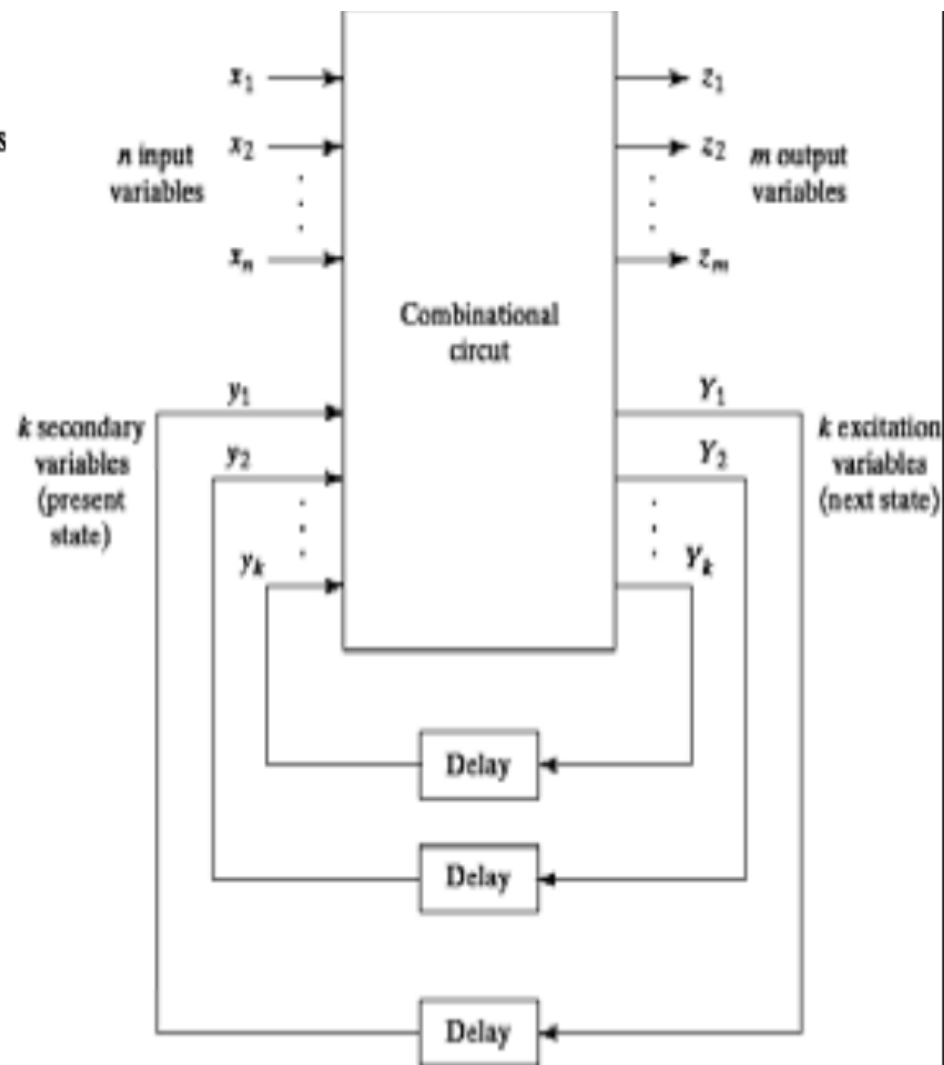- Much easier to design
 (preferred design style)
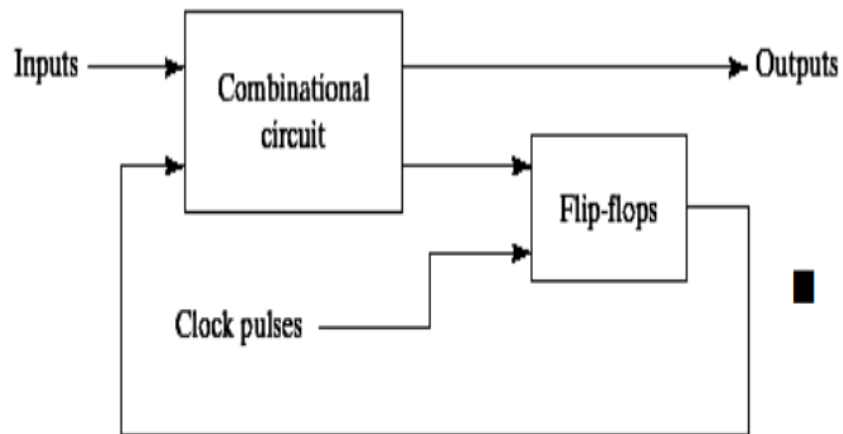
(a) Block diagram

(b) Timing diagram of clock pulses

Why Asynchronous Circuits ?

- Used when speed of operation is important ,,

  Response quickly without waiting for a clock pulse ,,

- Used in small independent systems ,,

  Only a few components are required ,,

- Used when the input signals may change

  independently of internal clock ,Asynchronous in nature ,,

- Used in the communication between two units that have their own independent clocks ,,

  Must be done in an asynchronous fashion

- **‚Steady-state condition**: „
- Current states and next states are the same
- ‚Difference between Y and y will cause a transition „

- **Fundamental mode: „**
- No simultaneous changes of two or more variables „
- The time between two input changes must be longer than the time it takes the circuit to a stable state „
- The input signals change one at a time and only when the circuit is in a stable condition

- Transition table is useful to analyze an asynchronous circuit from the circuit diagram „

- Procedure to obtain transition table:

1. Determine all feedback loops in the circuits

2. Mark the input (y_i) and output (Y_i) of each feedback loop

3. Derive the Boolean functions of all Y's

4. Plot each Y function in a map and combine all maps into one table

5. Circle those values of Y in each square that are equal to the value of y in the same row

An Example of Transition Table

$Y_1 = xy_1 + x'y_2$

$Y_2 = xy'_1 + x'y_2$

inputs

current states

$Y = Y_1Y_2$

stable !!

(a) Map for $Y_1 = xy_1 + x'y_2$

(b) Map for $Y_2 = xy'_1 + x'y_2$

(c) Transition table

9-1f
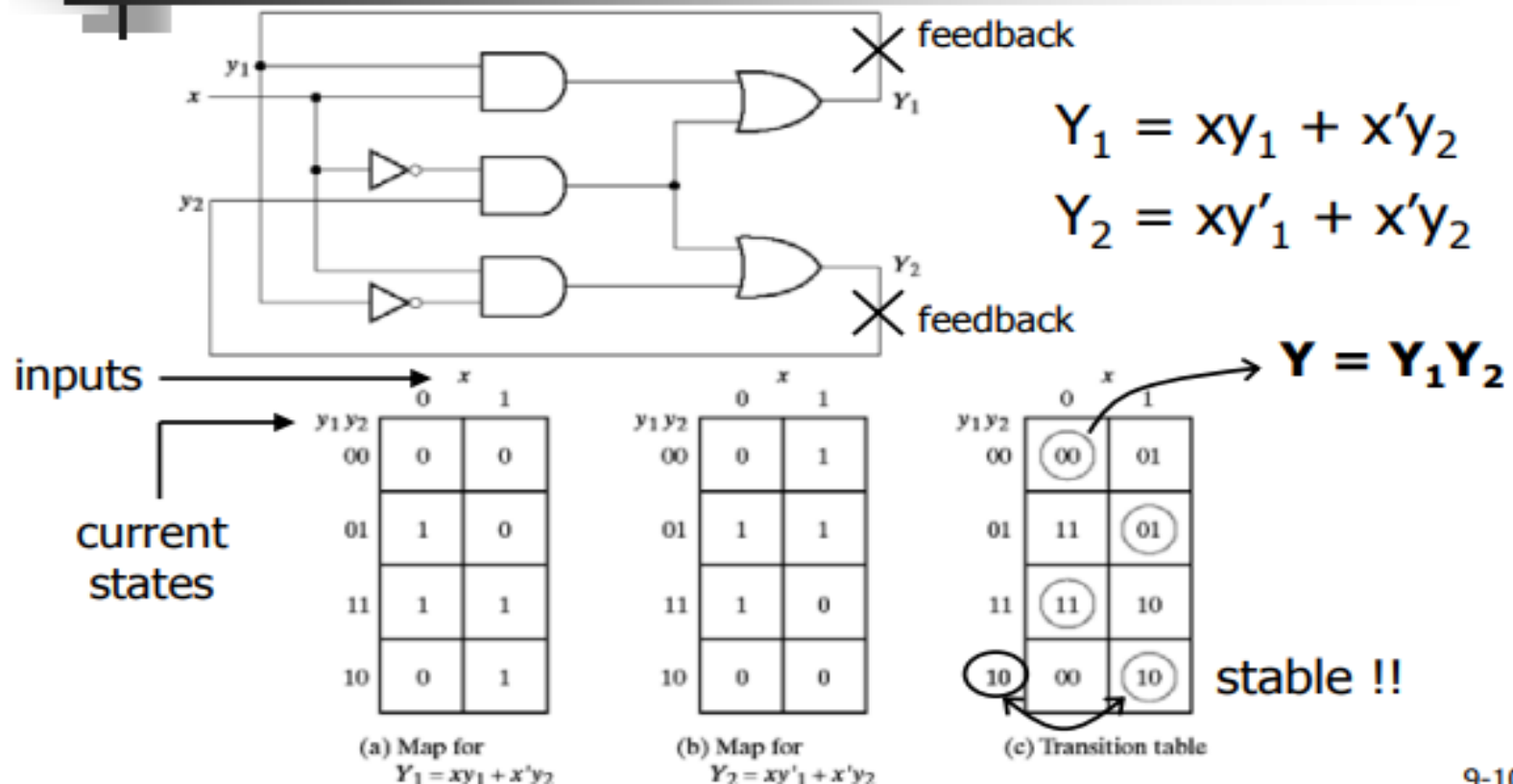
- When input x changes from 0 to 1 while y=00:
  - Y changes to 01 → unstable
  - y becomes 01 after a short delay → stable at the second row
  - The next state is Y=01
- Each row must have **at least one** stable state
- Analyze each state in this way can obtain its state table
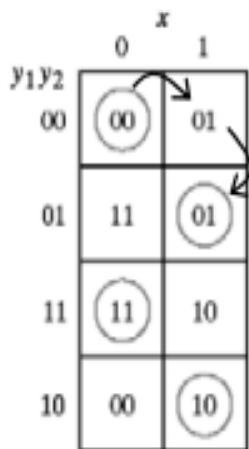
Present State		Next State				y_1y_2x : total state
		X=0		X=1		
0	0	0	0	0	1	4 stable total states: 000,011, 110,101
0	1	1	1	0	1	
1	0	0	0	1	0	
1	1	1	1	1	0	

- Procedure to obtain circuits from flow table:
    - Assign to each state a distinct binary value (convert to a transition table)
    - Obtain circuits from the map
- Two difficulties:
    - The binary state assignment (to avoid race)
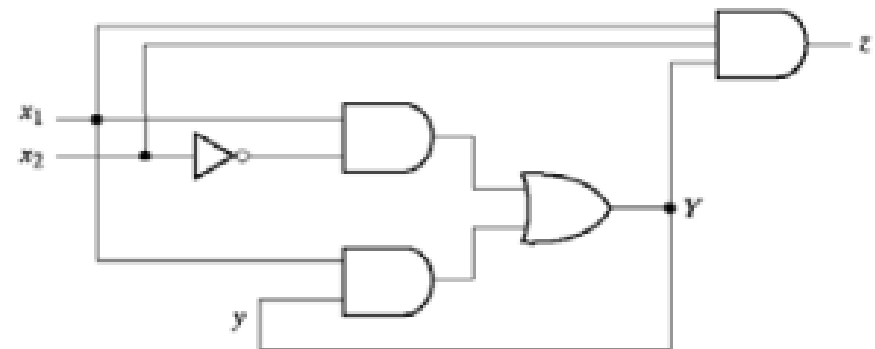   - The output assigned to the unstable states

Ex: from the flow table 9-4(b)

(a) Transition table
$Y = x_1 x_2' + x_1 y$

(b) Map for output
$z = x_1 x_2 y$

(c) Logic diagram

(a) Possible transitions:

$00 \rightarrow 11$
$00 \rightarrow 01 \rightarrow 11$
$00 \rightarrow 10 \rightarrow 11$

(b) Possible transitions:

$00 \rightarrow 11 \rightarrow 01$
$00 \rightarrow 01$
$00 \rightarrow 10 \rightarrow 11 \rightarrow 01$

(a) Possible transitions:

$00 \rightarrow 11$
$00 \rightarrow 01$
$00 \rightarrow 10$

(b) Possible transitions:

$00 \rightarrow 11$
$00 \rightarrow 01 \rightarrow 11$
$00 \rightarrow 10$

- Race condition:
  - **two or more** binary state variables will change value when one input variable changes
  - Cannot predict state sequence if unequal delay is encountered

- Non-critical race:
  - The final stable state **does not** depend on the change order of state variables

- Critical race:
  - The change order of state variables will result in **different** stable states
  - Should be avoided !!

9-14

Race can be avoided by proper state assignment

- Direct the circuit through intermediate unstable states with a unique state-variable change
- It is said to have a **cycle**

Must ensure that a cycle will terminate with a stable state

- Otherwise, the circuit will keep going in unstable states

(a) State transition:
$00 \rightarrow 01 \rightarrow 11 \rightarrow 10$

(b) State transition:
$00 \rightarrow 01 \rightarrow 11$

(c) Unstable

- Asynchronous circuit is also called _____ circuit.
- Combinational
- Self-timed
- Clock circuit
- Delayed

- How many different states does a 3-bit asynchronous down counter have?
- 2
- 4
- 6
- 8

Which of the following statements are true?

- **Asynchronous events does not occur at the same time**
- Asynchronous events are controlled by a clock
- Synchronous events does not need a clock to control them Only
- asynchronous events need a control clock

Memory elements in asynchronous circuits are Unclocked flip-flops

- **TRUE**
- FALSE

Internal propagation delay of asynchronous counter is removed by

- Ripple counter
- Ring counter
- Modulus counter
- **Synchronous counter**

- Explain the effect of propagation delay in asynchronous counters.

- What are the steps for an asynchronous sequential circuit design?

- Draw the block diagram of asynchronous segmental circuit and explain its working. Also list the different techniques used for state assignment.

- Design a 4-bit asynchronous counter with provision for asynchronous loading.

- Explain which sequential circuits are difficult to design and why?

- https://www.youtube.com/watch?v=MiuMYEn3dpg

- https://www.youtube.com/watch?v=ibQBb5yEDlQ

- https://www.youtube.com/watch?v=NfXkffUivKQ

- **Topic**: Circuit with Latches, Design Procedure, Reduction of State and flow Table, Race-free State Assignment, Hazards.

- **CO Covered :** CO4

- **Topic Objective :** The objective of Circuit with Latches, Design Procedure, Reduction of State and flow Table, Race-free State Assignment, Hazards is to Design a Circuit with Latches, Design Procedure, Reduction of State and flow Table, Race-free State Assignment, Hazards.

-

- **Topic outcome:** At the end of the course, the student will be able to Design a Circuit with Latches, Design Procedure, Reduction of State and flow Table, Race-free State Assignment, Hazards.

- The traditional configuration of asynchronous

circuits is using one or more feedback loops

No real delay elements

- It is more convenient to employ the SR latch as

  a memory element in asynchronous circuits

  Produce an orderly pattern in the logic diagram with the memory elements clearly visible.

- SR latch is also an asynchronous circuit

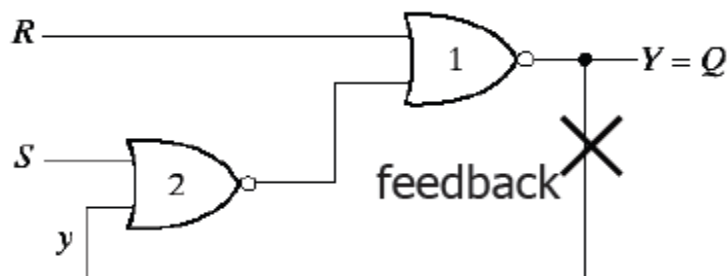   Will be analyzed first using the method for asynchronous circuits
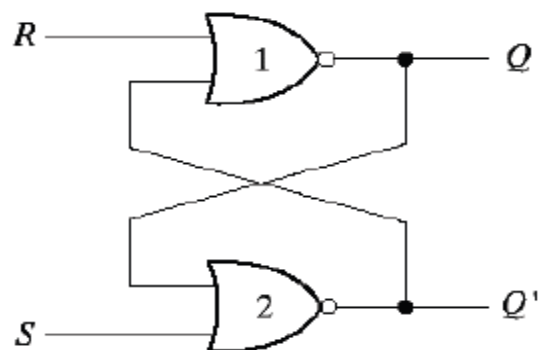
(a) Crossed-coupled circuit

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(After $SR = 10$)
0	1	0	1	
0	0	0	1	(After $SR = 01$)
1	1	0	0	

(b) Truth table

(c) Circuit showing feedback

SR

y	00	01	11	10
0	0	0	0	1
1	1	0	0	1

S=1, R=1 (SR = 1) should not be used ⇒ SR = 0 is normal mode

$Y = SR' + R'y$

$Y = S + R'y$ when $SR = 0$ ⟶ * should be carefully checked first

(d) Transition table

9-19
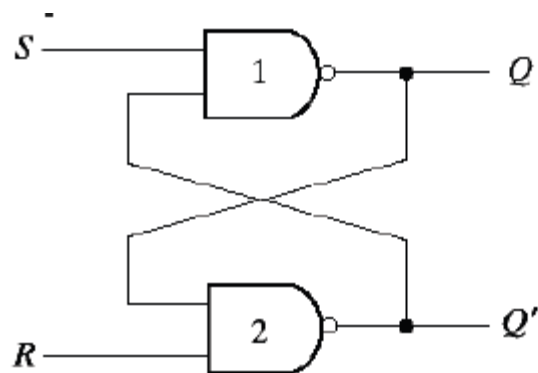
(a) Crossed-coupled circuit

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(After $SR = 10$)
0	1	1	0	
1	1	1	0	(After $SR = 01$)
0	0	1	1	
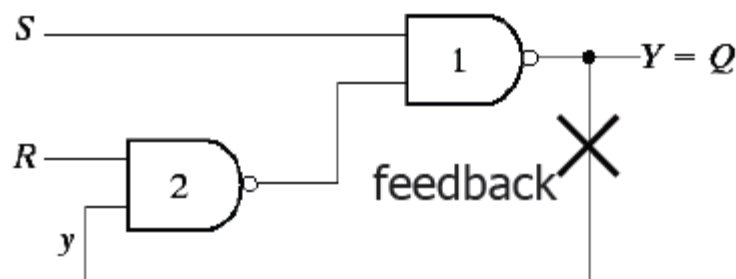
(b) Truth table

(c) Circuit showing feedback

$$SR$$

y	00	01	11	10
0	1	1	0	0
1	1	1	1	0

$Y = S' + Ry$ when $S'R' = 0$

(d) Transition table

S=0, R=0 (S'R' = 1)
should not be used
$\Rightarrow$ S'R' = 0 is
    normal mode

* should be carefully
  checked first 9-20

Analysis Procedure

Procedure to analyze an asynchronous sequential circuits with SR latches:

1. Label each latch output with Y_i and its external feedback path (if any) with y_i
2. Derive the Boolean functions for each S_i and R_i
3. Check whether SR=0 (NOR latch) or S'R'=0 (NAND latch) is satisfied
4. Evaluate Y=S+R'y (NOR latch) or Y=S'+Ry (NAND latch)
5. Construct the transition table for $Y=Y_1Y_2\ldots Y_k$
6. Circle all stable states where Y=y

Analysis Example

$S_1 = x_1 y_2$ $R_1 = x'_1 x'_2 \Rightarrow S_1 R_1 = x_1 y_2 x'_1 x'_2 = 0$ (OK)
$S_2 = x_1 x_2$ $R_2 = x'_2 y_1 \Rightarrow S_2 R_2 = x_1 x_2 x'_2 y_1 = 0$ (OK)

$$Y_1 = S_1 + R'_1 y_1$$
$$= x_1 y_2 + (x_1 + x_2) y_1$$
$$= x_1 y_2 + x_1 y_1 + x_2 y_1$$
$$Y_2 = S_2 + R'_2 y_2$$
$$= x_1 x_2 + (x_2 + y'_1) y_2$$
$$= x_1 x_2 + x_2 y_2 + y'_1 y_2$$
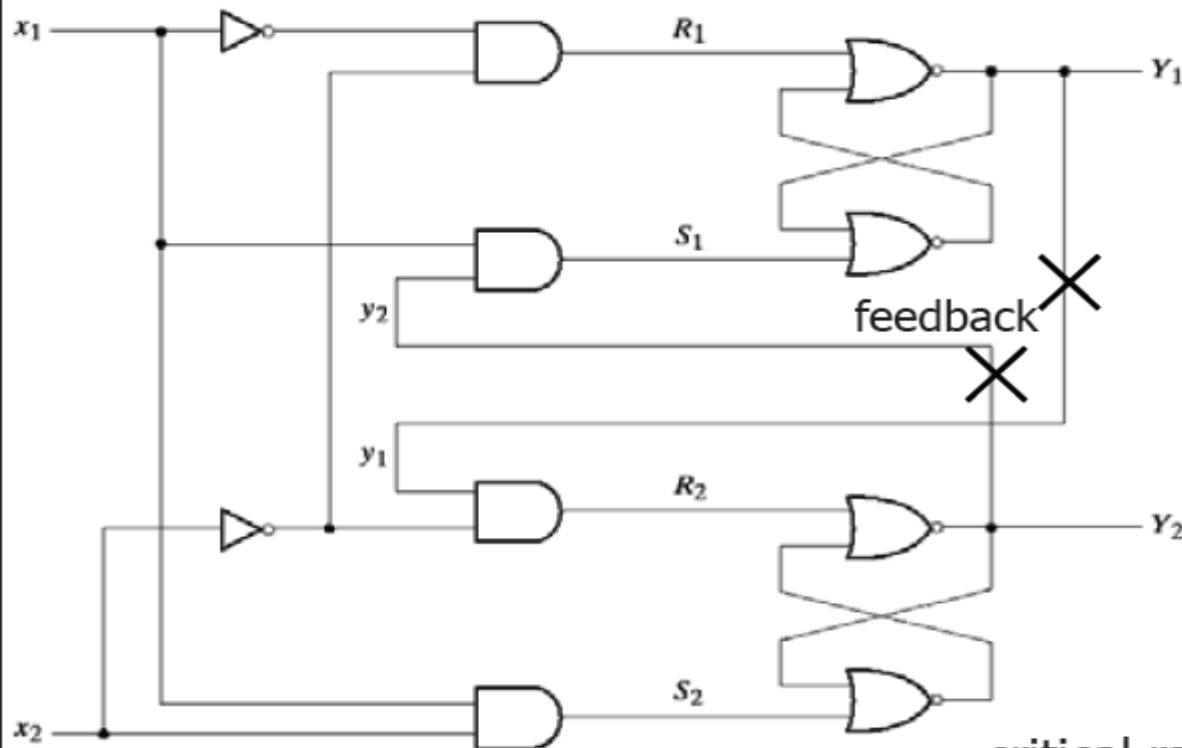
$y_1 y_2$ \ $x_1 x_2$	00	01	11	10
00	00	00	01	00
01	01	01	11	11
11	00	11	11	10
10	00	10	11	10

critical race !!

9-22

Procedure to implement an asynchronous sequential circuits with SR latches:

1. Given a transition table that specifies the excitation function $Y = Y_1Y_2\ldots Y_k$, derive a pair of maps for each S_i and R_i using the latch excitation table

2. Derive the Boolean functions for each S_i and R_i
   (do not to make Si and Ri equal to 1 in the same minterm square)

3. Draw the logic diagram using k latches together with the gates required to generate the S and R
   (for NAND latch, use the complemented values in step 2)

Implementation Example

Excitation table: list the required S and R for each possible transition from y to Y

(a) Transition table
$Y = x_1 x'_2 + x_1 y$

(b) Latch excitation table

(c) Map for $S = x_1 x'_2$

(d) Map for $R = x'_1$

(e) Circuit with NOR latch

(f) Circuit with NAND latch

y = 1 (outside) → 0 (inside)
∴ S=0, R=1 from excitation table

9-24

- ■ Design example: gated latch
  - ■ Accept the value of D when G=1
  - ■ Retain this value after G goes to 0 (D has no effects now)
- ■ Obtain the flow table by listing all possible states
  - ■ Dash marks are given when both inputs change simultaneously
  - ■ Outputs of unstable states are don't care

State	Input		Output	Comments
	D	G	Q	
a	0	1	0	D=Q because G=1
b	1	1	1	D=Q because G=1
c	0	0	0	After states a or d
d	1	0	0	After state c
e	1	0	1	After states b or f
f	0	0	1	After state e

DG

	00	01	11	10
a	c,−	(a),0	b,−	−,−
b	−,−	a,−	(b),1	e,−
c	(c),0	a,−	−,−	d,−
d	c,−	−,−	b,−	(d),0
e	f,−	−,−	b,−	(e),1
f	(f),1	a,−	−,−	e,−

9-28

Two or more rows can be merged into one row if there are **non-conflicting** states and outputs in **every** columns

After merged into one row:

- Don't care entries are overwritten
- Stable states and output values are included
- A common symbol is given to the merged row

Formal reduction procedure is given in next section

DG

	00	01	11	10
a	c ,–	(a), 0	b ,–	– ,–
c	(c), 0	a ,–	– ,–	d ,–
d	c ,–	– ,–	b ,–	(d), 0

DG

	00	01	11	10
b	– ,–	a ,–	(b), 1	e ,–
e	f ,–	– ,–	b ,–	(e), 1
f	(f), 1	a ,–	– ,–	e ,–

(a) States that are candidates for merging

DG

	00	01	11	10
a, c, d	(c), 0	(a), 0	b ,–	(d), 0
b, e, f	(f), 1	a ,–	(b), 1	(e), 1

DG

	00	01	11	10
a	(a), 0	(a), 0	b ,–	(a), 0
b	(b), 1	a ,–	(b), 1	(b), 1

(b) Reduced table (two alternatives)

DG

y	00	01	11	10
0	0	0	1	0
1	1	0	1	1

(a) $Y = DG + G'y$

DG

y	00	01	11	10
0	0	0	1	0
1	1	0	1	1

(b) $Q = Y$

- Assign a binary value to each state to generate the transition table
  - a=0, b=1 in this example
- Directly use the simplified Boolean function for the excitation variable Y
  - An asynchronous circuit without latch is produced
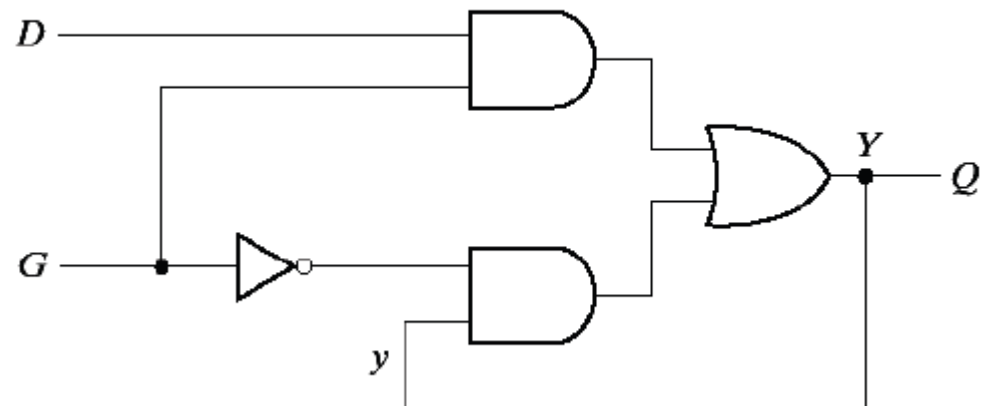
(a) $S = DG$

$R = D'G$

(a) Maps for S and R

Listed according to the transition table and the excitation table of SR latch
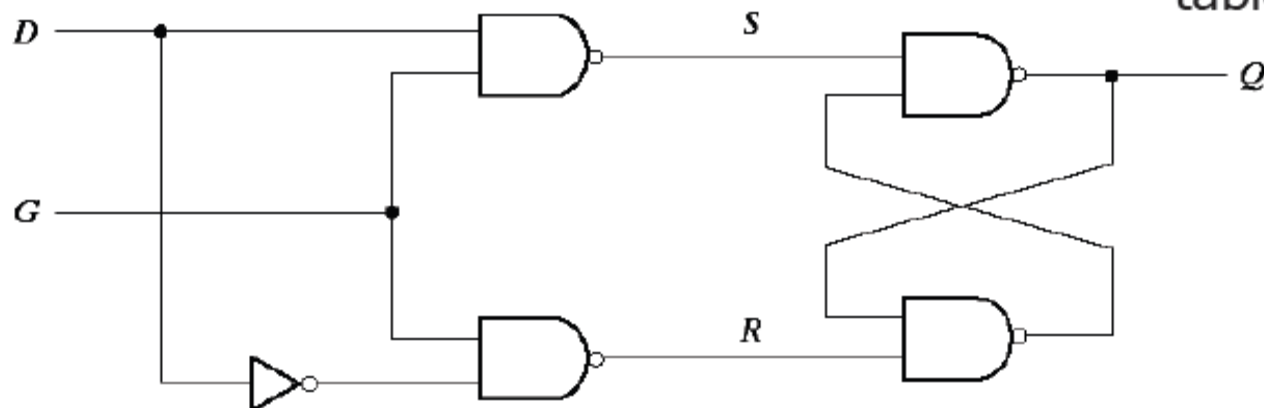
(b) Logic diagram

Two states are equivalent if they have the **same output** and go to the **same** (equivalent) **next states** for each possible input

- Ex: (a,b) are equivalent
    (c,d) are equivalent

State reduction procedure is similar in both sync. & async. sequential circuits

Present State	Next State x=0	Next State x=1	Output x=0	Output x=1
a	c	b	0	1
b	d	a	0	1
c	a	d	1	0
d	b	d	1	0

- For completely specified state tables:
    → use implication table
- For incompletely specified state tables:
    → use compatible pairs

- Step 1: build the implication chart

Present State	Next State x=0	x=1	Output x=0	x=1
a	d	b	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

$a \equiv b$ iff $d \equiv e$

$b \neq c$ since outputs are not equivalent

d and e are the same

- Step 2: delete the node with unsatisfied conditions
- Step 3: repeat Step 2 until equivalent states found

a≠f because c≠d

b≠f because c≠e
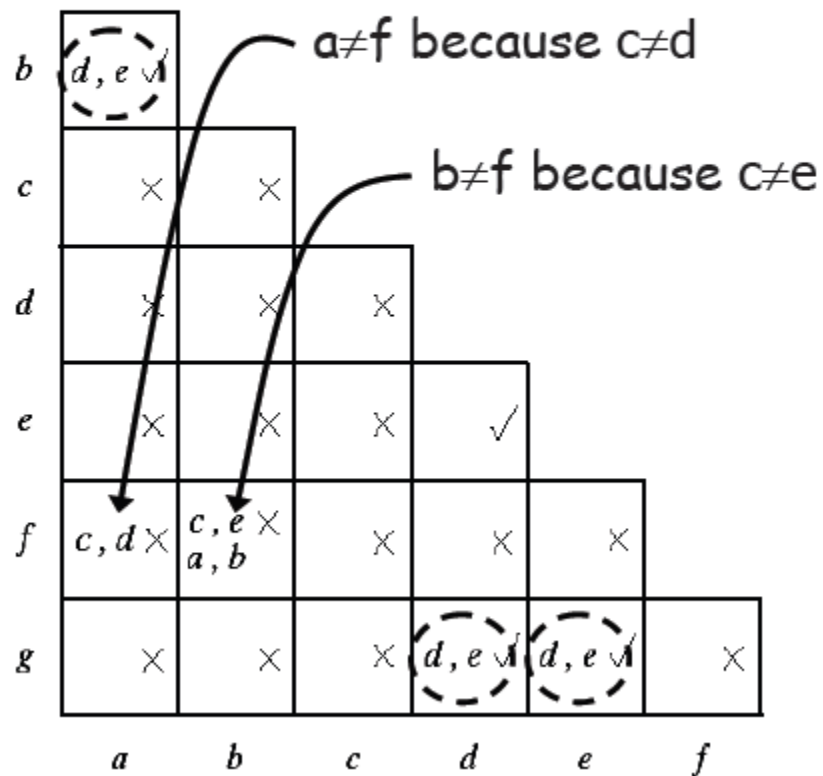
equivalent states :
(a,b) (d,e) (d,g) (e,g)

d == e == g

Present State	Next State x=0	x=1	Output x=0	x=1
a	d	a	0	0
c	d	f	0	1
d	a	d	1	0
f	c	a	0	0

Reduced State Table 9

Objective: choose a proper binary state assignment to **prevent critical races**

Only one variable can change at any given time when a state transition occurs

States between which transitions occur will be given **adjacent** assignments

- Two binary values are said to be adjacent if they differ in only one variable

To ensure that a transition table has no critical races, every possible state transition should be checked

- A tedious work when the flow table is large
- Only 3-row and 4-row examples are demonstrated

Three states require two binary variables

Outputs are omitted for simplicity

Adjacent info. are represented by a transition diagram

a and c are still not adjacent in such an assignment !!

- Impossible to make all states adjacent if only 3 states are used

(a) Flow table

(b) Transition diagram

9-4

- A race-free assignment can be obtained if we add an extra row to the flow table
  - Only provide a race-free transition between the stable states
- The transition from a to c must now go through d
  - 00 → 10 → 11 (no race condition)
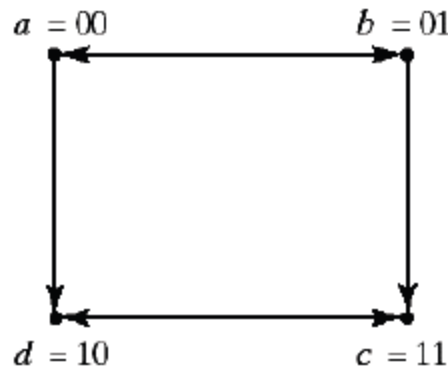
don't care but cannot be 10
(cannot stable)

9-45

Unwanted switching appears at the output of a circuit

- Due to different propagation delay in different paths

May cause the circuit to mal-function

- Cause temporary false-output values in combinational circuits
- Cause a transition to a wrong state in asynchronous circuits
- Not a concern to synchronous sequential circuits

Three types of hazards:

(a) Static 1-hazard   (b) Static 0-hazard   (c) Dynamic hazard

- Static hazard: a momentary output change when no output change should occur
- If implemented in sum of products:
  - no static 1-hazard → no static 0-hazard or dynamic hazard
- Two examples for static 1-hazard:
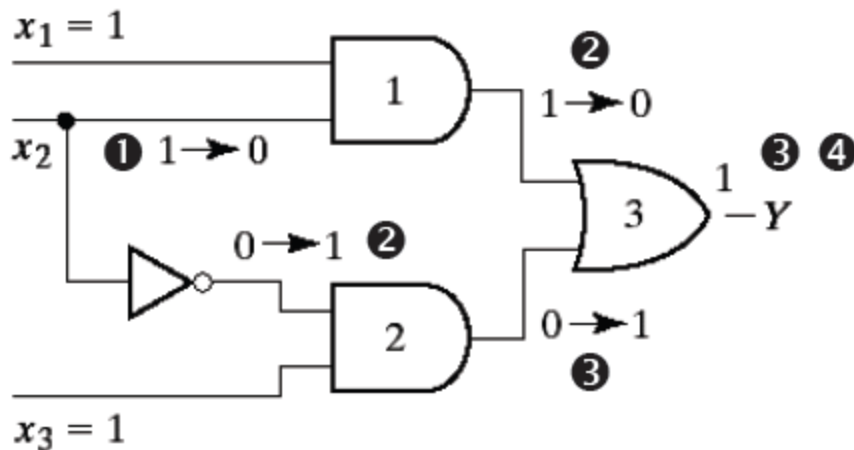
(a) AND-OR circuit
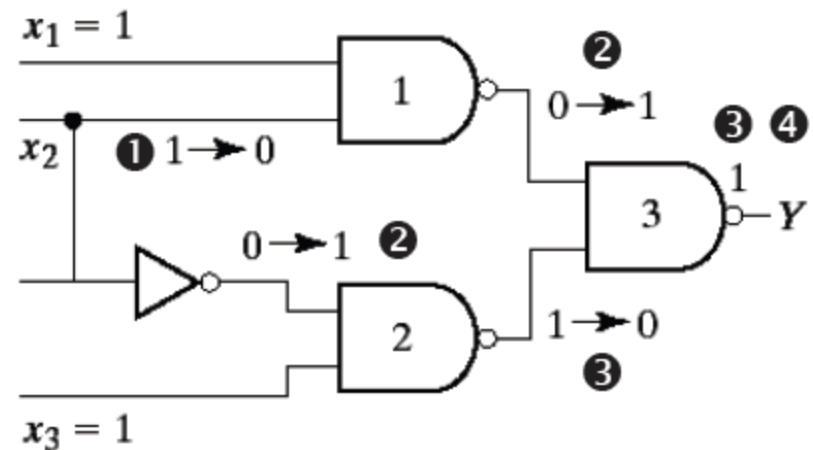
(b) NAND circuit

Hazard can be detected by inspecting the map

The change of input results in a change of covered product term

→ Hazard exists

- Ex: 111 → 101 in (a)

To eliminate the hazard, enclose the two minterms in another product term

- Results in redundant gates
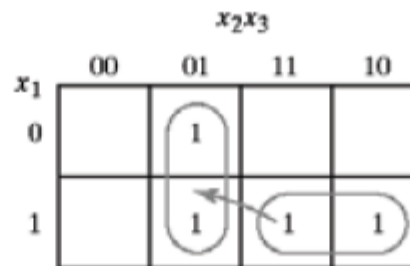
(a) $Y = x_1 x_2 + x'_2 x_3$
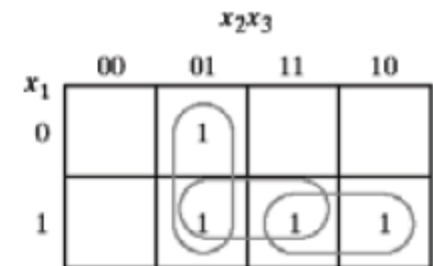
(b) $Y = x_1 x_2 + x'_2 x_3 + x_1 x_3$

Redundant !!
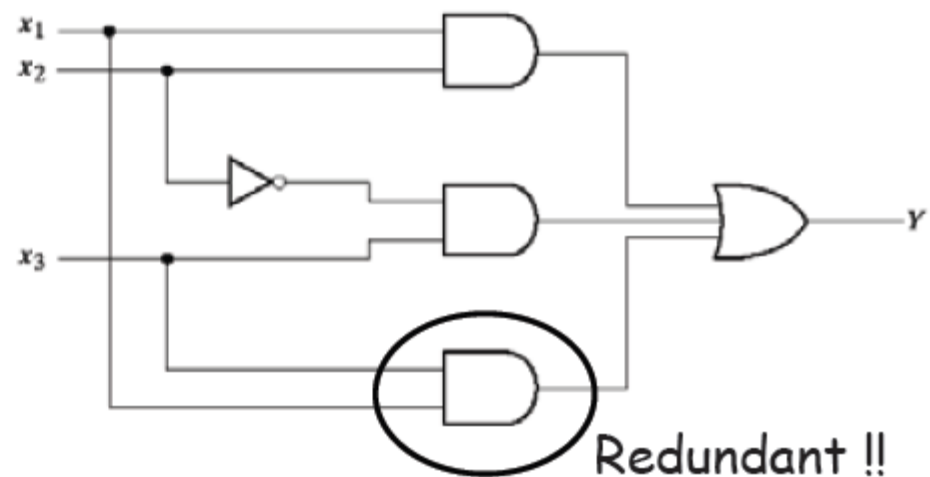
- Implement the asynchronous circuit with SR latches can also remove static hazards

  - A momentary 0 has no effects to the S and R inputs of a NOR latch
  - A momentary 1 has no effects to the S and R inputs of a NAND latch

Replaced by a latch

$Y = x_1 x_2 + x'_2 y$

Hazards exist !!

(a) Logic diagram
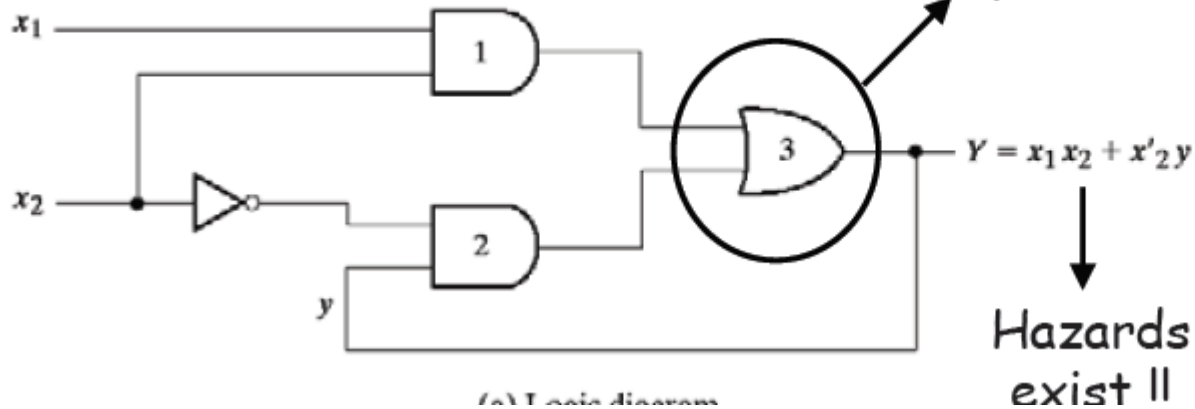
$x_1 x_2$

y	00	01	11	10
0	0	0	1	0
1	1	0	1	1

(b) Transition table

$x_1 x_2$

y	00	01	11	10
0			1	
1	1		1	1

(c) Map for Y

- Besides static and dynamic hazards, another type of hazard in asynchronous circuits is called *essential hazard*

- Caused by unequal delays along two or more paths that originate from the *same input*

- Cannot be corrected by adding redundant gates

- Can only be corrected by adjusting the amount of delay in the affected path

  - Each feedback path should be examined carefully !!

- No diagonal lines in the transition diagram
  → No need to add extra states
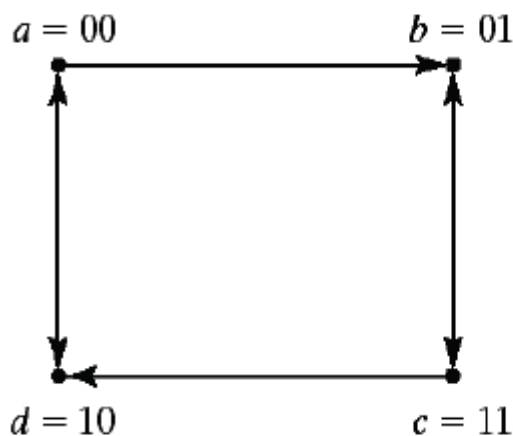
Fig. 9-43 Transition Diagram

(a) Transition table

(b) Output map $Q = y_2$

(a) $S_1 = y_2 TC + y'_2 T'C'$

(b) $R_1 = y_2 T'C' + y'_2 TC$

(c) $S_2 = y'_1 TC'$

(d) $R_2 = y_1 TC'$

Which one is the suitable to detecting the hazard in circuit?

- Karnaugh map
- Boolean expression
- Logic gates
- None of these

Which one is not the type of hazard

- Static-0 Hazard
- Static-1 Hazard
- Dynamic Hazard
- None of the above

In a logic circuit an Hazard is independent from

- Delay Existing

- Clock Pulses

- Latches

- Feedback

The dynamic hazard problem occurs in

- Combinational circuit alone

- Sequential circuit only

- Both (1) and (2)

- None of these

Weekly Assignment

- Implement asynchronous sequential circuits using latches.

- Why hazards occur in a circuit?

- Define primitive flow table with example

- Define race condition in an asynchronous sequential circuit

- Explain briefly the state-transition diagram, race-free state assignment.

- Explain the reduction techniques of hazards in circuits.

- https://www.youtube.com/watch?v=jm0PGDSSBkI

- https://www.youtube.com/watch?v=tUOGg2YVP8I

- https://www.youtube.com/watch?v=DwK8mEjHnx0

1. What is an asynchronous sequential circuit?

- **An asynchronous sequential circuit is not driven by a periodic clock signal to synchronize its internal states.**

- An asynchronous sequential circuit is driven by a periodic, fixed clock signal.

- An asynchronous sequential circuit is slower than a synchronous sequential circuit.

- An asynchronous sequential circuit does not synchronize its internal states.

2. What is a flip-flop?

- **A flip-flop is a memory device controlled by a clock.**

- A flip-flop is a clock device.

- A flip-flop is an analogous circuit.

- A flip-flop is a digital clock.

3. The effect of change in input more than one state is called**a.**

- undefined condition**.**

- **race condition**

- reset condition

- ideal condition

4. The change in state occurs during**-**

- **pulse transition**

- outputs

- clock pulses

- inputs

5. Asynchronous sequential logic circuit not uses

- input.

- outputs

- **clock pulses**

- time

6. Naming the states is done in

- transition table

- stable state

- **flow table**

- excitation table

7. The delay elements provide

- large memory

- outputs

- clock pulses

- **short term memory**

8. The analysis of Asynchronous sequential circuits are used to obtain

- **table**

- a diagram

- graph

- both a and b

9. Race condition is present in

- synchronous logic circuit

- asynchronous logic circuit

- ideal logic circuit

- both a and b

10. During the design of asynchronous sequential circuits it is more convenient to name the state by letters this type of table called

- **Square table**

- Latch table

- Flow table

- None

- Choose the correct one from the given answers for the following questions:
  = (**faster, triggered ,two ,feed back**)

- In sequential circuits, the output signals are **……** to the input side

- Combinational circuits are often…….than sequential circuits.

- There are **…..** type of sequential circuits.

- Synchronous Sequential Circuits are **……** in the presence of a clock signal

Choose the correct one from the given answers for the following questions: =
(**absence, change the state ,latch, two**)

- Asynchronous Sequential Circuits function in the **-------** of a clock signal.

- The sequential circuit is also called a ----- because both are a memory cell, which are capable of storing one bit of information.

- The basic latch consists of **----** inverters

- The output of latches will remain in set/reset untill the trigger pulse is given to **------**

    :

Choose the correct one from the given answers for the following questions: = (**primitive flow table, SR latch , asynchronous circuits,state reduction**)

- The reduction of flip-flops in a sequential circuits are referred as **------**

- The first step of analysis procedure of --------is to label outputs

- Table having one state in each row is called **primitive flow table**

- One of the properties of ----------------is feedback loop

- Choose the correct one from the given answers for the following questions: = (**Synchronous counter , The output decreases by 1,4 , clocked flip-flops**)

- Memory elements in synchronous circuits are **clocked flip-flops** .

- Internal propagation delay of asynchronous counter is removed by----

- What happens to the parallel output word in an asynchronous binary downcounter whenever a clock pulse occurs-------

- How many flip-flops are required to construct a decade counter-----

Choose the correct one from the given answers for the following questions:
=(**Clock signal ,Two, Self-timed ,It filters the reset signal**)

- How many types of resets are there in hardware design----

- In synchronous reset, reset is sampled with respect to ------

- Which of the following is an advantage of a synchronous reset---

- Asynchronous circuit is also called-------circuit.

(SEM-III) THEORY EXAMINATION 2019-20
DIGITAL SYSTEM DESIGN

Time: 3 Hours   Total Marks: 100

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief.   2 x 10 = 20

Qno.	Question	Marks	CO
a.	The solution to the quadratic equation $k^2-11k + 22 = 0$ are x = 3 and x = 6. What is the base of the number system?	2	1
b.	Simplify the expression F (A, B, C, D) = ACD+$\bar{A}$ B + $\bar{D}$ by K- Map.	2	1
c.	Construct half subtractor using logic gates.	2	2
d.	Implement a 4:1 multiplexer using 2:1 multiplexer.	2	2
e.	What do you mean by race around condition in JK Flip Flop?	2	3
f.	Distinguish between Leach and Flip Flop.	2	3
g.	What is logic family? Give the classification of logic families in brief.	2	4
h.	Describe figure of merit & noise immunity of TTL & CMOS ICs.	2	4
i.	What are the advantages and disadvantages of flash type ADC?	2	5
j.	The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0Volts, what is the output for an input of 101101111?	2	5

SECTION B

2. Attempt any *three* of the following: 3 x 10 = 30

Qno.	Question	Marks	CO
a.	Design an excess-3 to BCD code converter.	10	1
b.	Implement a full adder by using 8:1 multiplexer.	10	2
c.	Design a sequential circuit with two Flip Flops, A & B and one input x. When x=0, the State of the circuit remains the same when x=1 the circuit passes through the state transitions from 00 to 01 to 11 to 10 back to 00 & repeat.	10	3
d.	Compare TTL and CMOS logic families and also draw CMOS NOR gate.	10	4
e.	Explain the operation of successive approximation ADC. Discuss it merits and demerits.	10	5

SECTION C

3. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Minimize the logic function using Quine-McCluskey Method $F(A, B,C,D,E) = \sum m(8,9,10,11,13,15,16,18,21,24,25,26,27,30,31)$	10	1
b.	Simplify the logic expression using K-Map $F(A,B,C,D,E,F) = \sum m(0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61)$	10	1

Printed Page 2 of 2   Sub Code:KEC302

Paper Id: | 130322 | Roll No: [ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ] •

4. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Design a 4-bit parallel binary Adder/Subtractor circuit.	10	2
b.	Design a 4-bit comparator circuit using logic gates.	10	2

5. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Discuss Mealy and Moore FSM. What do you mean by excitation table?	10	3
b.	For the given state diagram design the circuit using T flip flop	10	3

6. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Draw three input standard TTL NAND gate circuit and explain its operation.	10	4
b.	Implement the following function using PLA $F_1 = \sum m(0,3,4,7)$ $F_2 = \sum m(1,2,5,7)$	10	4

7. Attempt any *one* part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	With a neat diagram explain the operation of R-2R DAC.	10	5
b.	With a neat sketch explain the operation of Flash ADC.	10	5

Sessional Paper-1

Subject Code: MACSE0304

Roll No: ☐☐☐☐☐☐☐☐☐☐☐☐☐

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY ,GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.tech. (Int.) CSE

(SEM:III, SESSIONAL EXAMINATION –I)(2021-2022)

Subject Name: Digital Logic & Circuit Design

Time: 1.15Hours   Max. Marks:30

General Instructions:

➤ All questions are compulsory. Answers should be brief and to the point.
➤ This Question paper consists of 2 pages &5questions.
➤ It comprises of three Sections, A, B, and C. You are to attempt all the sections.
➤ **Section A** -Question No- 1 is objective type questions carrying 1 mark each, Question No- 2 is very short answer type carrying 2 mark each. You are expected to answer them as directed.
➤ **Section B** - Question No-3 is Short answer type questions carrying 5 marks each. You need to attempt any two out of three questions given.
➤ **Section C** -Question No. 4 &5are Long answer type (within unit choice) questions carrying 6marks each. You need to attempt any one part _a or b._
➤ Students are instructed to cross the blank sheets before handing over the answer sheet to the invigilator.
➤ No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

		SECTION – A	**[8]**	**CO**	**Blooms Level**
1.	**Attempt all parts**		(4×1=4)	CO	K
	a.	The XOR gates output will be low if two inputs are _____ a) 00 b) 01 c) 10 d) None of these	(1)	CO1	K2
	b.	A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate? a) OR b) AND c) XOR d) NAND	(1)	CO1	K1
	c.	2's Complement of a binary number $(10101110)_2$ a) 01010001 b) 11010001 c) 01010010 d) 11010111	(1)	CO1	K2
	d.	DeMorgan's theorem states that _____ a) (A.B)' = A' + B' b) (A + B)' = A'. B c) A' + B' = A'.B' d) (A.B)' = A' + B	(1)	CO1	K1

Printed page: ….   **Subject Code: MACSE0304**

Roll No: ☐☐☐☐☐☐☐☐☐☐☐☐☐

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		SECTION – A	[8]	CO	Blooms Level
1.	Attempt all parts		(4×1=4)	CO	K
	a.	A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate? a) OR b) AND c) XOR d) NAND	(1)	CO1	K1
	b.	The NOR gate output will be high if the two inputs are _____ a) 00 b) 01 c) 10 d) 11	(1)	CO1	K1
	c.	Excess-3 code of 739 is: a) 1010 0110 1100 b) 1101 1001 1000 c) 1101 0110 1100 d) 1010 1001 1000	(1)	CO1	K2
	d.	Binary equivalent of gray code 101011 is: a) 110010 b) 101010	(1)	CO1	K2

Old Question Papers

Printed Page 2 of 2   Sub Code: KEC302

Paper Id: 130322   Roll No: [ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ]

4. Attempt any one part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Design a 4-bit parallel binary Adder/Subtractor circuit.	10	2
b.	Design a 4-bit comparator circuit using logic gates.	10	2

5. Attempt any one part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Discuss Mealy and Moore FSM. What do you mean by excitation table?	10	3
b.	For the given state diagram design the circuit using T flip flop	10	3

6. Attempt any one part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	Draw three input standard TTL NAND gate circuit and explain its operation.	10	4
b.	Implement the following function using PLA $F_1 = \sum m(0,3,4,7)$ $F_2 = \sum m(1,2,5,7)$	10	4

7. Attempt any one part of the following: 1 x 10 = 10

Qno.	Question	Marks	CO
a.	With a neat diagram explain the operation of R-2R DAC.	10	5
b.	With a neat sketch explain the operation of Flash ADC.	10	5

- What are synchronous and asynchronous sequential circuit? Write the procedure for the analysis of a sequential circuit.

- Draw the state diagram for a sequence generator which produce an output '1' every time the sequence 0101 is detected and output '0' at all other times. Design the circuit also.

- Implement asynchronous sequential circuits using latches.

- Design a sequence detector circuit to detect a serial input sequence of 1010. It should produce an output 1 when the input pattern has been detected.

- What are the advantages and disadvantages of Synchronous Counters Over Asynchronous Counters?

- Compare Asynchronous and Synchronous Sequential Circuits

- Explain the steps involved in the design of sequential logic circuits.

- Explain the rules for state assignment of synchronous sequential circuit.

- Explain the clock generation circuit.

- What are the advantages and disadvantages of Synchronous Counters Over Asynchronous Counters?

- Compare Asynchronous and Synchronous Sequential Circuits

- Explain the steps involved in the design of sequential logic circuits.

- Explain the rules for state assignment of synchronous sequential circuit.

- Explain the clock generation circuit.

Youtube/other Video Links:

- https://www.youtube.com/watch?v=VBM5XTvJSRQ&ab_channel=JAESCompanyJAESCompany

- https://www.youtube.com/watch?v=1A_NcXxdoCc&ab_channel=NesoAcademyNesoAcademyVerified

References

1. R.P. Jain, "Modern Digital Electronics," Tata McGraw Hill, 4th edition, 2009.
2. A. Anand Kumar, "Fundamental of Digital Circuits," PHI 4th edition, 2018.
3. W.H. Gothmann, "Digital Electronics- An Introduction to Theory and Practice," PHI, 2nd edition, 2006.

Thank You