NAME _____
First Last

Student ID# _____

STONY BROOK UNIVERSITY

COMPUTER SCIENCE DEPARTMENT

MIDTERM #1 EXAMINATION
VERSION A

CSE 320
Spring 2014
March 26, 2014

This is a closed-book exam. (80 minutes)
Use this form for your work and return it.

The exam has 9 problems.
It is crucial to show all work done on the provided paper.

#1 _____	(10 pts)	#6 _____	(10 pts)
#2 _____	(14 pts)	#7 _____	(12 pts)
#3 _____	(10 pts)	#8 _____	(12 pts)
#4 _____	(7 pts)	#9 _____	(15 pts)
#5 _____	(10 pts)		

TOTAL _____ (100 Max)

1 [1 pt each] Multiple Choice. Write in the correct answer.

_____ A 2-level Multiplexor gate representation is equivalent to which of the following (select all that apply)
(a) 2-level AND-OR (b) 2-level OR-AND (c) Sum-Of-Products
(d) Product-Of-Sums (e) Minterm Expression (f) Maxterm Expression

_____ An ISA does not specify which of the following?
(a) number formats (b) register assignment (c) memory size (d) addressing modes (e) instruction set

_____ A multiplexer with 4 selector bits has how many input values?
(a) 2 (b) 5 (c) 8 (d) 16 (e) 32

_____ A MIPS register file is capable of reading ___ register(s) at a time.
(a) 0 (b) 1 (c) 2 (d) 3 (e) 4

_____ What type of combinatorial circuit maps 2^n inputs to a binary value of size n?
(a) Encoder (b) Decoder (c) Half Adder (d) XOR gate (e) Multiplexor

_____ A flip-flop
(a) always stores 0 (b) save data on every clock cycle (c) stores a 1-bit value (d) stores the opposite of the input value

_____ Which of the following is NOT a Universal Set (select all that apply)
(a) {AND, OR, NOT} (b) {AND, OR} (c) {NAND} (d) {NOR} (e) {XOR}

_____ At the start of the decode stage, the PC contains
(a) the current instruction to execute (b) the memory address of the data
(c) the memory address of the current instruction (d) the memory address of the next instruction

_____ The SLT instruction is which instruction format?
indent (a) register (b) immediate (c) jump (d) branch

2 [14pts] Short Answer

(a) [4 pts] Draw and label all parts of MIPS R-type Instruction format, including size of the fields.

(e) [4 pts] What is the critical path of a circuit? Why is it important?

3 [10 pts] Short Answer

(a) [2 pts] Consider a new gate # described by the following table. Write the minimal boolean expression for this gate.

x	y	x#y
0	0	1
0	1	1
1	0	0
1	1	1

(b) [8 pts] Use this gate to build other gates in order to show it is a universal gate. If needed use constant 0 or constant 1.

4 [7 pts] Boolean Expressions.

$$f = ((A' + B)' + C')' + DC' + AB'$$

(a) [1 pts] How many literal appear in the boolean expression? _____

(b) [4 pts] Find all minterms, answer in boolean expression form:

(c) [2 pts] Name the maxterms, answer in $\prod M(?)$ form :

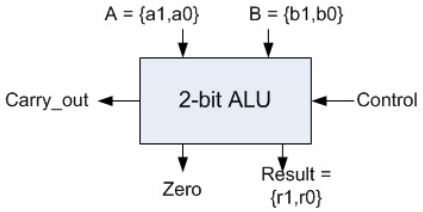
5 [10 pts] Using the postulates of Boolean algebra, prove the following formulas:

$$x'yz + x'yz' + xyz + zyz' = x'y + yz$$

6 [10 pts] Given seven input signals (a,b,c,d,e,f, and g) implement the following functionality using one 2-bit (4-output) decoder, and OR and AND gates.

If a and e are both 1, and at least 2 of inputs b,c and f are 1, the output is 1.
If d is 0 and e is 1, the output is 1.
If g is 1, the output is 1.
In all other cases, the output is 0.

7 [12 pts] Using 2-bit (1-selector) multiplexors and 1-bit Adders, build a 2-bit ALU as described by the figure (with Carry_{out} and zero output signals) which performs the following functions. Numbers are in two's complement form. Note: There is no Carry_{in} signal.



Control	Operation
00	-B
01	A - B
10	B - A
11	-A

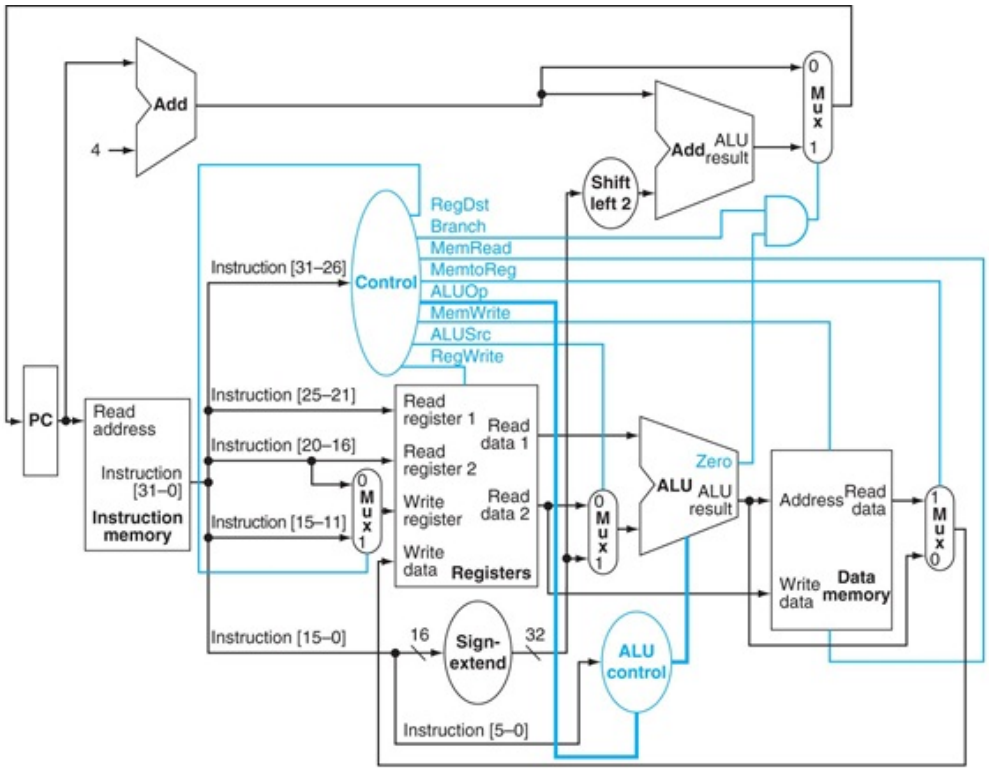
8 [12 pts] Single-cycle Datapath

Implement a "branch on odd" instruction into the single-cycle MIPS datapath.

```
BODD Rs, label

#if Reg[Rs] is odd
#    PC <= PC + 4 + (sign-extend(IR[15:0]) << 2);
```

Modify the datapath and the control table to implement the BODD instruction. Use the minimal amount of additional hardware and fill/modify/expand the control table. **Mark the full datapath for the new instruction.**



Type	RegDst	ALUSrc	MemtoReg	RegWrite	MemRead	MemWrite	Branch	ALUOp1	ALUp0	Jump
R	1	0	0	1	0	0	0	1	0	0
lw	0	1	1	1	1	0	0	0	0	0
sw	X	1	X	0	0	1	0	0	0	0
beq	X	0	X	0	0	0	1	0	1	0
j	X	X	X	0	X	0	X	X	X	1

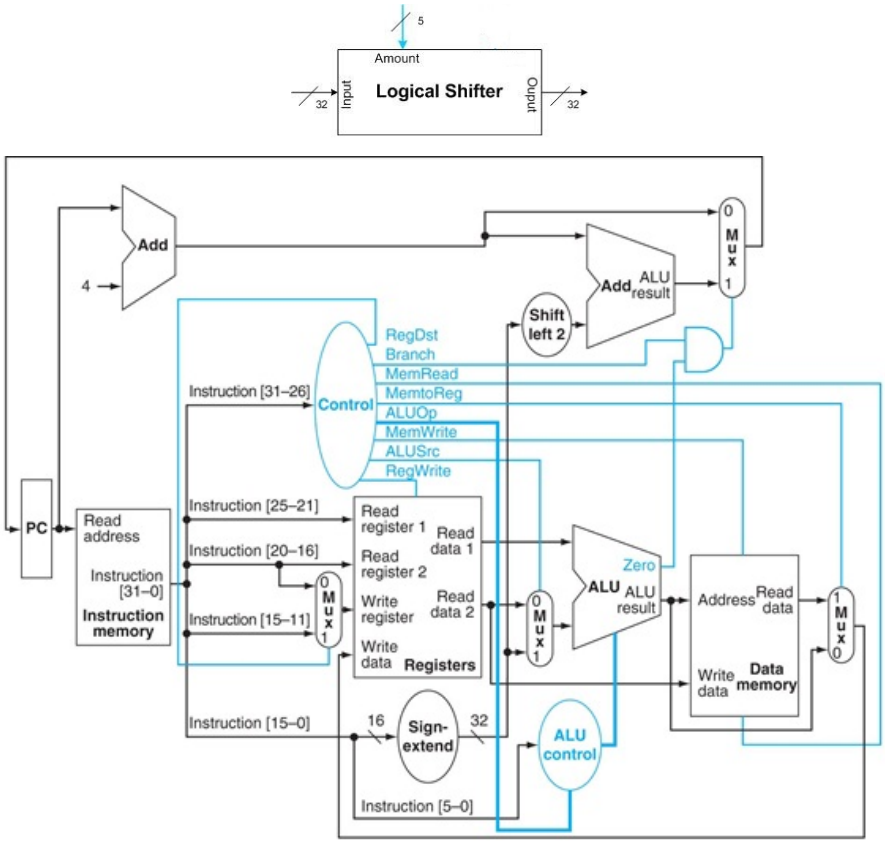
9 [15 pts] Single-cycle Datapath

Modify the datapath and the control table to implement logical shifting instruction 'srl'.A shifter may be added to the datapath as specified below.

```
Reg[rd] <- Reg[rt] >> shamt;
# register rt is shifted to the right by the shamt. The upper bits are loaded with 0.
```

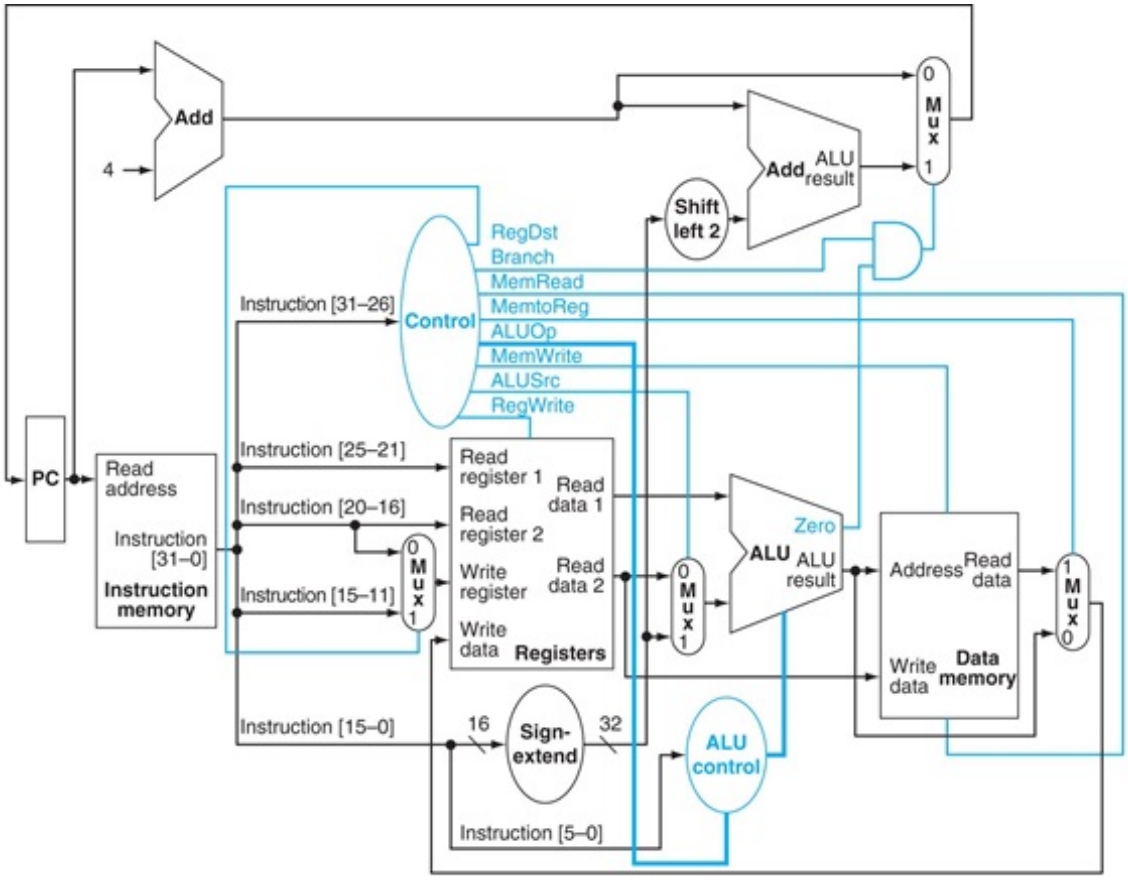
The shifter amount control specifies the number of bits to shift. The value to be shifted is placed on the input and after a delay the shifted value is available on the output.

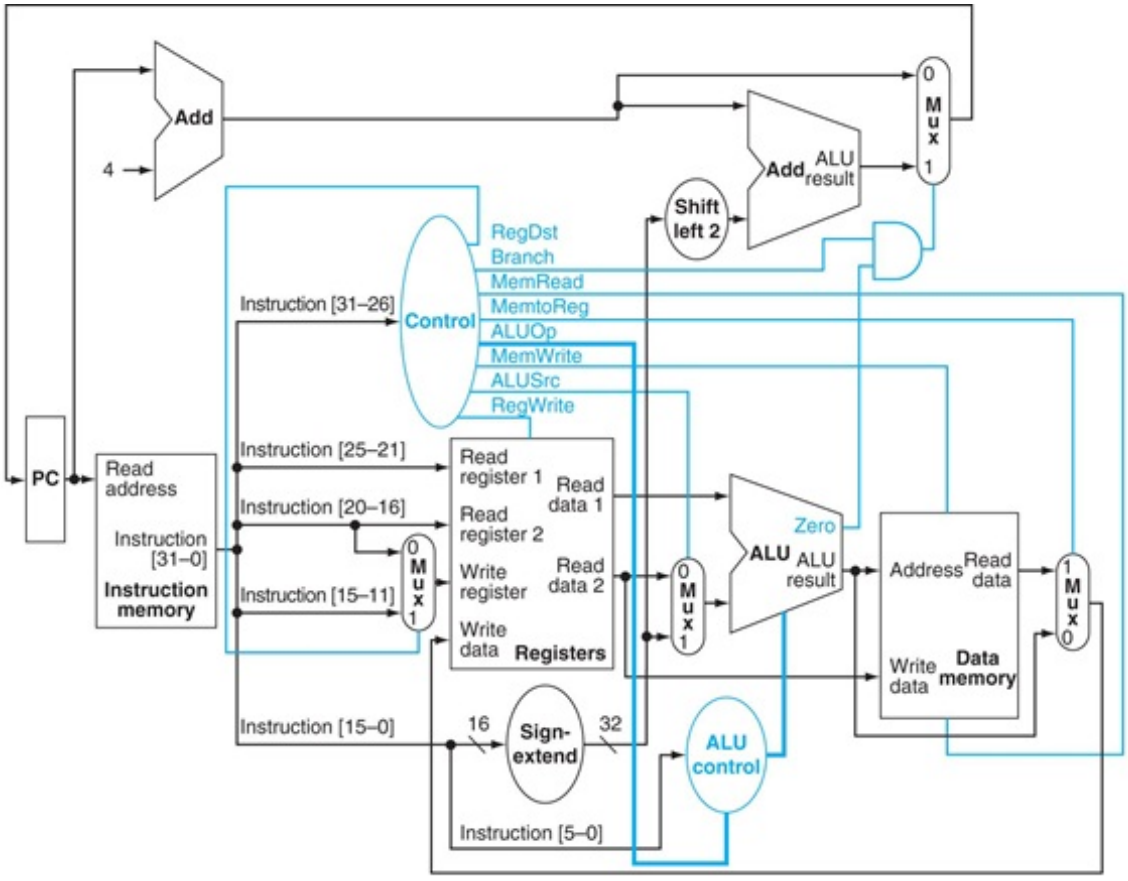
Modify the datapath and the control table to implement the 'srl'instruction. Use the minimal amount of additional hardware and fill/modify/expand the control table. **Mark the full datapath for the new instruction.**



Type	RegDst	ALUSrc	MemtoReg	RegWrite	MemRead	MemWrite	Branch	ALUOp1	ALUp0	Jump
R	1	0	0	1	0	0	0	1	0	0
lw	0	1	1	1	1	0	0	0	0	0
sw	X	1	X	0	0	1	0	0	0	0
beq	X	0	X	0	0	0	1	0	1	0
j	X	X	X	0	X	0	X	X	X	1

Extra space provided.


Add
4
0
M
u
x
1
Add
ALU result
Shift left 2
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
ALU control
Zero
ALU
ALU result
Address
Read data
Write data
Data memory


Add
4
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ALU
ALU result
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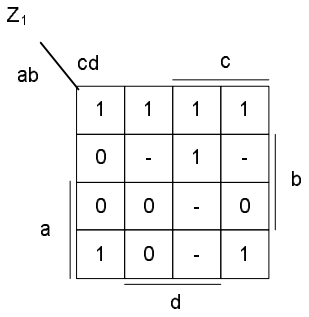
Write data
Data memory

Karnough Maps

(a) Write the simplified SOP expression for the Boolean function defined by the following Karnough map. Draw the corresponding 2-level NAND-NAND network.

(b) Write the simplified POS expression for the Boolean function defined by the following Karnough map. Draw the corresponding 2-level NOR-NOR network.

(c) Draw the corresponding network with 2-bit multiplexors.



[25 pts] Pick one of the following, and answer (a)-(c):
• The binary digit vector x_2, x_1, x_0 represents integer x in the range $0 \leq x \leq 7$. Design a digital system using only NOR gates that implements the following function $Z = min(u, w)$ where $u = |x^2 + 2x - 4|$ and $w = |x^2 - 3|$.

• Design a system which takes two inputs, a 3-bit binary number X and a control bit C. If the control input is 1, the system should output Z = X * 2_{10}. If the control input is 0, the system should output Z = X^2.

(a) [10 pts] Create the Truth Table. How many bits are needed to represent Z?

(b) [10 pts] Find the minimal boolean expressions using Karnough maps for the most significant bit (MSB) and least significant bit (LSB) of Z.

(c) [5 pts] Create the minimal two level NOR-NOR implementation for the outputs in (b).

[25 pts] Design a controller to display an electronic die as shown below. Inputs to the controller represent a 3-bit number, which indicates what is to be displayed. There are nine outputs, A - I, one for each of the dots. A dot will light when given a 1, and is unlit when given a 0.

(a) [5 pts] Create the truth table.

(b) [10 pts] Implement using the minimal number of AND, OR, and NOT gates. *Assume only uncomplemented variables are given.*

(c) [10 pts] A simplified circuit can be designed using a 4-selector demultiplexor and OR gates. Design the circuit.