CSE320 Fall 2014

Homework#8
Quiz in Lecture Tues. Dec. 2, 2014
There are no make-up quizzes!

Problem 1: Consider a direct-mapped cache with 2^{16} words in main memory. The cache has 16 blocks of 8 words each. It is a **word-addressable computer**.

(a) How many blocks of main memory are there?

(b) What is the format of a memory address as seen by the cache, that is, what are the sizes of the tag, cache block, and block offset fields (if they apply)?

(c) To which cache block will the memory reference $DB63_{16}$ map?

Problem 2: Consider a **byte-addressable** computer with 16MB of main memory, a cache capable of storing a total of 64KB of data and block size of 32 bytes.

(a) How many bits in the memory address?

(b) How many blocks are in the cache?

(c) Assume the cache is direct mapped. What is the format of the memory address, including names and sizes?

(d) Assume the cache is 4-way set associative. What is the format of the memory address, including names and sizes?

(e) Assume the cache is fully associative. What is the format of the memory address, including names and sizes?

Problem 3: Consider a **byte-addressable** computer, ie. You access things in bytes instead of words, with 16-bit addresses, a cache capable of storing a total of 2KB of data, and blocks of 8 bytes. What is the format of the memory address, including names and sizes, for (a) direct mapped, (b) fully associative, (c) 4-way set associative cache? Where in the cache would the memory address BAD016 be mapped for each of the three mappings (answer in binary or decimal)?

Problem 4: Suppose we have a **byte addressable** computer that has a 32-byte cache with 8 bytes per block. The memory address is 8 bits long. The system accesses memory addresses (in hex) in this exact order: 6E, B9, 17, E0, 4E, 4F, 50, 91, A8, AB, AD, 93, and 94.

(a) Assuming the cache is direct mapped, what memory addresses will be in cache block 2 after the last address has been accessed?

(b) Assuming the cache is direct mapped, what is the hit ratio for the entire memory reference sequence given, assuming the cache is initially empty?

(c) Assuming the cache is 2-way set associative with a LRU replacement policy, what is the hit ratio?

Problem 5: The computer spends 82% of the time computing and 18% waiting for the disk. The instruction mix and the average cycles per instruction (CPI) for each type is:

(a) What is the speedup of the machine if the processor is replaced with a new one that reduces the total computation time by 35%.

Type	Percentage	CPI
Integer	40%	1
Floating Point	30%	5
All Others	30%	2

(b) What is the speedup of the machine if the disk is replaced with a solid state device that reduces the disk waiting time by 85%.

(c) What is the speedup of the machine if the CPI of floating point operations was reduced to 1?

(d) Would an infinitely fast disk drive outperform the the speedup in parts (i-iii)?

Problem 6: Calculate the performance of a processor taking into account stalls due to data cache and instruction cache misses.

- The data cache has a 92% hit rate with a 2 cycle hit latency and 124 cycle miss penalty (cache miss and memory latency together).
- The instruction cache has a 90% hit rate with a a 2 cycle hit latency and 50 cycle miss penalty.
- The base CPI of the processor is 1.0
- 30% of instructions are loads and stores.

Assume the load never stalls a dependent instruction and assume the processor must wait for stores to finish when they miss the cache. Finally, assume that instruction cache misses and data cache misses never occur at the same time. Show your work.

(a) Calculate the additional CPI due to the instruction cache stalls.

(b) Calculate the additional CPI due to the data cache stalls.

(c) Calculate the overall CPI for the machine.

Problem 7: Suppose a computer using set associative cache has 2^{21} words of main memory and a cache of 64 blocks, where each cache block contains 4 words. If the cache is 4-way set associative, what is the format of a memory address as seen by the cache?

Problem 8: Consider two processors with different cache configurations:

- Cache 1: Direct Mapped with one-word blocks. Instruction miss rate is 4%, data miss rate 6%
- Cache 2: Two-way set associative with four-word blocks. Instruction miss rate is 2%, data miss rate 3%

For these processors, one-half of the instructions contain a data reference. Assume that the cache miss penalty is 6 + block size in words. The CPI for this workload is measured on the processor with Cache 1 and was 2.0.

(a) Determine which processor spends the most cycles on cache misses.

(b) If the cycle times are 420ps and 310ps for processor with Cache 1 and 2 respectively, determine which processor is the fastest.