CSE 320 Spring 2014 ***Homework #2 Quiz Version 1***

Name:_______________________________________ID:______________________

No calculators, notes, or textbooks allowed. Show all your work for full credit.
<u>Time limit:</u> 20 mins

$$Z\ \{A,B,C,D,E\} = ABC'D'E' + A'BC'D + CDE$$

<u>Problem 1 [5 points]:</u> Implement the Z using <u>**one**</u> 4-input (2-bit selector) multiplexor and the <u>**minimal**</u> number of 2-input (1-bit selector) multiplexors.

<u>Problem 2 [5 points]:</u> Implement the Z using <u>**one**</u> 16-input (4-bit selector) multiplexor.

(More on back)

$$Z\ \{A,B,C,D,E\} = ABC'D'E' + A'BC'D + CDE$$

Problem 3 [10 points]: Implement Z using a 4-input decoder and the minimal number of AND and/or OR gates.

Problem 2 [4 points]:

$$Z = xy'z' + xy'z + xyz' + x'yz' + x'y'z$$

Implement Z using 2-input multiplexors (1-selector).

DO NOT SIMPLIFY THE INITIAL EXPRESSION. You may simplify the subexpressions into the MUX.

CSE 320 Spring 2014 ***Homework #3 Quiz Version 1***

***Name:*____*ID:*________________________**

No calculators, notes, or textbooks allowed. Show all your work for full credit.
Time limit:* *20 mins

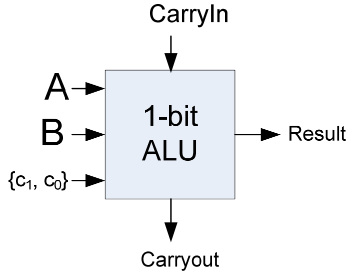
Problem 1: Short answer

a. [2 pts] When performing division of two 12-bit integer numbers, how many clock cycles (iterations of the algorithm) are required?

b. [2 pts] When performing multiplication, which of the following registers is shifter to the left by 1 bit?

□ Multiplicand □ Product □ Multiplier

Problem 2: Consider the following 1-bit ALU with the following delay times for each operation.



Control			***Delay for Result (ns)***	***Delay CarryIn to CarryOut (ns)***
C_1	C_0	***Operation***		
0	0	A + B + CarryIn	3	2
0	1	A XOR B	3	-
1	0	A OR B	2	-
1	1	SLTZ	1	-

a. [4 pts] What is the delay time to complete each operation in the 3-bit ALU?

A + B + Carry_in ______________________________

A XOR B ______________________________

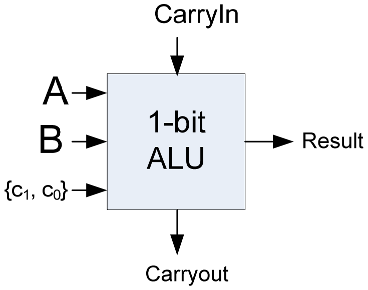
A OR B ______________________________

SLTZ ______________________________

b. [2 points] Which operation determines the overall delay (critical path) of the 3-bit ALU?

(More on back)

Problem 3 [10 points]: Implement the 1-bit ALU with XOR and NAND gates and a single 4-input (2-bit selector) multiplexor. Assume only uncomplemented variables are given. (Hint: Build required gates from NAND gates)



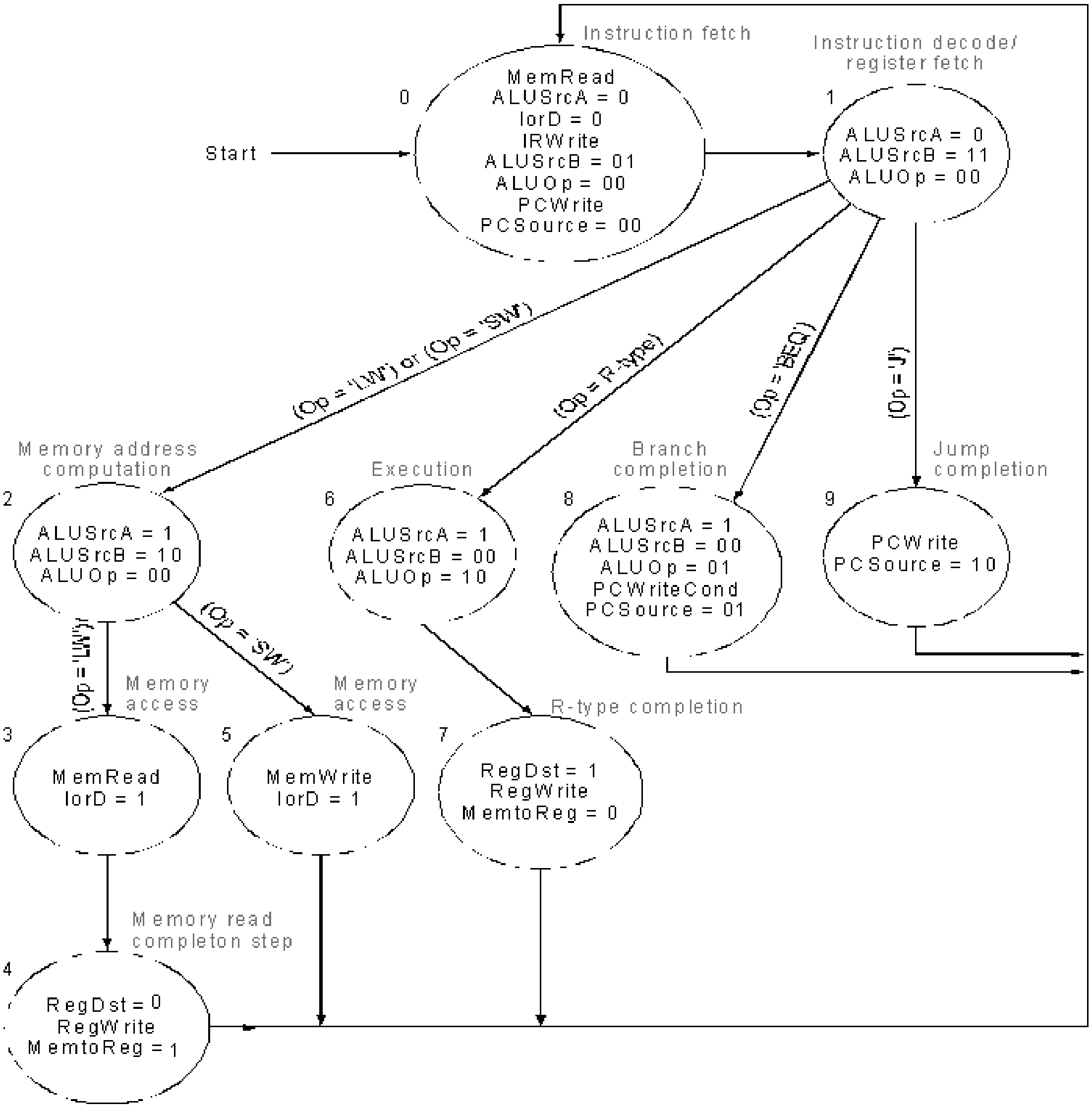
Control		
C_1	C_0	***Operation***
0	0	A + B + CarryIn
0	1	A XOR B
1	0	A OR B
1	1	SLTZ

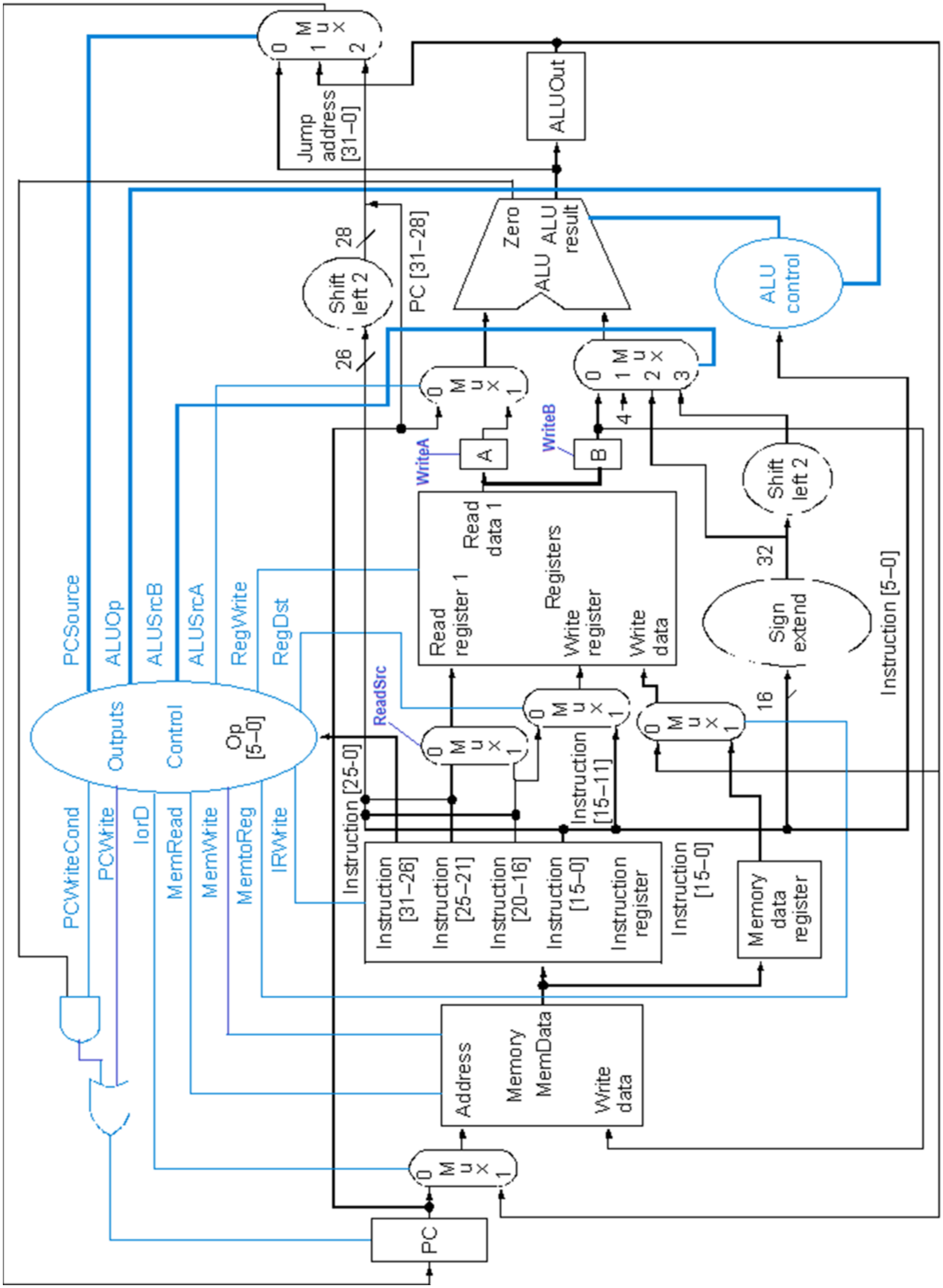
CSE 320 Spring 2014 *Homework #4 Quiz*

***Name:*_______________________________________ *ID:*______________________**

No calculators, notes, or textbooks allowed. Show all your work for full credit.
<u>Time limit:</u> 20 mins

1. Assume the original multicycle datapath is altered to support a register file with only 1 read data port as shown on the handout. Modify the finite state machine control to indicate the control signals for the new datapath.




PCWriteCond
PCWrite
IorD
MemRead
MemWrite
MemtoReg
IRWrite
PCSource
ALUOp
ALUSrcB
ALUSrcA
RegWrite
RegDst
Outputs
Control
Op
[5–0]
PC
Mux
0
1
Address
Memory
MemData
Write
data
Instruction
[31–26]
Instruction
[25–21]
Instruction
[20–16]
Instruction
[15–0]
Instruction
register
Instruction
[15–0]
Memory
data
register
Instruction [25-0]
Instruction
[15–11]
ReadSrc
Read
register 1
Read
data 1
Registers
Write
register
Write
data
16
32
Sign
extend
Shift
left 2
Instruction [5–0]
WriteA
WriteB
A
B
4
2
3
26
28
PC [31–28]
Zero
ALU
ALU
result
ALU
control
ALUOut
Jump
address
[31–0]

CSE 320 Spring 2014 *Homework #5 Quiz Version A*

Name:____ ***ID:***______________________

No calculators, notes, or textbooks allowed. Show all your work for full credit.
<u>Time limit:</u>* *20 mins

Suppose we have two machine implementations of the same instruction set architecture, on which we execute Program P.

- Machine 1 (M1) has a clock rate of 3.0GHz & takes an average of 2.0 clock cycles per instruction (CPI) for P.
- Machine 2 (M2) has a clock rate of 2.5GHz & has a CPI of 1.2 for P.

(a) If program P executes in 8 million instructions (on both machines), how long will it take to run Program P on Machine 1? on Machine 2?

(b) Calculate the average MIPS ratings for each machine, M1 and M2.

(c) Suppose that the 8 million instructions implemented on M1 fall into two performance classes, the first (Class A) takes 1 clock cycle to execute, while the second (Class B) takes 3 clock cycles to execute. How many Class B instructions are executed when program P is run?

(more on back)

Problem 2: Consider two machines with the same instruction set, Machine A and Machine B. Machine B runs floating-point instructions 5 times faster than machine A. Program Q takes 80 seconds to run on machine A and spends 1/4 its time in floating-point instructions. How much faster is machine B (over machine A) at executing this program?

CSE 320 Spring 2014 *Homework #6 Quiz Version A*

Name:____ ID:______________________

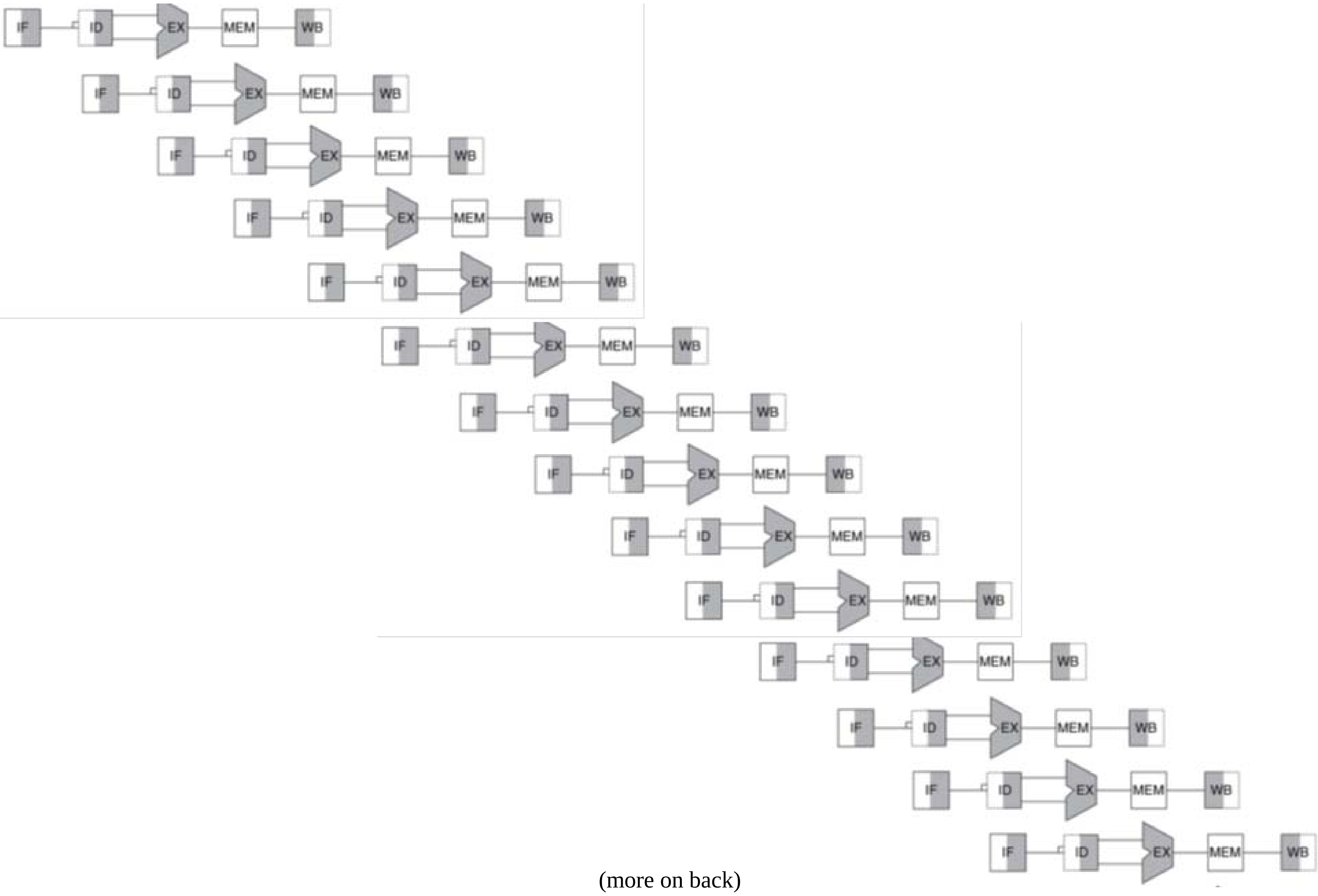
No calculators, notes, or textbooks allowed. Show all your work for full credit.
***Time limit:** 15 mins*

Consider the following MIPS code

```
sw $4, 20 ($6)
sub $3, $4, $6
add $5, $3, $2
1w $7, 100 ($5)
lw $8, 20 ($7)
add $3, $7, $8
```

(a) What type of hazards occurs in the code above? Where do they occur?

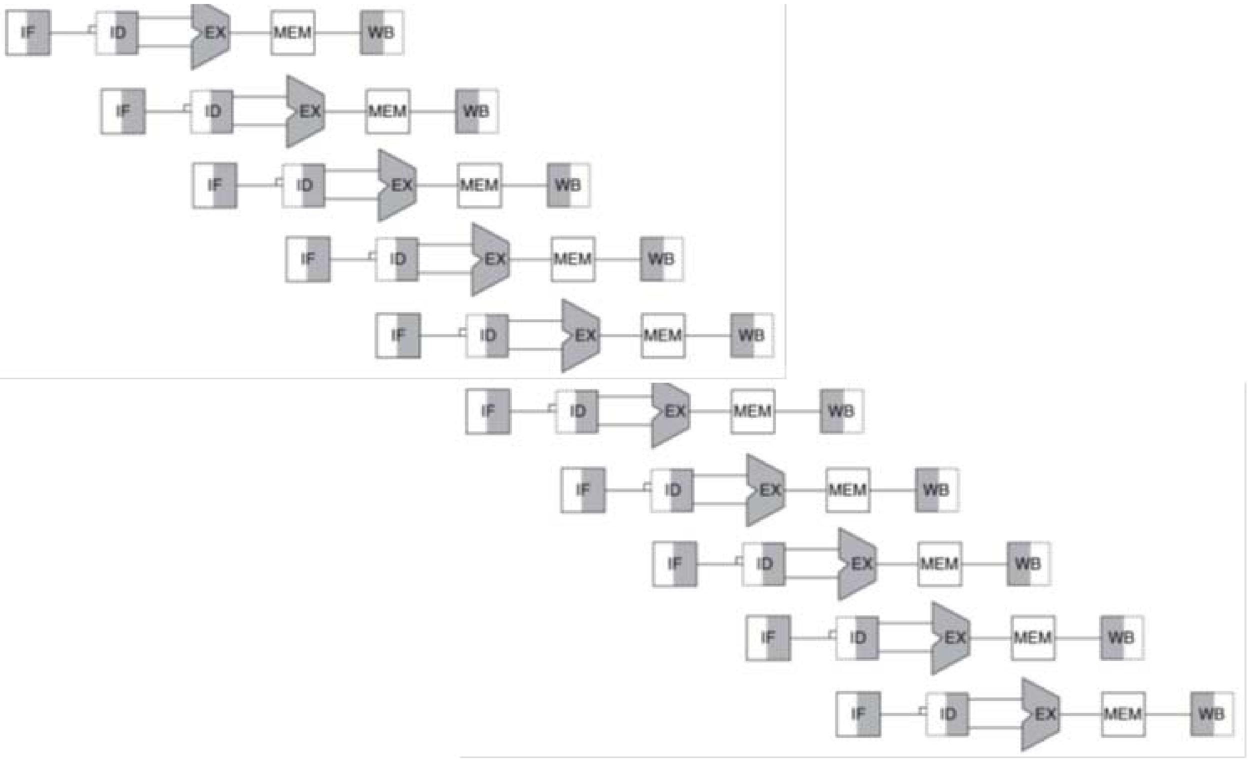
(b) Assume, there is **no forwarding** in the pipeline. Label the instructions and insert stalls (bubbles) to eliminate all hazards (ie. There should be no forwarding lines)



(more on back)

```
sw $4, 20 ($6)
sub $3, $4, $6
add $5, $3, $2
1w $7, 100 ($5)
lw $8, 20 ($7)
add $3, $7, $8
```

(c) Assume there **<u>is forwarding</u>** in the pipeline. Label the instructions; show the forwarding paths and\or stalls needed to execute the code.



(d) Can the code be reordered in order to improve performance? If Yes, Show how. If not, why?