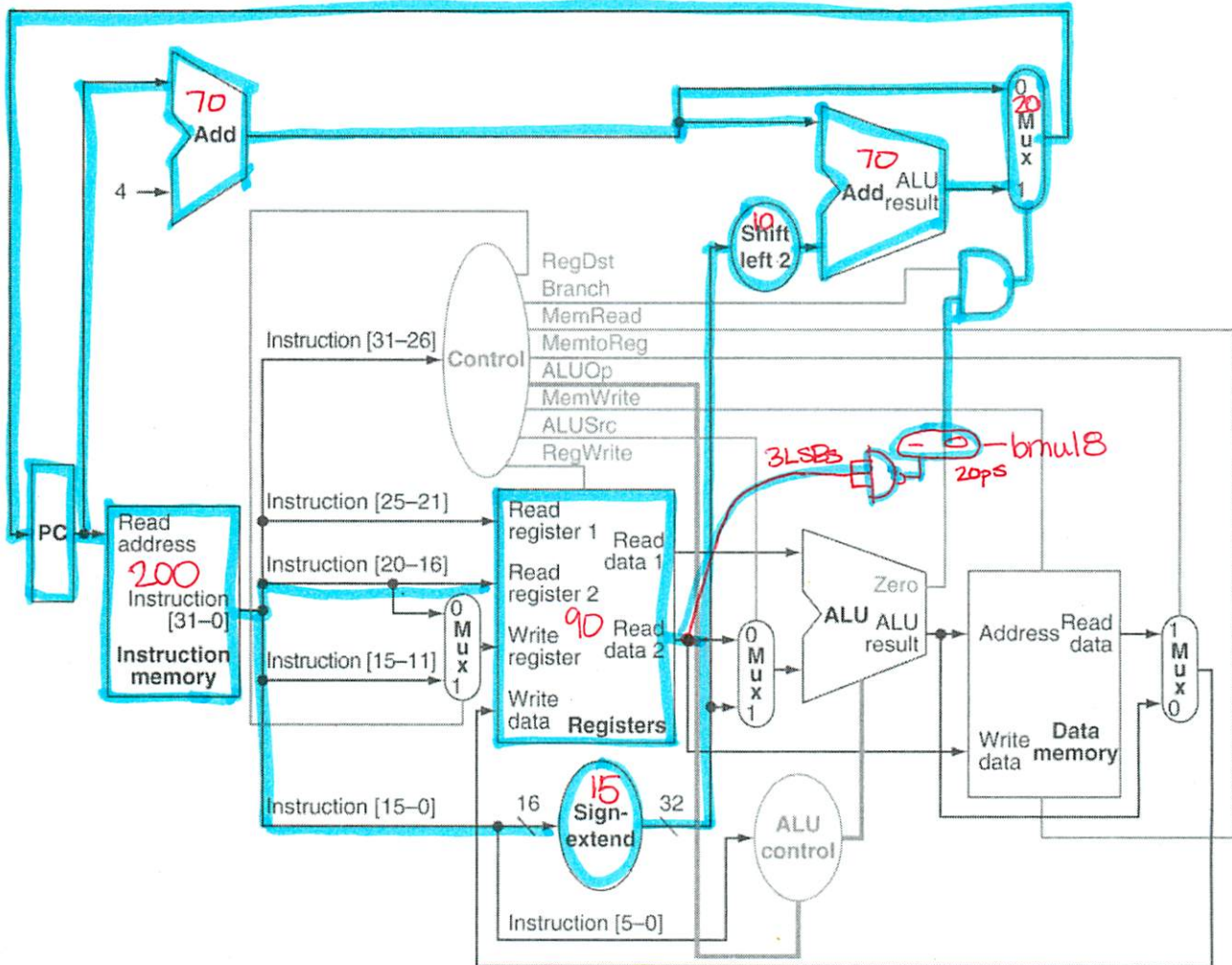


Name: SOLUTION

ID: \_\_\_\_\_

No calculators, notes, or textbooks allowed. Show all your work for full credit.

Time limit: 20 mins



- a. Modify the datapath (above) and control table (below) to implement the new 'bmul8' instruction.  
 bmul8 rt, label # if(Reg[rt] is a multiple of 4) PC <- PC+4 + Instruction[15:0] << 0

Instr	RegDst	RegWrite	ALUSrc	Mem Read	Mem Write	MemtoReg	Branch	ALUOp	bmul8	
lw	0	1	1	1	0	1	0	00	x	
sw	X	0	1	0	1	X	0	00	x	
R-type	1	1	0	0	0	0	0	10	x	
beq	X	0	0	0	0	X	1	01	0	
bmul8	X	0	X	0	0	X	1	XX	1	

- b. Assume the following timing values for the datapath components in ps. All other units are negligible.

I-Mem	Adder	Mux	ALU	Reg File	D-Mem	Sign Ext	Shift Left 2	ALU Control
200	70	20	90	90	250	15	10	30

What is the delay for the bmul8 instruction?

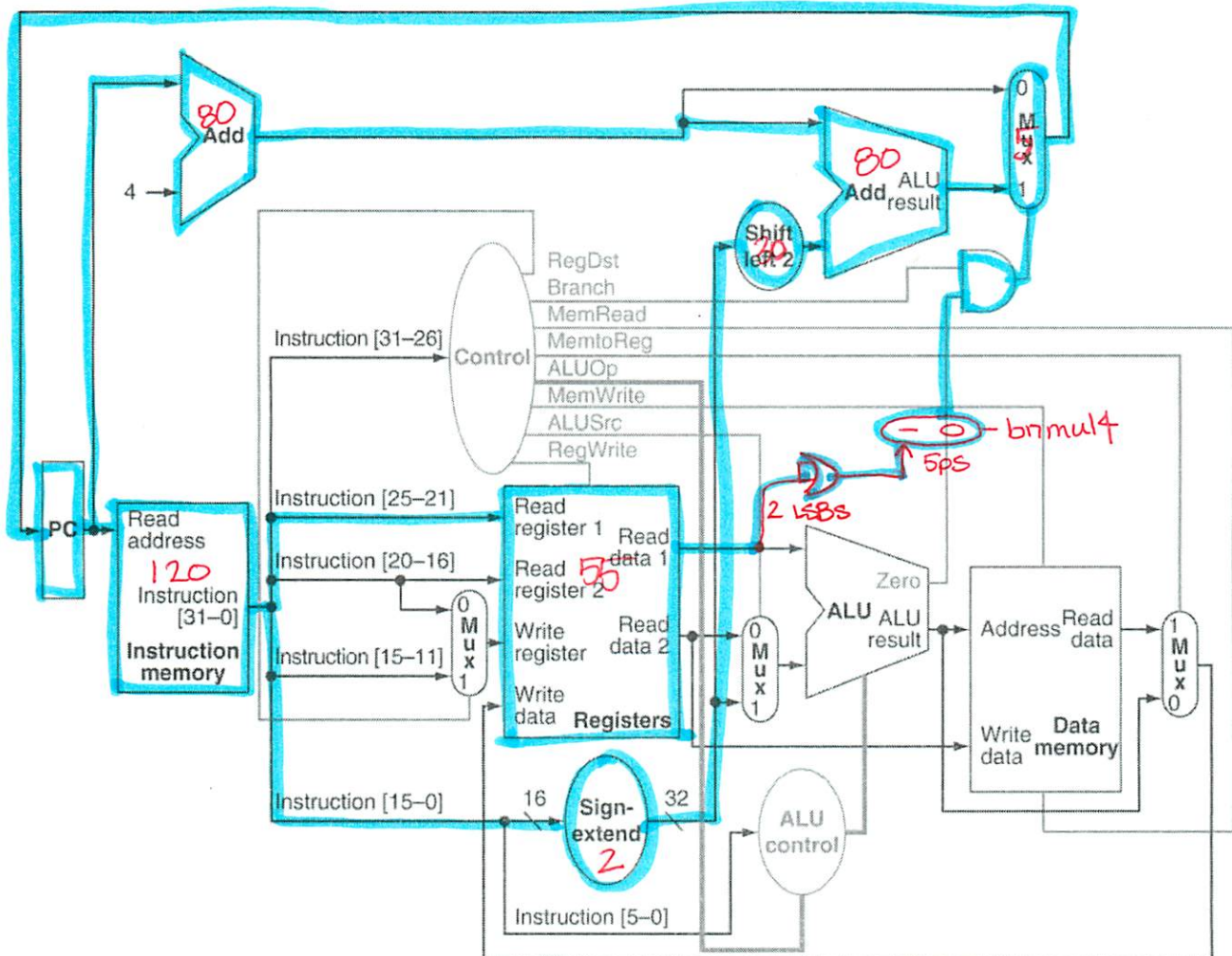
330ps

Name: SOLUTION

ID: \_\_\_\_\_

No calculators, notes, or textbooks allowed. Show all your work for full credit.

Time limit: 20 mins



- a. Modify the datapath (above) and control table (below) to implement the new 'bnmul4' instruction.  
 bnmul4 rs, label      # if(Reg[rs] is NOT a multiple of 4) PC <- PC+4 + Instruction[15:0] << 0

Instr	RegDst	RegWrite	ALUSrc	Mem Read	Mem Write	MemtoReg	Branch	ALUOp	bnmul4	
lw	0	1	1	1	0	1	0	00	x	
sw	X	0	1	0	1	X	0	00	x	
R-type	1	1	0	0	0	0	0	10	x	
beq	X	0	0	0	0	X	1	01	0	
bnmul4	x	0	x	0	0	x	1	xx	1	

- b. Assume the following timing values for the datapath components in ps. All other units are negligible.

I-Mem	Adder	Mux	ALU	Reg File	D-Mem	Sign Ext	Shift Left 2	ALU Control
120	80	5	70	55	250	2	30	30

What is the delay for the bnmul4 instruction? 237 ps