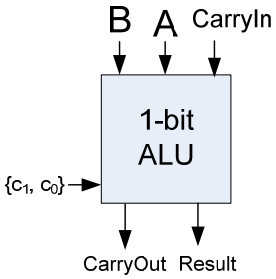
***CSE 320 Fall 2014*** ***Homework #3 Quiz Version 1***

***Name:_____ID:_____***

***No calculators, notes, or textbooks allowed. Show all your work for full credit.***
***Time limit:** 25 mins*

Problem 1: Consider the following 1-bit ALU with the following delay times for each operation.




| *Control* $C_1$ | $C_0$ | *Operation* | *Delay for Result (ns)* | *Delay CarryIn to CarryOut (ns)* |
|---|---|---|---|---|
| 0 | 0 | A + B + CarryIn | 3 | 2 |
| 0 | 1 | A XOR B | 1 | - |
| 1 | 0 | A OR B | 2 | - |
| 1 | 1 | A' | 1 | - |

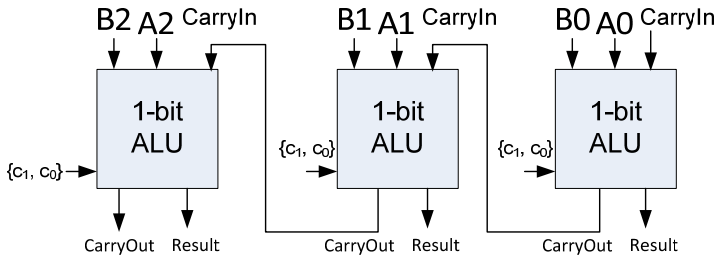
a. [4 pts] What is the delay time to complete each operation in the 3-bit ALU? (Hint: draw the units connected together to build a 3bit ALU first)

A + B + CarryIn ___**7**___

A XOR B ___**1**___

A OR B ___**2**___

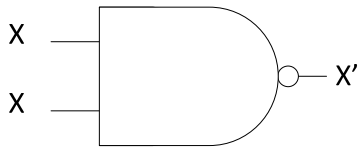
A' ___**1**___




b. [2 points] Which ALU operation determines the overall delay (critical path) of the 3-bit ALU? **A + B + CarryIn**

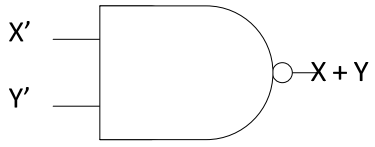
Problem 2 [6 points]: Show that NAND is a universal gate by building the following gates:

NOT:




| *X* | *Y* | *NAND* |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

OR:

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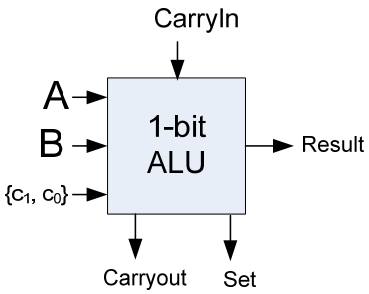
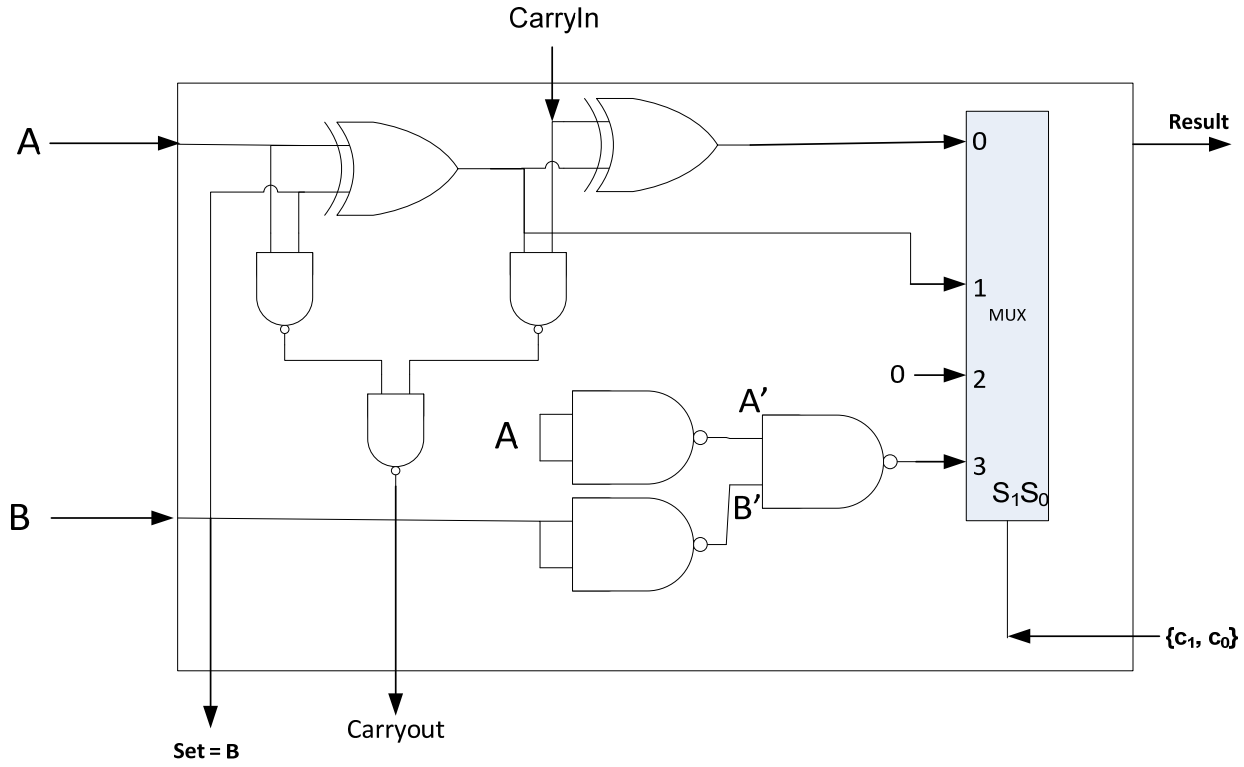
Problem 3 [12 points]: Implement a 1-bit ALU for the Most significant bit of a larger ALU with XOR and NAND gates and a single 4-input (2-bit selector) multiplexor. Assume only uncomplemented variables are given. (Hint: Build any required gates/units from XOR & NAND gates like in problem 2.)




| *Control* $C_1$ | $C_0$ | *Operation* |
|---|---|---|
| 0 | 0 | A+B+CarryIn |
| 0 | 1 | A XOR B |
| 1 | 0 | Set if B is Negative |
| 1 | 1 | A OR B |



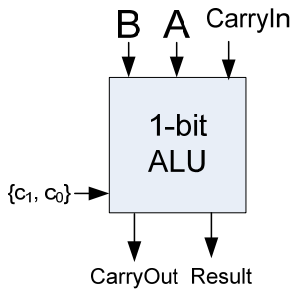

S

***CSE 320 Fall 2014*** ***Homework #3 Quiz Version 2***

***Name:_____ID:_____***

***No calculators, notes, or textbooks allowed. Show all your work for full credit.***
***Time limit:** 25 mins*

Problem 1: Consider the following 1-bit ALU with the following delay times for each operation.




| *Control* $C_1$ | $C_0$ | *Operation* | *Delay for Result (ns)* | *Delay CarryIn to CarryOut (ns)* |
|---|---|---|---|---|
| 0 | 0 | A NAND B | 2 | - |
| 0 | 1 | A + B | 3 | 1 |
| 1 | 0 | B’ | 1 | - |
| 1 | 1 | A + B + CarryIn | 4 | 2 |

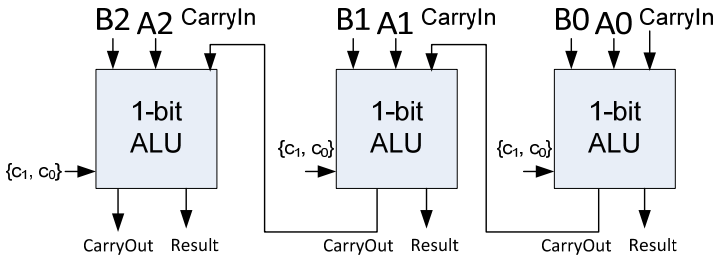
a. [4 pts] What is the delay time to complete each operation in the 3-bit ALU? (Hint: draw the units connected together to build a 3bit ALU first)

A NAND B __2_

A + B __5__

B’ __1__

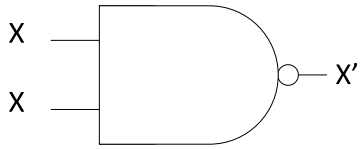
A + B + CarryIn __8__




b. [2 pts] Which ALU operation determines the overall delay (critical path) of the 3-bit ALU?
**A + B + CarryIn**

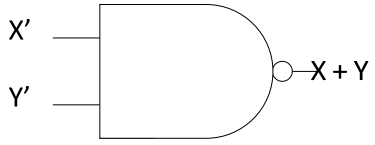
Problem 2 [6 points]: Show that NAND is a universal gate by building the following gates:

NOT:




| *X* | *Y* | *NAND* |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

OR:

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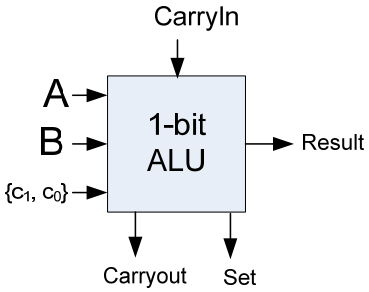
Problem 3 [12 points]: Implement a 1-bit ALU for the Most significant bit of a larger ALU with XOR and NAND gates and a single 4-input (2-bit selector) multiplexor. Assume only uncomplemented variables are given. (Hint: Build any required gates/units from XOR & NAND gates like in problem 2.)




| ***Control*** | | ***Operation*** |
|---|---|---|
| $C_1$ | $C_0$ | |
| 0 | 0 | Set if A is Positive |
| 0 | 1 | A OR B |
| 1 | 0 | A XOR B |
| 1 | 1 | A + B + CarryIn |