CS320 Fall 2014

Homework#7
Quiz in Lecture Thurs Nov 20, 2014
There are no make-up quizzes!

Problem 1: Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 1.2 GHz and M2 has a clock rate of 3 GHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	M1	M2	Frequency
A	1	2	50%
B	2	4	30%
C	5	4	20%

(a) Calculate the average CPI for each machine, M1, and M2.
(b) Calculate the average MIPS ratings for each machine, M1 and M2.
(c) Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

Problem 2: Suppose we have two implementations (M1 and M2) of the same instruction set architecture. Machine 1 has a clock rate of 500MHz and takes an average of 2.0 clock cycles per instruction (CPI) for a program. Machine 2 has a clock rate of 400MHz and a CPI of 1.2 for a program.
(a) Which machine is faster for this program, and by how much?

(b) If a test program executes in 10 million instructions (on both machines), how long will it take to run the program on Machine 1? Machine 2?

(c) Suppose that the 10 million instructions implemented on M1 fall into two performance classes, the first (Class A) takes one clock cycle to execute, while the second (Class B) takes 5 clock cycles to execute. How many Class B instructions are executed when our test program is run?

Problem 3: (Amdahl's law question) Suppose you have a machine which executes a program consisting of 50% floating point multiply, 20% floating point divide, and the remaining 30% are from other instructions.

(a) Management wants the machine to run 4 times faster. You can make the divide run at most 3 times faster and the multiply run at most 8 times faster. Can you meet management's goal by making only one improvement, and which one?

(b) Dogbert has now taken over the company removing all the previous managers. If you make both the multiply and divide improvements, what is the speed of the improved machine relative to the original machine?

Problem 4: Suppose that we can improve the floating point instruction performance of machine by a factor of 15 (the same floating point instructions run 15 times faster on this new machine). What percent of the instructions must be floating point to achieve a Speedup of at least 8?

Problem 5: Multi-cycle performance
Two important parameters control the performance of a processor: cycle time and cycles per instruction. There is an enduring trade-off between these two parameters in the design process of microprocessors. While some designers prefer to increase the processor frequency at the expense of large CPI, other designers follow a different school of thought in which reducing the CPI comes at the expense of lower processor frequency. Consider the following machines, and compare their performance using the following instruction mix: 25% loads, 13% stores, 47% ALU instructions, and 15% branches/jumps. Assume the unmodified multi-cycle datapath and finite state machine.

M1: The multicycle datapath is designed with a 1 GHz clock

M2: A machine like M1 except that register updates are done in the same clock cycle as a memory read of ALU operation. Thus in the finite state machine, states 6 and 7 and states 3 and 4 are combined. This machine has an 3.2 GHz clock, since the register update increases the length of the critical path.

M3: A machine like M2 except that effective address calculations are done in the same clock cycle as a memory access. Thus states 2, 3, and 4 can be combined, as can 2 and 5, as well as 6 and 7. This machine has a 2.8 GHz clock because of the long cycle created by combining address calculation and memory access.

(a) Which of the machines has the shortest cycle time?

(b) Are there instruction mixes that would make another machine have a shorter cycle time, and if so, what are they?

Problem 6: A pipelined processor has a clock rate of 5.5 GHz and executes a program with 5 million instructions. The pipeline has 5 stages, and instructions are issued at a rate of one per clock cycle. Ignore penalties due to branch instructions, and filling and emptying the pipelines.
(a) What is the speedup of the processor for this program compared to a non-pipelined processor?
(b) what is the throughput (in MIPS) of the pipelined processor?

Problem 7: Computer A has an overall CPI of 1.3 and can be run at a clock rate of 3 GHz. Computer B has a CPI of 2.5 and can be run at a clock rate of 2.2 Ghz. We have a particular program we wish to run. When compiled for computer A, this program has exactly 100,000 instructions. How many instructions would the program need to have when compiled for Computer B, in order for the two computers to have exactly the same execution time for this program?

Problem 8: (a) Multiple 8-bit numbers 20010 * 3510 using the multiplier in Figure 3.3 (Page 184 of your book). What is the value in the Product, Multiplicand and Multiplier after 5 clock cycles? How many total times did you use the ALU to Add?
(b) Repeat part (a) using the multiplier in Figure 3.5 (Page 186 of your book). What is the value in the Product register after 4 clock cycles?

Problem 9: Dividing integers: Consider 4-bit binary unsigned division. Divide 6 by 4 using the hardware in Figure 3.8 (Page 190). When calculating the result, how many times did you reset the Remainder back to its previous value.