# Alain Zhang

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## EDUCATION

**University of California San Diego (UCSD)**                                    San Diego, CA
*Master of Science in Computer Engineering*, GPA: 4.0                              June 2027
*Bachelor of Science in Computer Engineering*, GPA: 3.7                            June 2026
Courses: Operating Systems, Advanced Data Structures, Theory of Computation, Design and Analysis of Algorithms, Linear & Nonlinear Optimizations, Computer Architecture, Analog Design, Programming Languages, Compilers

## EXPERIENCE

**SciStream, Argonne National Laboratory**                                         Lemont, IL
*Software Engineering Intern*                                             June 2025 – August 2025
- Automated multi-site networking experiments on FABRIC/ESnet using FABlib APIs; configured SmartNIC/ASIC data-planes for high-throughput evaluation on workloads across distributed compute and networking resources.
- Developed a benchmarking framework with iperf3, GridFTP, and P4-programmed switches to analyze TCP vs. UDP tunnel protocol performance in exascale-class HPC environments.
- Built reproducible pipelines with OpenSSL-secured tunnels, protocol-level debugging, traffic inspection, and real-time logging to streamline workflows and troubleshoot across layers.

**Adaptive Hybrid Systems Laboratory, UC San Diego**                            San Diego, CA
*Research Intern*                                                           Apr 2025 – Present
- Designing reinforcement learning policies for distributed, real-time load shedding on power grids; simulating multi-area grids with communication faults and criticality-based reward shaping.

**UCSD Electrical and Computer Engineering - Engineering Computation**           San Diego, CA
*Tutor and Grader*                                                          Sep 2024 – Present
- Designed and implemented C-language autograder scripts to automatically validate student code.
- Helped lead hour-long review sessions in C for over 200 students under the TA's direction.

## PROJECTS

**STM32 BLE Tracker — Bare-Metal Firmware (C, I2C, BLE)**
- Built BLE advertising firmware in C using BlueNRG-MS stack; triggered wake-on-motion via LSM6DSL sensor ($I^2C$).
- Wrote timer/GPIO drivers for LED symbol encoding at 20Hz; optimized for low-power and stop-mode transitions.
- Conducted hardware bring-up, interrupt testing, and signal debugging using logic analyzer and serial output.

**Real-Time Task Scheduler with DVFS on Raspberry Pi 5 (Embedded Linux)**
- Built an EDF-inspired scheduler for periodic tasks with execution-time profiling and deadline checks.
- Integrated simple DVFS logic to switch CPU frequencies and tracked utilization across idle, low, and high states.

**Armv8 PMU Kernel Module — Performance Counters (Linux Kernel, C/ASM)**
- Developed linux kernel module to configure ARMv8 performance counters; measured instructions, cache hits/misses.
- Accessed system registers via inline assembly, enabling low-level CPU performance profiling and validation.

**Single-Cycle FPU Processor — SystemVerilog + Assembler**
- Designed ISA, ALU, register file, memory, controller modules with support for FP ops and conversion instructions.
- Verified functionality with a SystemVerilog testbench using assertions and functional coverage.

## SKILLS

*Languages*: C, Python, Java, C++, Bash/Batch/Powershell, System Verilog, Assembly (ARM/MIPS)
*Tools*: STM32CubeIDE, logic analyzer, oscilloscope, serial debug, Wireshark
*Concepts*: Bare-metal, RTOS, DVFS, paging, caching, DMA, memory-mapped I/O, interrupts, $I^2C$, SPI, timers
*Version Control & DevOps*: Git, GitHub, GitHub Actions, Docker, Prometheus