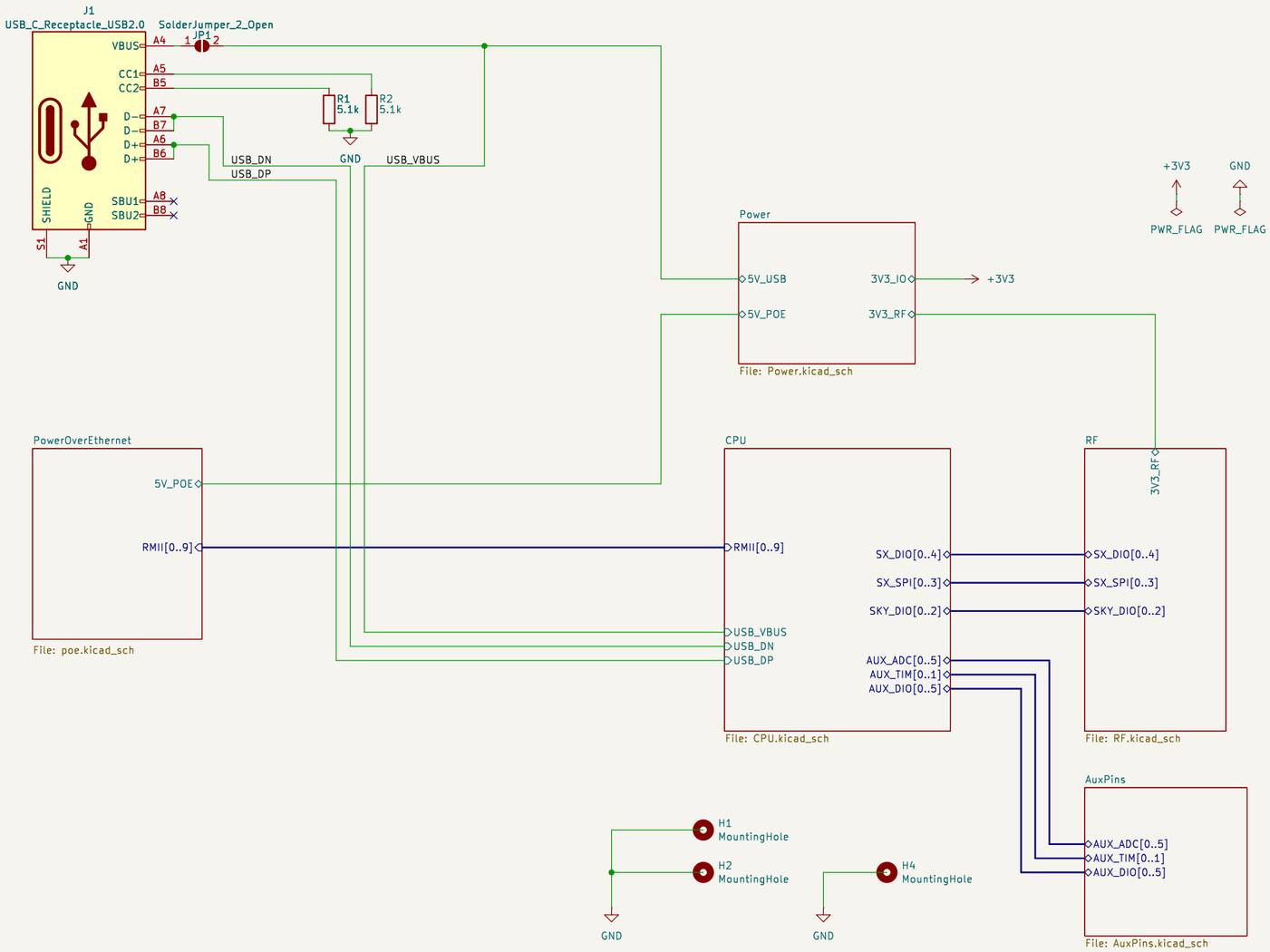

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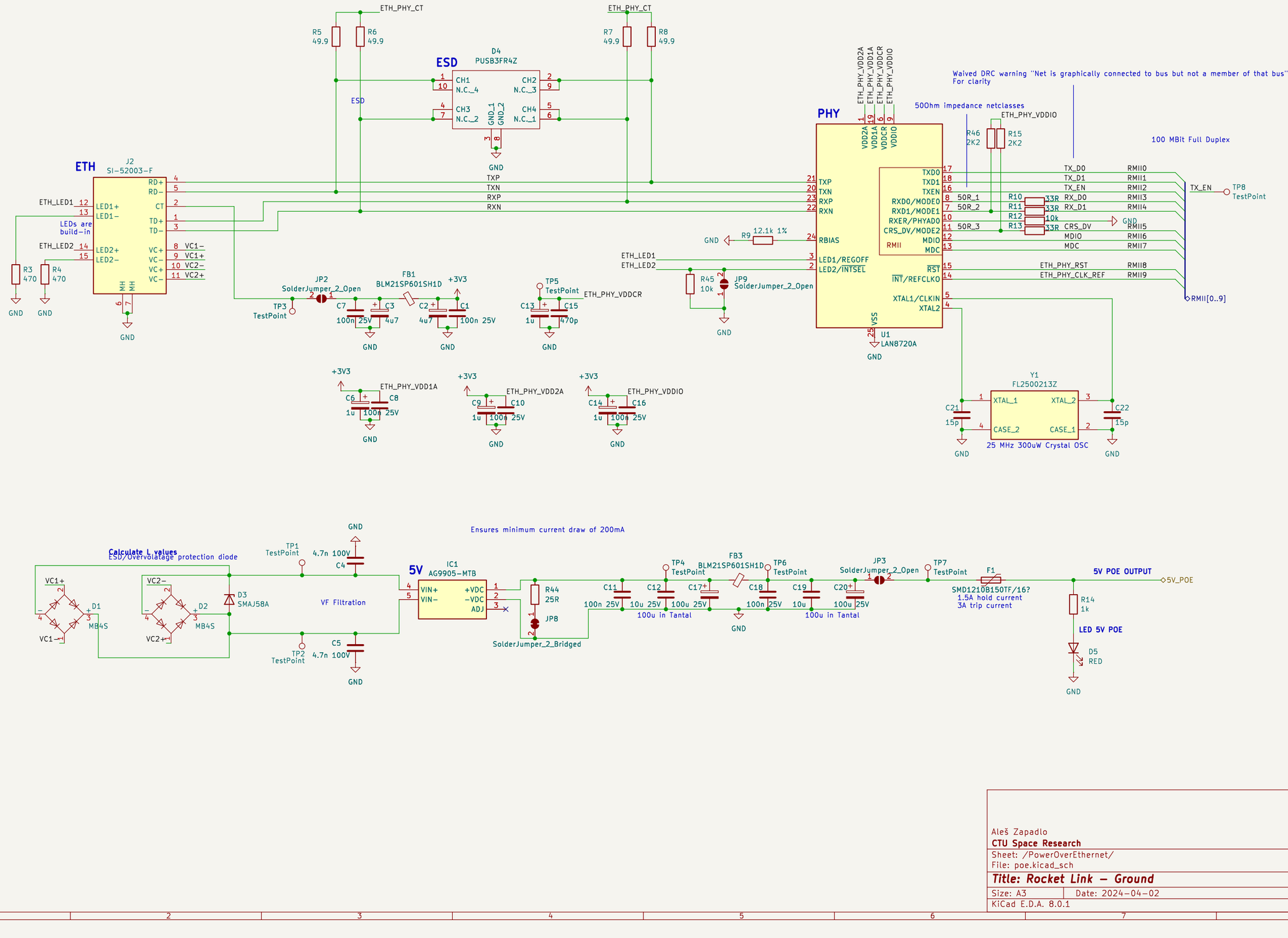
Sheet: /
File: RocketLink_Ground.kicad_sch

Title: Rocket Link – Ground

Size: A3	Date: 2024-04-02	**Rev: 1.0**
KiCad E.D.A. 8.0.1		Id: 1/6


ETH_PHY_CT
R5 49.9
R6 49.9
R7 49.9
R8 49.9
D4
PUSB3FR4Z
ESD
CH1
CH2
CH3
CH4
N.C._4
N.C._3
N.C._2
N.C._1
GND_1
GND_2
GND
ETH
J2
SI-52003-F
RD+
RD-
CT
TD+
TD-
VC+
VC-
LED1+
LED1-
LED2+
LED2-
ETH_LED1
ETH_LED2
LEDs are build-in
R3 470
R4 470
TXP
TXN
RXP
RXN
PHY
VDD2A
VDD1A
VDDCR
VDDIO
ETH_PHY_VDD2A
ETH_PHY_VDD1A
ETH_PHY_VDDCR
ETH_PHY_VDDIO
Waived DRC warning "Net is graphically connected to bus but not a member of that bus" For clarity
500hm impedance netclasses
100 MBit Full Duplex
ETH_PHY_VDDIO
R46 2K2
R15 2K2
TXD0
TXD1
TXEN
RXD0/MODE0
RXD1/MODE1
RXER/PHYAD0
CRS_DV/MODE2
MDIO
MDC
RMII
50R_1
50R_2
50R_3
R10 33R
R11 33R
R12 10k
R13 33R
TX_D0
TX_D1
TX_EN
RX_D0
RX_D1
CRS_DV
RMII0
RMII1
RMII2
RMII3
RMII4
RMII5
RMII6
RMII7
TX_EN
TP8
TestPoint
RMII[0..9]
RST
INT/REFCLKO
ETH_PHY_RST
ETH_PHY_CLK_REF
RMII8
RMII9
XTAL1/CLKIN
XTAL2
VSS
U1
LAN8720A
RBIAS
LED1/REGOFF
LED2/INTSEL
R9 12.1k 1%
R45 10k
JP9
SolderJumper_2_Open
JP2
SolderJumper_2_Open
TP3
TestPoint
FB1
BLM21SP601SH1D
C7 100n 25V
C3 4u7
C2 4u7
C1 100n 25V
+3V3
TP5
TestPoint
ETH_PHY_VDDCR
C13 1u
C15 470p
Y1
FL2500213Z
XTAL_1
XTAL_2
CASE_2
CASE_1
C21 15p
C22 15p
25 MHz 300uW Crystal OSC
C6 1u
C8 100n 25V
C9 1u
C10 100n 25V
C14 1u
C16 100n 25V
ETH_PHY_VDD1A
ETH_PHY_VDD2A
ETH_PHY_VDDIO
Calculate L values
ESD/Overvoltage protection diode
VC1+
VC1-
VC2+
VC2-
D1
MB4S
D2
MB4S
D3
SMAJ58A
VF Filtration
TP1
TestPoint
TP2
TestPoint
C4 4.7n 100V
C5 4.7n 100V
Ensures minimum current draw of 200mA
5V
IC1
AG9905-MTB
VIN+
VIN-
+VDC
-VDC
ADJ
R44 25R
JP8
SolderJumper_2_Bridged
C11 100n 25V
C12 10u 25V
C17 100u 25V
TP4
TestPoint
FB3
BLM21SP601SH1D
TP6
TestPoint
C18 100n 25V
C19 10u
C20 100u 25V
100u in Tantal
JP3
SolderJumper_2_Open
TP7
TestPoint
F1
SMD1210B150TF/16?
1.5A hold current
3A trip current
5V POE OUTPUT
5V_POE
R14 1k
LED 5V POE
D5
RED
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CTU Space Research
Sheet: /PowerOverEthernet/
File: poe.kicad_sch
Title: Rocket Link – Ground
Size: A3
Date: 2024-04-02
Rev: 1.0
KiCad E.D.A. 8.0.1
Id: 2/6

MCU PROG. LED

LED_BLUE_1 LED_BLUE_2
R16 1k
R17 1k
LED_BLUE_1 D6 BLUE
D7 BLUE LED_BLUE_2
GND GND

+3V3
SolderJumper_3_Bridged12 JP4
TP13 TestPoint
R18 100k
GND

Y2
ABM8AAIG-8.000MHz-V2R-T3
RCC_OSC_IN RCC_OSC_OUT
C23 6p
C24 6p
GND

J3 Conn_01x02_Pin
NRST
TP10 TestPoint
C25 100n 25V
GND GND

+3V3
C28 1u
C29 100n 25V
GND

+3V3
C30 100n 25V
C31 1u
C32 100n 25V
C34 1u
C36 100n 25V
C38 1u
C40 100n 25V
C41 1u
GND

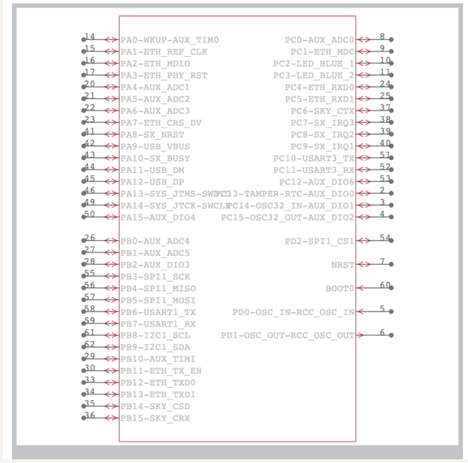
PWR_FLAG
FB2 BLM21SP601SH1D
+3V3
C33 1u
C35 100n 25V
C37 100n 25V
C39 1u
GND GND

U2
STM32F107RCTx

7	NRST				
60	BOOT0				
		RCC_OSC_IN	5	PD0	
		RCC_OSC_OUT	6	PD1	
SX_SPI[0..3]	SX_SPI3	SPI_CS	54	PD2	
AUX_ADC[0..5]	AUX_ADC0		8	PC0	
RMII[0..9]	RMII7	MDC	9	PC1	
		LED_BLUE_1	10	PC2	
		LED_BLUE_2	11	PC3	
	RMII3	RX_D0	24	PC4	
SKY_DIO[0..2]	RMII4	RX_D1	25	PC5	
SX_DIO[0..4]	SKY_DIO1	SKY_CTX	37	PC6	
	SX_DIO4	SX_IRQ3	38	PC7	
	SX_DIO3	SX_IRQ2	39	PC8	
	SX_DIO2	SX_IRQ1	40	PC9	
		USART3_TX	51	PC10	
		USART3_RX	52	PC11	
AUX_DIO[0..5]	AUX_DIO5		53	PC12	
	AUX_DIO0		2	PC13	
	AUX_DIO1		3	PC14	
	AUX_DIO2		4	PC15	
		AUX_TIM0		PA0	AUX_TIM[0..1] RMII[0..9]
		ETH_PHY_CLK_REF	RMII9	PA1	
		MDIO	RMII6	PA2	
		ETH_PHY_RST	RMII8	PA3	
		CRS_DV	RMII5	PA4	
			AUX_ADC1	PA5	AUX_ADC[0..5]
			AUX_ADC2	PA6	
			AUX_ADC3	PA7	SX_DIO[0..4]
		SX_NRST	SX_DIO1	PA8	
		SX_BUSY	SX_DIO0	PA9	USB[0..2]
			USB_VBUS	PA10	USB_VBUS
			USB_DN	PA11	USB_DN
			USB_DP	PA12	USB_DP
		SWDIO		PA13	
		SWDCLK		PA14	
			AUX_DIO4	PA15	AUX_DIO[0..5]
			AUX_ADC4	PB0	AUX_ADC[0..5]
			AUX_ADC5	PB1	
			AUX_DIO3	PB2	AUX_DIO[0..5]
		SPI_CLK	SX_SPI2	PB3	SX_SPI[0..3]
		SPI_MISO	SX_SPI0	PB4	
		SPI_MOSI	SX_SPI1	PB5	
		USART1_TX		PB6	
		USART1_RX		PB7	
	R19 100	I2C_CLK		PB8	
	R20 100	I2C_SDA		PB9	
			AUX_TIM1	PB10	AUX_TIM[0..1] RMII[0..9]
		TX_EN	RMII2	PB11	
	50R_4	TX_D0 R21 33R	RMII0	PB12	
	50R_5	TX_D1 R22 33R	RMII1	PB13	SKY_DIO[0..2]
	50R_6	SKY_CSD	SKY_DIO0	PB14	
		SKY_CRX	SKY_DIO2	PB15	

VBAT VDD VDD VDD VDD VDDA VSS VSSA MCU_VSSA GNDGND

Symbol



I2C header
J16 I2C
GND SCL SDA 3V3
+3V3
R25 4.7k
R26 4.7k
I2C_CLK
I2C_SDA
SP4065-08ATG
IC10
ESD I2C/USART3

NRST
AUX_TIM1
AUX_TIM0

GND
IC3
SP4065-08ATG
ESD

SWD header
J15 SWD
3V3 SWCLK GND SWDIO MCU_NRST
+3V3
SWDCLK
SWDIO
NRST

USART3 LED
+3V3
R23 1k
R24 1k
D8 BLUE
D9 BLUE
USART3_RX
USART3_TX

USART1 LED
+3V3
R27 1k
R28 1k
D10 BLUE
D11 BLUE
USART1_RX
USART1_TX

USART1 Debug header
J14 UART
GND RX TX 3V3
+3V3
IC2
SP4065-08ATG
USART1_RX
USART1_TX

USART3 Debug header
+3V3
USART3_TX
USART3_RX
3V3 TX RX GND
UART J4
GND

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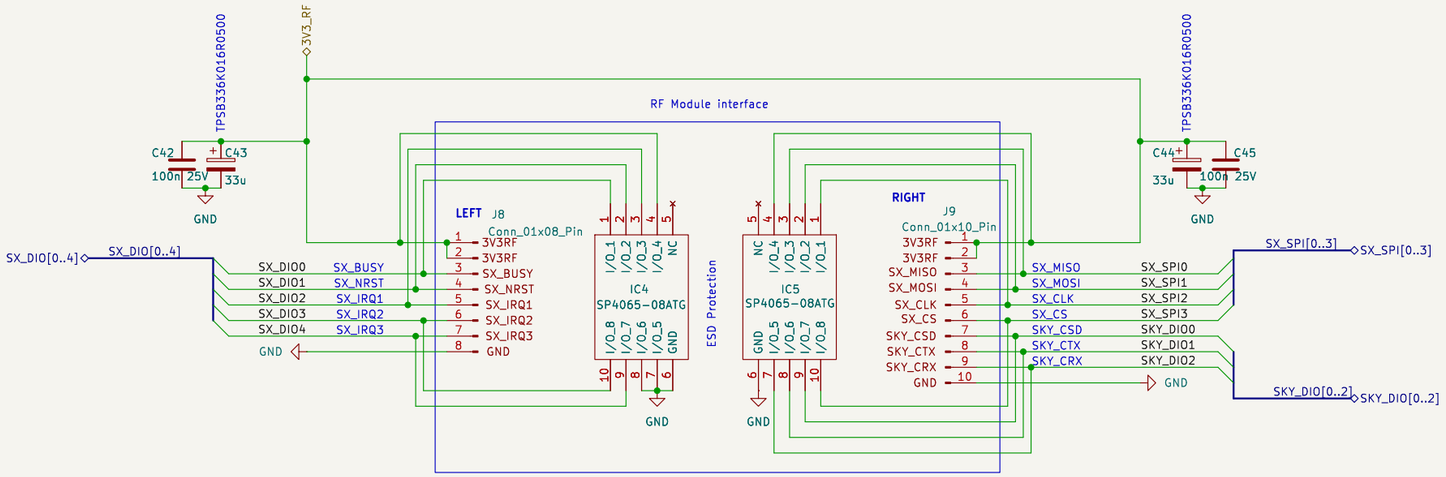
Sheet: /CPU/
File: CPU.kicad_sch
Title: Rocket Link – Ground

Size: A3	Date: 2024-04-02	**Rev: 1.0**
KiCad E.D.A. 8.0.1		Id: 3/6



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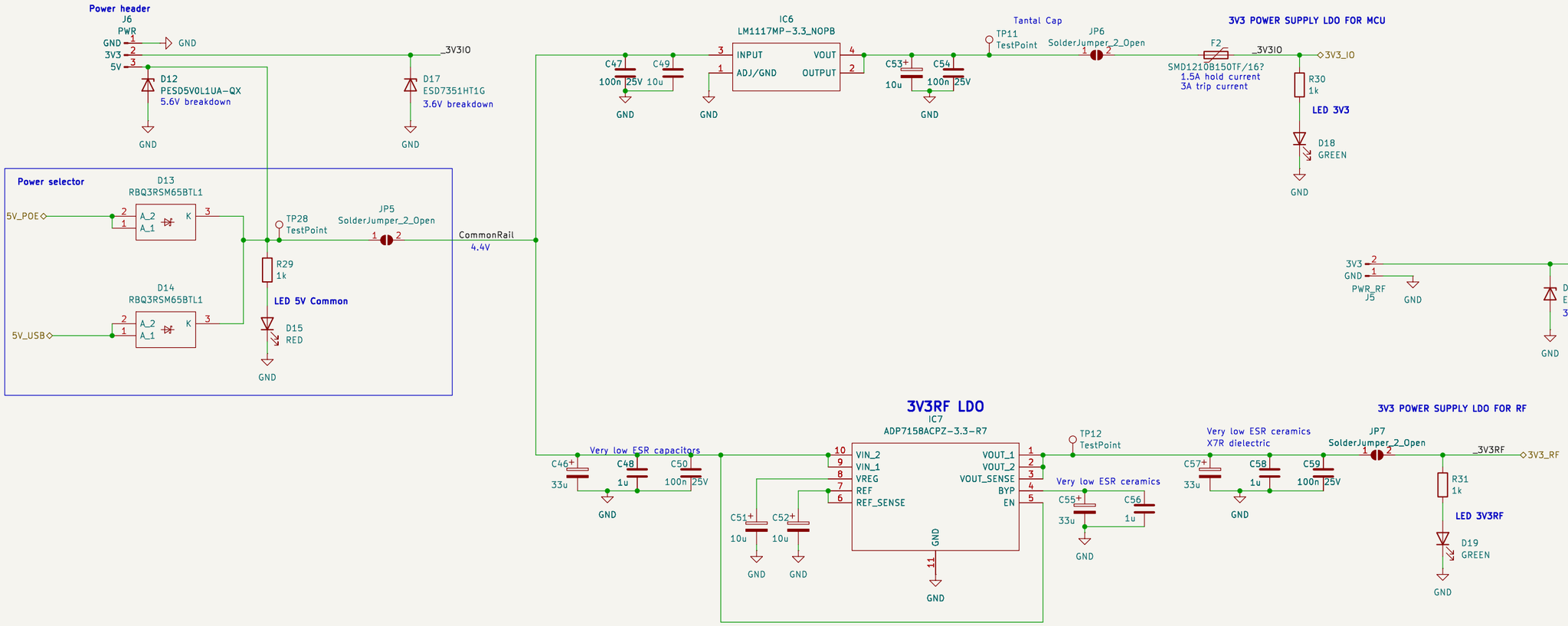
Sheet: /RF/		
File: RF.kicad_sch		
Title: Rocket Link – Ground		
Size: A3	Date: 2024-04-02	**Rev: 1.0**
KiCad E.D.A. 8.0.1		Id: 4/6



PCB LAYOUT CONSIDERATIONS

Place the input capacitor as close as possible between the VIN pin and ground. Place the output capacitor as close as possible between the VOUT pin and ground. Place the bypass capacitors (C_{REG}, C_{REF}, and C_{BYP}) for V_{REG}, V_{REF}, and V_{BYP} close to the respective pins (VREG, REF, and BYP) and ground. The use of a 0805, 0603, or 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited. Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.

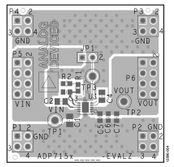


Figure 62. Sample 10-Lead LFCSP PCB Layout

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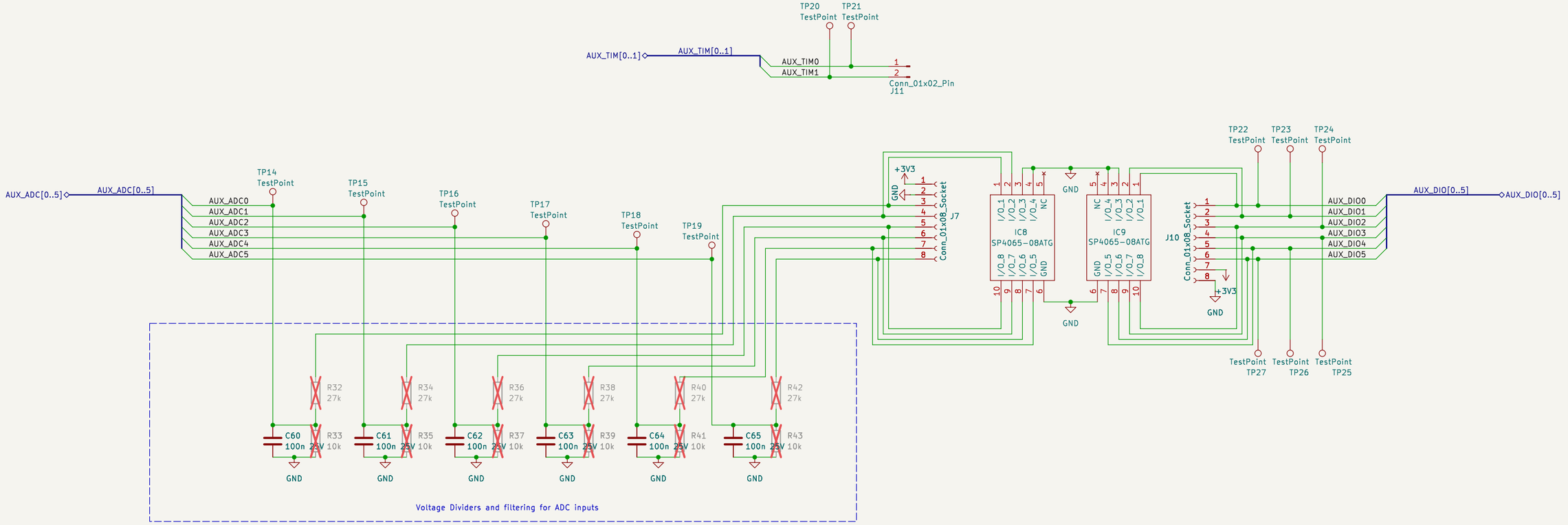
Sheet: /Power/
File: Power.kicad_sch

Title: Rocket Link – Ground

Size: A3	Date: 2024-04-02	**Rev: 1.0**
KiCad E.D.A. 8.0.1		Id: 5/6



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Sheet: /AuxPins/
File: AuxPins.kicad_sch

Title: Rocket Link – Ground

Size: A3	Date: 2024-04-02	**Rev: 1.0**
KiCad E.D.A. 8.0.1		Id: 6/6