



1. Description

1.1. Project

Project Name	STM32F401CDU6_PWM
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	06/02/2024

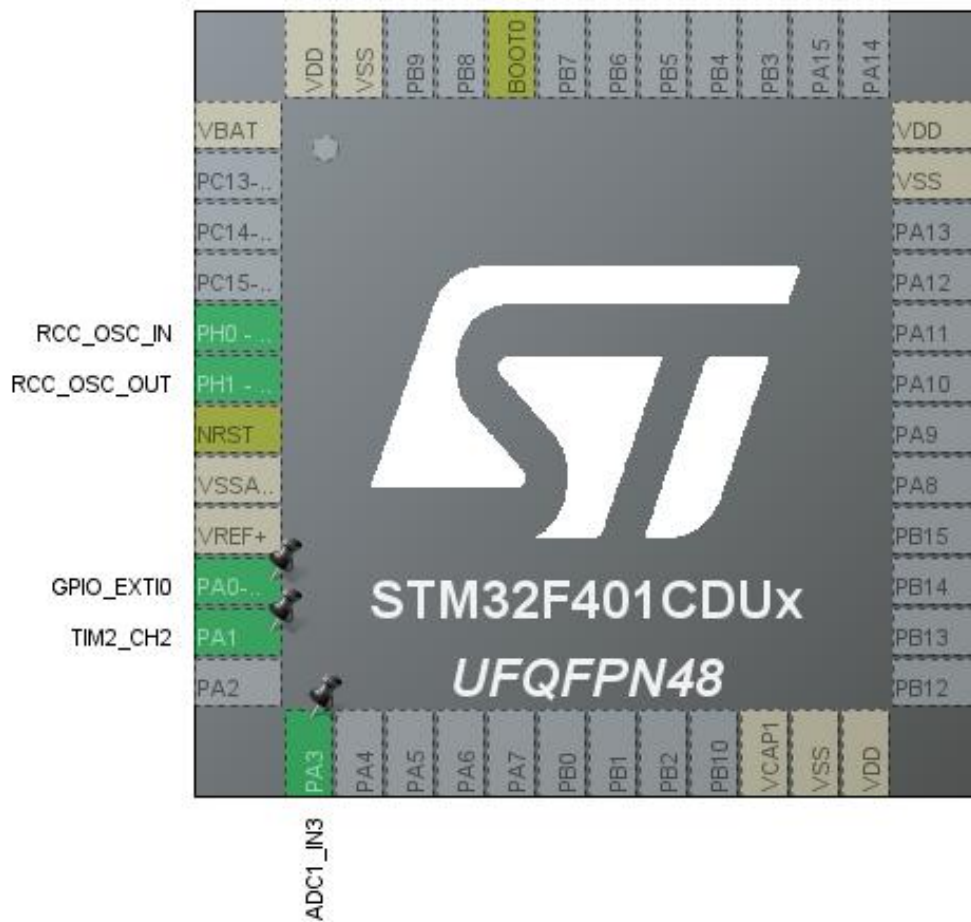
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F401
MCU name	STM32F401CDUx
MCU Package	UFQFPN48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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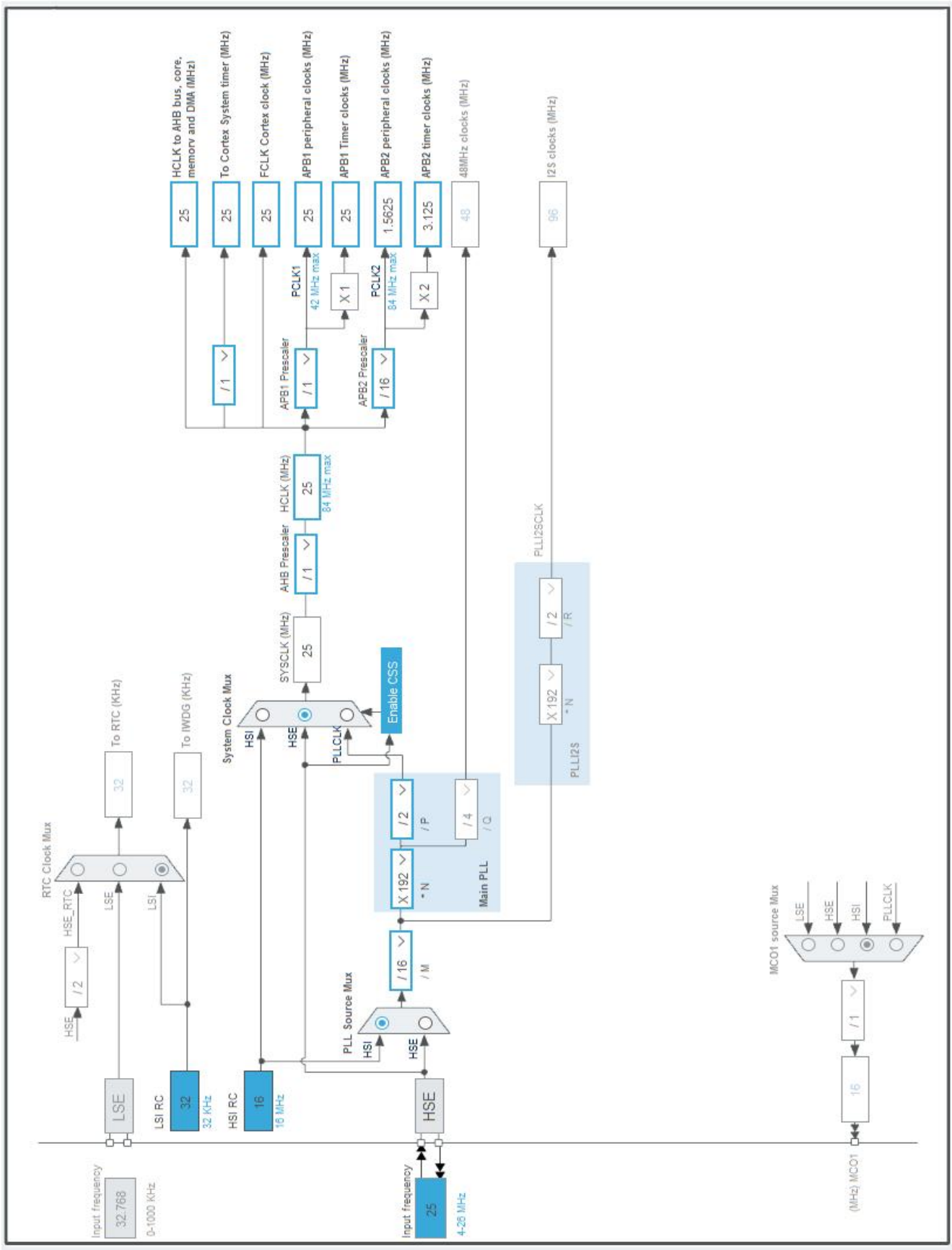
2. Pinout Configuration



3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VREF+	Power		
10	PA0-WKUP	I/O	GPIO_EXTI0	
11	PA1	I/O	TIM2_CH2	
13	PA3	I/O	ADC1_IN3	
22	VCAP1	Power		
23	VSS	Power		
24	VDD	Power		
35	VSS	Power		
36	VDD	Power		
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32F401CDU6_PWM
Project Folder	C:\Users\Siraj\STM32CubeIDE\workspace_1.14.0\STM32F401CDU6_PWM
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_TIM2_Init	TIM2
5	MX_ADC1_Init	ADC1

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F401
MCU	STM32F401CDUx
Datasheet	DS10086_Rev3

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

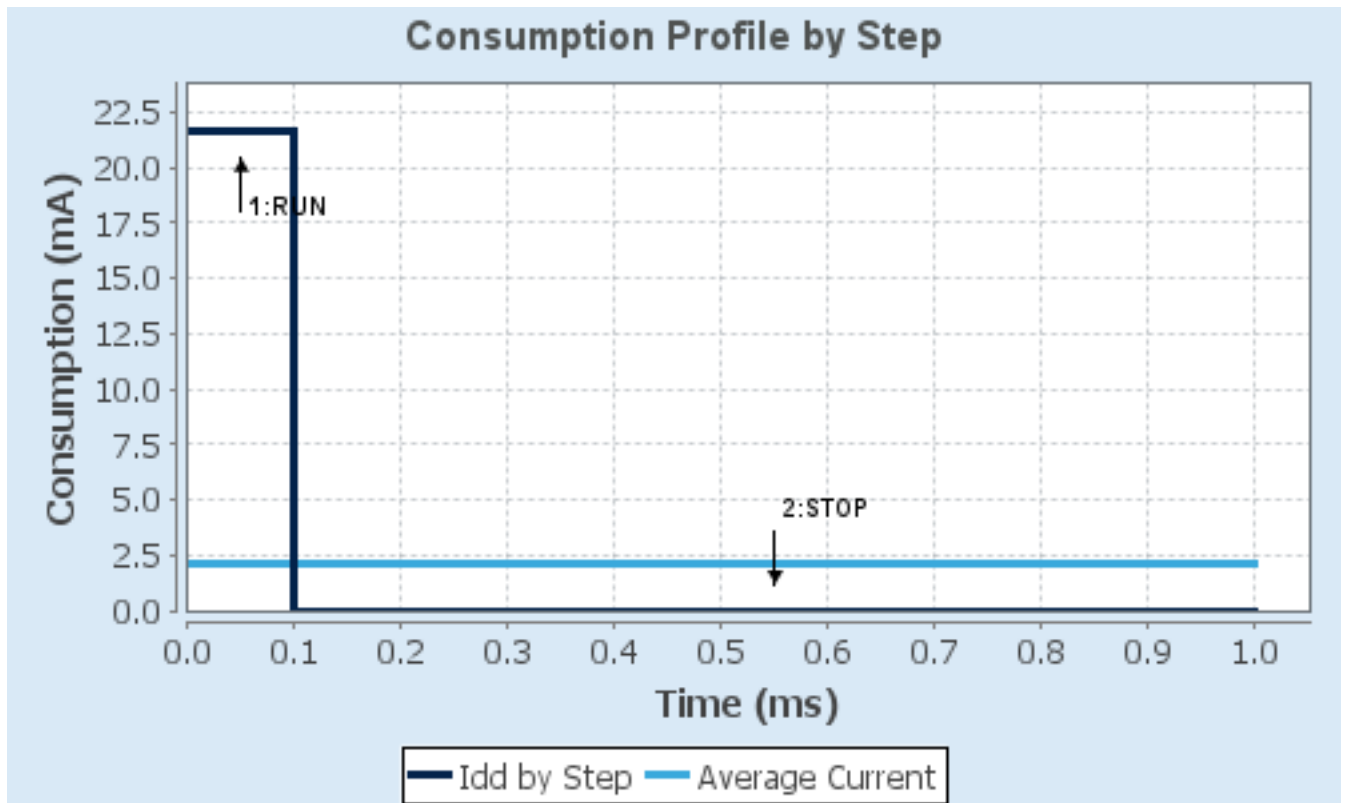
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale2-Medium	No Scale
Fetch Type	FLASH/ART/PREFETCH	n/a
CPU Frequency	84 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	21.6 mA	10 μ A
Duration	0.1 ms	0.9 ms
DMIPS	105.0	0.0
Ta Max	102.72	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.17 mA
Battery Life	2 months, 4 days, 8 hours	Average DMIPS	105.0 DMIPS

1.6. Chart



2. Peripherals and Middlewares Configuration

2.1. ADC1

mode: IN3

2.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests **Enabled ***

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 3

Sampling Time **480 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

2.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Instruction Cache Enabled

Prefetch Buffer Enabled

Data Cache Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
TIM Prescaler Selection Disabled
HSE Startup Timeout Value (ms) 100
LSE Startup Timeout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 2

2.3. SYS

Timebase Source: SysTick

2.4. TIM2

Clock Source : Internal Clock

Channel2: PWM Generation CH2

2.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) **25000-1 ***
Counter Mode Up
Counter Period (AutoReload Register - 32 bits value) **500-1 ***
Internal Clock Division (CKD) No Division
auto-reload preload **Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)
Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode PWM mode 1
Pulse (32 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PA0-WKUP	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	Pull-down *	n/a	

3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: **Circular ***
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
EXTI line0 interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
TIM2 global interrupt	unused		
FPU global interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line0 interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Computing
DMA ✓	ADC1 ✓	TIM2 ✓			
GPIO ✓					
IVVIC ✓					
RCC ✓					
SYS ✓					

5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f401_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f401_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f4_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
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Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32f4x1.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstmcsuite.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Product Certifications	https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an4646-peripheral-interconnections-on-stm32f401-and-stm32f411-lines-stmicroelectronics.pdf
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for related Tools [mcu-power-modes-with-best-dynamic-efficiency-stmicroelectronics.pdf](https://www.st.com/resource/en/application_note/an4365-using-stm32f4-for-related-Tools-mcu-power-modes-with-best-dynamic-efficiency-stmicroelectronics.pdf)

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