



main

Gates

**D AND Gate**

..... NAND Gate  
..... NOR Gate

XNOR Gate

☒ Even Parity

Controlled  
Plexers

Memory

**Base**

Facing

Data Bits

### Pull Behavior

### Label Location

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East

No

No

Unch

C	
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West

Sans

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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