Seema Gangaiah Aarella

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Professional Statement

I am a passionate researcher in the field of security aware Internet-of-Things(IoT) and Cybersecurity, my research involves Secure Authentication systems for Edge Data Centers in Collaborative Edge Computing environment. The goal of my research is to model secure and energy aware authentication system to provide security for the cyberphysical systems in Smart Village environment. Developing hardware assisted security solutions using Physically Unclonable Functions (PUF), Certificate Authority(CA), integrating Machine Learning(ML) models in the security systems for secure authentication and monitoring of Edge Data Centers against external attacks.

Education

Ph.D. in Computer Science and Engineering — Aug. 2019 – Present
University of North Texas — *Denton, TX*

Master of Science, Engineering Systems — Aug. 2012 – May 2014
University of North Texas — *Denton, TX*

Master of Technology, VLSI and Signal Processing — Aug. 2010 – May 2012
Jain University — *Bangalore, India*

Bachelor of Engineering, Electronics and Communication — Jan. 1996 – Sept 2000
Bangalore University — *Bangalore, India*

Research Interests

- Cybersecurity, Hardware-Assisted Security, Security-by-Design(SbD), Secure Authentication System, Collaborative Edge Computing, Machine Learning, Security of Cyberphysical Systems for Smart Village infrastructure, XORArbiter PUF based Secure Authentication System, SRAM PUF based Certificate Authority(CA) for secure authentication of Edge Data Centers during Load Balancing, External Attack Detection and Prevention, Machine Learning models for Intrusion Detection and Anomaly Detection, Security of Cyberphysical Systems

Experience

Teaching Assistant — Jan 2020 – Present
UNIVERSITY OF NORTH TEXAS — *Denton, TX*

- Teaching Assistant (TA) for **CSCE 1030: Computer Science**
- Conducting C and C++ labs for a 3 sections of 30-40 students in each, on weekly basis
- demostration and instruction delivery, teaching students to use tools like PuTTY, WinSCP, MinGW, Nano, Vim and Notepad++
- Teaching students to write readable, efficient and correct C/C++ programs that include programming structures such as assignment statements, selection statements, loops, arrays, pointers, console and file I/O, structures, command line arguments, both standard library and user-defined functions, and multiple header (.h) and code (.c or .cpp) files
- Design and implement programming solutions to problems in C or C++, teach software process model that can be used to develop significant applications composed of hundreds of functions
- explaining code logic and helping in debugging and error handling, teach the steps necessary to edit, compile, link and execute C/C++ programs
- Grading code submissions for each lab, every week, Conduction Lab exams and grading the exams, Grading C and C++ projects

- Holding weekly office hours to tutor students, provide extra help with the course and Zybook activities

Research Assistant May 2023 – July 2023
UNIVERSITY OF NORTH TEXAS *Denton, TX*

- Assisted in organizing NSF-funded Easy-Med: Interdisciplinary Training in Security, Privacy-Assured Internet of Medical Things
- Delivered lectures about the on-going research based on Security of Cyber Physical Systems, Collaborative Edge Computing, Secure Authentication System and other peer research
- Demostrated the working models of Secure Authentication for Edge Data Centers
- Demonstrated the working of Machine Learning Models for Secure Authentication Monitoring and Intrusion Detection
- Conducted hardware demonstration of peer research related to IoMT

Teaching Assistant Jun. 2021 – Aug. 2021
UNIVERSITY OF NORTH TEXAS *Denton, TX*

- Teaching Asisstant (TA) for **CSCE 2110: Foundations of Data Structures**
- Design and implement programming solutions to problems in C or C++ in IDEs like XCode, Visual Studio Code, and compilers like MinGW
- Teaching to create pseudocode and flowcharts, use of abstraction in the design and implementation of algorithms, such as sorting and searching algorithms, use of hash tables in design of software
- Provide instructions and demostration of unit tests and testing strategies for C/C++ programs, GNU debugger(gdb) for C and C++ codes
- Teaching and supervising the complete implementation of project in GitLab, creating tasks, merging and closing tasks on GitLab Board
- Teaching git commands to set up local credentials, local repository, staging files, committing files, modifying files, working with branches and remote server
- Holding weekly office hours to tutor students, provide extra help with the course, and address queries regarding the subject, helping students with queries on their Zybook activities

Software Engineer Nov 2015 – Oct 2016
HMSA (BLUE CROSS BLUE SHEILD) *Honolulu, HI*

- Worked as lead developer to design, implement ETL solutions on Trizetto process in Agile Scrum envrionment
- Worked on retrofit, upgrade and maintenance of data for HHIN (Hawaii Healthcare Information Network)
- Worked with tools like TOAD, SQLDeveloper to connect to oracle database to write queries and generate the result
- Performed Unit Testing, Integration testing, Regression testing, troubleshooting and bug fixing in development, IST, QA/UAT environments
- Involved in knowledge transfer to the end users and created extensive documentation on the design, development, implementation, daily loads and process flow of the Informatica mappings
- Worked as offshore coordinator for a team of offshore developers delegating ETL development work, providing solutions and support, writing test cases, testing their applications and deploy to TEST and PROD
- Worked on TIDAL job scheduler, creating new jobs, running existing and providing production support and monitoring jobs
- Worked as production support for the team every two weeks as a routine, monitoring job, reporting status, fixing bugs
- Worked on SQL server 2012 database used for the PROVIDER data, developed applications to extract and load data into HHIN database
- Worked on Retrofit Project, retrofitted the existing applications for a change in the existing table in the SQL server source schema

- Worked on retrofitting the existing SSIS or RS packages for the change in source schema table, tested and deployed to production
- Worked on Serena Business Manager to create DBA requests and schedule and track deployments to TEST and PROD environments

Programmer Analyst Jan 2015 – Nov 2015
PEGASUS INFO TECH *Dallas, TX*

- Worked on Data Integration projects to extract, analyze, transform and load data to Operational Data Store
- Developed mappings using ETL tools for sources like Oracle, DB2, SQL Server, flat files to load into BI system
- Worked on complete Extract, transformation and load process (ETL) using Informatica 9.6.1/9.5/9.1.1 application development and upgrades from 9.1 to 9.5 to 9.6.1
- Worked in all phases of SDLC using Agile and Waterfall methodologies for Data Integration, including requirement gathering from business users, analysis, design, creation of business requirement documents, mapping documents, impact/gap analysis document, ETL development, testing, and implementation
- Organizing, defining, translating, refining, and documenting business requirements into well-defined functional and technical specifications
- Developed ETL jobs for PreForeClosure applications
- Developed mappings using various transformations in Designer to extract the data from relational sources like Oracle and non-relational source like flat files to perform mappings based on company requirements and load into ODS and BI system
- Used different tasks (Session, Command, Decision, Timer, Email, Event-Raise, Event-Wait, and Control) in the workflow
- Performed Unit Testing, Integration testing, Regression testing, troubleshooting and bug fixing in development, IST, QA/UAT environments
- Worked on TIDAL job scheduler/ Control-M scheduler, creating new jobs, running existing and providing production support and monitoring jobs
- Involved in knowledge transfer to the end users and created extensive documentation on the design, development, implementation, daily loads and process flow of the Informatica mappings

Intern Sep 2014 – Dec 2014
COMPNOVA *Plano, TX*

- Worked on application development using ETL Informatica in Agile based environment
- Performance Tuning Informatica Targets, Sources, mappings and sessions.Incremental loading Target databases using SCD Type1/Type2 loads
- Creating an Integration Service, Repository Service, repository backup, restore repositories
- Integration of data sources like Oracle 11g/10g/9i/8i, DB2, MS SQL Server 2005/2000, Flat Files, XML files
- Developing and debugging Informatica mappings, mapplets, sessions, and workflows
- Worked on non-relational sources like Flat files and used secure FTP, SSH, Hummingbird, worked on Oracle PL/SQL programming, Stored procedures
- Designing, implementing, and maintaining project templates for business analysis, quality assurance scope management, and change management
- Performing Unit Testing, Integration testing, Regression testing, troubleshooting and bug fixing in development, IST, QA/UAT environments
- Well versed in using HP ALM (formerly Mercury Quality Center) to document defects

Student Assistant May 2014 – Mar 2015
UNIVERSITY OF NORTH TEXAS *Denton, TX*

- Software and Windows Server maintenance (2008, 2010), management of all the labs in the ETEC department

- Computer hardware assembly and troubleshooting, Cloning, Deployment, Windows Server installation and maintenance
- Coordination and scheduling, system updating and installing necessary applications on demand
- Tech support to all systems across all the labs
- Installation and maintenance of NetSupport school software

Teaching Assistant Aug 2013 – May 2014
UNIVERSITY OF NORTH TEXAS *Denton, TX*

- Conducted laboratory work for Engineering Undergraduate students
- Asisted students in leraning Matlab, Simulink, LogixPro, Multisim, Quartus II
- Assisted students and professors in project work in the courses - Digital control of industrial processes, Circuit analysis, Advanced circuit analysis

Lecturer Nov 2001 – Jul 2003
KUPPAM COLLEGE OF ENGINEERING *Kuppam, India*

- Teaching core Electronics and Communication courses
- Creating course materials and scheduling the courses
- Establising the laboratories for related courses, creating lab syllabus, lab manuals, ordering electronic equipments, organizing labs
- Recruting laboratory assistants and instructors, assigning lab work to assitants and monitoring
- Conducting internal course examinations, lab examinations and grading
- Conducting student seminars, assigning seminar topics to students in current trends in Electronics and Communications Technology, supporting students with projects realted to the course
- working with the college management in conducting and organizing technical events and annual events
- Served as member of Disciplinary Committee
- **Courses Handled as Lecturer:**
- Semiconductor Devices and circuits
- Pulse and Digital Circuits
- Analog Communication
- Television Engineering
- Telecommunication
- Digital communication

Publications

Conferences

- **S. G. Aarella**, Saraju P Mohanty, and Elias Kougianos (2023). "Fortified Edge 3.0: A Lightweight Machine Learning Based Approach forSecurity in Collaborative Edge Computing", In 21st OITS International Conference on Information Technology (OCIT)(OCIT-2023) (pp. 6).
- **S. G. Aarella**, S. P. Mohanty, E. Kougianos and D. Puthal, "Fortified-Edge 2.0: Machine Learning based Monitoring and Authentication of PUF-Integrated Secure Edge Data Center", in Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2023, pp. 1-6, DOI: https://doi.org/10.1109/ISVLSI59464.2023.10238517.
- **S. G. Aarella**, S. P. Mohanty, E. Kougianos and D. Puthal, "Fortified-Edge: Secure PUF Certificate Authentication Mechanism for Edge Data Centers in Collaborative Edge Computing", in Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI), 2023, pp. Accepted, DOI: https://doi.org/10.1145/3583781.3590249.

- **S. G. Aarella**, S. P. Mohanty, E. Kougianos and D. Puthal,"PUF-based Authentication Scheme for Edge Data Centers in Collaborative Edge Computing", in Proceedings of the IEEE International Symposium on Smart Electronic Systems (iSES), 2022, pp. 433–438, DOI: https://doi.org/10.1109/iSES54909.2022.00094.

- **S. G. Aarella**, A. K. Tripathy, S. P. Mohanty, and E. Kougianos, "EasyBand2.0: A Framework with Context-Aware Recommendation Mechanism for Safety-Aware Mobility during Pandemic Outbreaks", in Proceedings of the 23rd International Symposium on Quality Electronic Design (ISQED), 2022, pp. 187–193, DOI: https://doi.org/10.1109/ISQED54688.2022.9806250.
- **S. G. Aarella**, A. K. Tripathy, S. P. Mohanty, and E. Kougianos, "iTour2.0: A Smart Tourism Application for Independent Mobility of Tourists", in Proceedings of the OITS International Conference on Information Technology (OCIT), 2021, pp. 472–477, DOI: https://doi.org/10.1109/OCIT53463.2021.00097.
- **S. G. Aarella**, V. P. Yanambaka, S. P. Mohanty, and E. Kougianos, "Fortified-Edge 4.0: A ML-Based Error Correction Framework for Secure Authentication in Collaborative Edge Computing", in Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI), 2024, pp. 639–644, DOI: https://doi.org/10.1145/3649476.3660384.

- V. Parlapalli, V. Jayaram, **S. G. Aarella**, K. Peddireddy and R. R. Palle, "Enhancing Cybersecurity: A Deep Dive into Augmented Intelligence Through Machine Learning and Image Processing," 2023 International Workshop on Artificial Intelligence and Image Processing (IWAIIP), Yogyakarta, Indonesia, 2023, pp. 96-100, doi: 10.1109/IWAIIP58158.2023.10462845.

Presentations

- **S. G. Aarella**, S. P. Mohanty, E. Kougianos and D. Puthal, "Fortified-Edge 2.0: Machine Learning based Monitoring and Authentication of PUF-Integrated Secure Edge Data Center", in Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2023, pp. 1-6, DOI: https://doi.org/10.1109/ISVLSI59464.2023.10238517.
- **S. G. Aarella**, S. P. Mohanty, E. Kougianos and D. Puthal, "Fortified-Edge: Secure PUF Certificate Authentication Mechanism for Edge Data Centers in Collaborative Edge Computing", in Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI), 2023, pp. Accepted, DOI: https://doi.org/10.1145/3583781.3590249.

- **S. G. Aarella**, S. P. Mohanty, E. Kougianos and D. Puthal,"PUF-based Authentication Scheme for Edge Data Centers in Collaborative Edge Computing", in Proceedings of the IEEE International Symposium on Smart Electronic Systems (iSES), 2022, pp. 433–438, DOI: https://doi.org/10.1109/iSES54909.2022.00094.
- **S. G. Aarella**, A. K. Tripathy, S. P. Mohanty, and E. Kougianos, "EasyBand2.0: A Framework with Context-Aware Recommendation Mechanism for Safety-Aware Mobility during Pandemic Outbreaks", in Proceedings of the 23rd International Symposium on Quality Electronic Design (ISQED), 2022, pp. 187–193, DOI: https://doi.org/10.1109/ISQED54688.2022.9806250.
- **S. G. Aarella**, A. K. Tripathy, S. P. Mohanty, and E. Kougianos, "iTour2.0: A Smart Tourism Application for Independent Mobility of Tourists", in Proceedings of the OITS International Conference on Information Technology (OCIT), 2021, pp. 472–477, DOI: https://doi.org/10.1109/OCIT53463.2021.00097.
- **S. G. Aarella**, V. P. Yanambaka, S. P. Mohanty, and E. Kougianos, "Fortified-Edge 4.0: A ML-Based Error Correction Framework for Secure Authentication in Collaborative Edge Computing", in Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI), 2024, pp. 639–644, DOI: https://doi.org/10.1145/3649476.3660384.

- **S. G. Aarella**, "FPGA Implementation of Floating Point Arithmetic Processor", Indian Society for Technical Education, Tumkur, India, 14-15 Oct 2011

Other Publications

- **Seema G. Aarella**, Author - 'Letters From The Heart' - ISBN: 9789380154015 - 2009

Awards and Honors

- **CENG/DT Award(85%)** University of North Texas, 2021-2023 - $540
- **NSF Student Travel Grant** for 2023 IEEE Computer Society International Symposium on VLSI (IEEE ISVLSI), 2023 - $500

- **NSF Student Travel Grant** for 2022 IEEE International Conference on Communications (IEEE ICC), 2022 - $300

- **Tuition Benefit Scholarship** Toulouse Graduate School, University of North Texas, 2020-2023
- **Tuition Benefit Scholarship** Toulouse Graduate School, University of North Texas, 2023-2024
- **TGS Academic Achievement Award**, University of North Texas, 2020-2021 - $1000
- **TGS Academic Achievement Award**, University of North Texas, 2019-2020 - $1000

Academic Projects

NSF AWARD OAC-1924112:EASY-MED (Student Volunteer) May 2023

- Training STEM students with sensing, security, and privacy-aspects of smart healthcare and provide them a career path in smart healthcare
- Participated in student enrollment request screening and selecting candidates for the project
- Participated in organizing the training through the course
- Delivered lectures about the on-going research based on Security of Cyber Physical Systems, Collaborative Edge Computing, Secure Authentication System and other peer research
- Demostrated the working models of Secure Authentication for Edge Data Centers
- Demonstrated the working of Machine Learning Models for Secure Authentication Monitoring and Intrusion Detection

JACOBSTHAL NUMBER CALCULATOR May 2014

- Tools - C, Verilog, Matlab, ModelSim, Quartus II, Altera DE 115 FPGA
- In mathematics, the Jacobsthal numbers are an integer sequence named after the German mathematician Ernst Jacobsthal. Like the related Fibonacci numbers, they are a specific type of Lucas sequence defined by a similar recurrence relation
- Software realization of Jacobstal Number Calculator was coded by using C and Matlab which displayed the output for a given input - n
- Hardware realization of the same was written in Verilog and simulated in ModelSim and implemented into the Altera FPGA

IMPLEMENTATION OF 4-BIT FLOATING POINT ARITHMETIC PROCESSOR May 2012

- Tools - VHDL, ModelSim, Leonardo Spectrum, Xilinx Virtex II pro
- Floating point numbers have sign, mantissa and exponent. 4-bit processor was designed using state machines to add, subtract, multiply and divide floating point numbers
- Code was written in VHDL, simulated in ModelSim and implemented in Xilinx Virtex II Pro FPGA

IMPLEMENTATION OF DWT FOR IMAGE COMPRESSION May 2011

- Tools - VHDL, ModelSim
- This Project describes principles of Discrete Wavelet Transformation (DWT) and provides VHDL implementation of it applied to Image compression
- Standard JPEG2000 for picture compression is based on this process
- DWT using Le Gall 5/3 filter bank was designed and implemented in VHDL into two parts - DWT2D and IDWT2D
- The modules were simulated in ModelSim for direct transformation and for inverse transformation to perform one-dimensional DWT and IDWT of the signal

TELECARD OCT 2000

- Tools - Smart Card, C, JAVA
- A Tele card is a smart card based electronic card used to make local and long distance phone calls over a telephone line. The telecard containes user information and the cash amount that is due
- The Tele card is inserted to the interface slots that form a connection loop with the phone. once the call is connected the pulse is counted and after the call the cost of the call gets deducted from the card memory and new balance is written
- The hardware comprised of the fabricated Tele card having EEPROM chip for PC interface. Software for the interface was developed using C and JAVA

Peer Reviewer - Journals & Conferences

- SNCS (Springer Nature Computer Science)
- ACM JETC(ACM Journal on Emerging Technologies in Computing Systems)
- IEEE OJCOM (Open Journal of the Communications Society)
- International Journal of Advanced Computer Science and Applications
- Integration
- Machine Learning with Applications
- Software Impacts
- IEEE International Symposium on Smart Electronics (IEEE iSES) 2023
- IEEE International Conference on Digital Health (IEEE ICDH) 2023
- IEEE International Symposium on Smart Electronics (IEEE iSES) 2022
- IEEE ICC WS-04 2ND Workshop on Metaverse-based Networking, Computing and Security (METANCS) 2024
- International Conference on Mathematical Modelling & Computer Simulation in Artificial Intelligence (UKSim) 2024

Judge

- **16th Annual 2023 Globee Awards for Women in Business**, Globee Business Awards
- **11th Annual 2023 Leadership Awards**, Globee Business Awards
- Expert Education Judge **CODiE Awards 2024**
- Industry Judge for **Globee Awards for Cybersecurity 2024**
- Industry Judge for **Globee Awards for Technology 2024**
- Industry Judge for **Golden Bridge Awards 2024**
- Industry Judge for **Globee Awards for American Business 2024**

Certifications

- Course Completion Certificate, **Introduction to Generative Adversarial Networks (GANs)**, LinkedIn Learning, Nov 2023
- Certificate of Excellence **"Technical Writing Skills"**, Researcher Academy, Oct 2023
- Certificate of Excellence **"Fundamentals of Peer Review"**, Researcher Academy, Oct 2023
- Certificate of Excellence **"Certified Peer Reviewer Course"**, Researcher Academy, July 2023
- Certificate of Attendance **"2022 IEEE ICC Conference Seoul, South Korea"** (virtual), May 2022
- Course Completion Certificate,**"Create Smart Maps in Python and Leaflet"**, Udemy, May 2021
- Course Completion Certificate, **"Web Development in Java and Advanced Java"**, Sun Microsystems, April 2000

Professional Development Activities

- Completed the Graduate Student Teaching Excellence Program (GSTEP) course, to develop and refine teaching skills, Spring 2023

Professional Organization Member

- IEEE Student
- IEEE Young Professionals
- IEEE Computer Society
- IEEE Computer Society's Technical Community on Security and Privacy
- ACM Professional
- IAENG (International Association of Engineers)

Technical Skills

Languages: Python, C, C++, Java, Assembly, Shell Scripting, VHDL, Verilog, SQL, PL/Sql

Databases: Oracle 11g/10g/9i/8i/7.x, IBM DB2, MS SQL Server 2005/2008/2012, SQLite3

Developer Tools: Git, VS Code, PyCharm, MCUXpresso IDE, Arduino IDE, Raspbian, Mu Editor

EDA Tools: Mentor Graphics ModelSim, Leonardo Spectrum, Precision RTL, IC Flow, AMS, Xilinx EDK, ISE, CodeWarrior, LogixPro, Quartus II, LabView, Multisim, NIOS II, iMPACT, ChipScope Pro, Matlab

ETL Tools: Informatica Power Center 9.x/8.x/7.x, PowerExchange

HDLs: VHDL, Verilog

FPGAs: Xilinx Virtex II Pro, Altera DE2