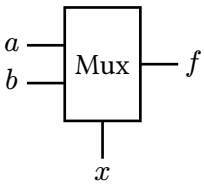
Digital Electronics

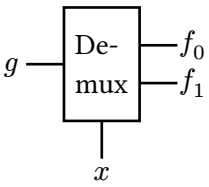
Components

2-to-1 Selector (Multiplexer)



a	b	x	f
X	b	0	b
a	X	0	a

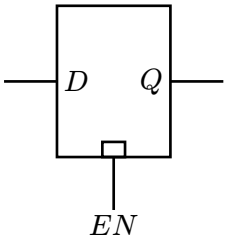
Demultiplexer



g	x	f_0	f_1
g	0	g	0
g	1	0	g

A **decoder** is a demux with g set to 1.

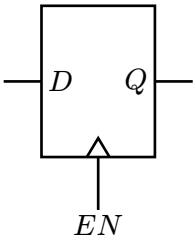
Level-triggered D Flip-flop



A 1 input version of the RS-latch.

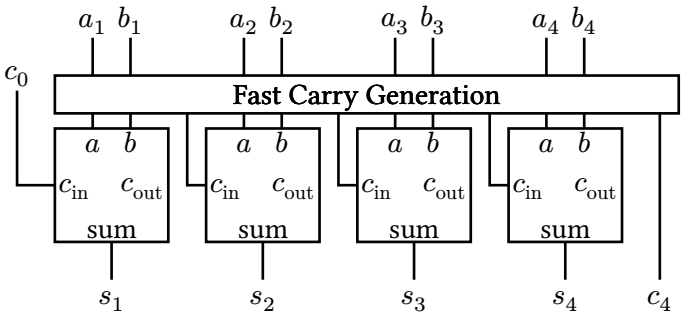
- $EN = 1$ then $Q = D$
- $EN = 0$ then Q unchanged.

Edge-triggered D Flip-flop



Output changes only on a rising edge.

In addition, there are the **programmable logic array** and **ROM**. Multiple memory devices can be connected to the same bus with **tristate buffers** which disconnects from the bus when not selected.



c_{in}	a	b	c_{out}
?	0	0	0
?	0	1	?
?	1	0	?
?	1	1	1

The level of c_4 is reduced $8 \to 5$

Combinatory Logic

Combinatory output depends only on current input.

- **Disjunctive normal form** (sum of product) is the sum minterms.
- **Conjunctive normal form** (product of sum) is the product of maxterms.

Hazards are brief changes in output, multilevel logic can introduce hazards.

- **Static hazards**: output momentarily transitions when isn't supposed to change.
- **Dynamic hazard**: output changes more than once when it's supposed to change once.

Name	Identity
Distribution	$a \cdot (b + c + \cdots) = a \cdot b + a \cdot c + \cdots$ $a + (b \cdot c \cdots) = (a + b) \cdot (a + c) \cdots$
Absorption	$a + a \cdot b = a$ $a \cdot (a + b) = a$
Consensus	$a \cdot b + \overline{a} \cdot c + b \cdot c = a \cdot b + \overline{a} \cdot c$ $(a + b) \cdot (\overline{a} + c) \cdot (b + c) = (a + b) \cdot (\overline{a} + c)$
DeMorgan's	$\overline{a + b + c + \cdots} = \overline{a} \cdot \overline{b} \cdot \overline{c} \cdot \cdots$ $\overline{a \cdot b \cdot c \cdot \cdots} = \overline{a} + \overline{b} + \overline{c} + \cdots$

Logic minification with **K-maps** and the **QM-method**.

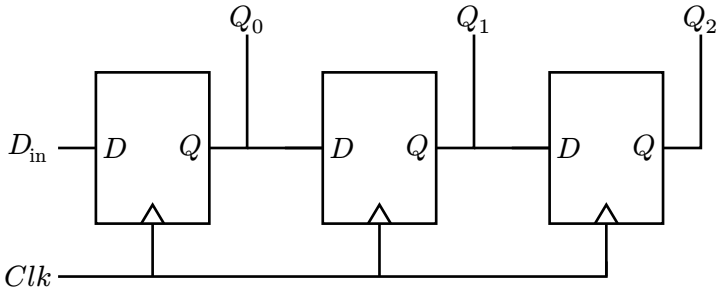
1. List all minterms and don't care terms.
2. Merge terms: tick them and write on the next column.
3. Select the minimum covering set of prime implicants.

Sequential Logic

Sequential logic depends on current input and previous state.

- The **ripple counter** is not synchrnous, propagation delay build up, limiting maximum clock speed before miscounting happens. We used synchrnous counters in lab.
- Counters are used for counting, producing a delay, generating sequences, dividing frequences.

Shift Registers



- It is a synchrnous machine because all FFs are connected to the same Clk.
- Q_n is delayed by n clock cycles.

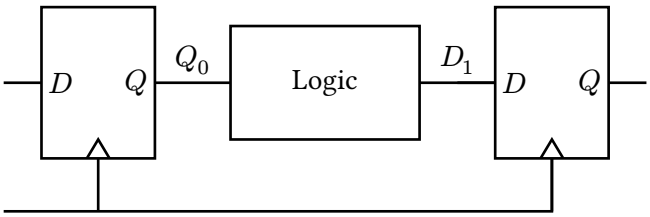
Used as a **serial data link**:

1. Parallel data in
2. Pass through a wire as serial data
3. Parallel data out

Timing Constraints for Asynchronous Input

T_c clock period is the time between rising edges.

- t_{pc} time after Clk when Q_0 changes
- t_{pd} time after Q_0 when D_1 changes
- t_{su} setup time for the right FF, D_1 needs to settle t_{su} before the next rising edge
- t_{skew} is the range of time Clk reaching all FFs



Requires $T_c \geq \max\left(t_{pc} + t_{pd} + t_{su} + t_{\text{skew}}\right)$

- t_{hold} minimum hold time for the right FF, D_1 cannot update for t_{hold} after Clk

Requires $\min\left(t_{pc} + t_{pd} + t_{\text{skew}}\right) \geq t_{\text{hold}}$

If violated, Q will remain in a **metastable state** until it resolves to a valid state.

$$P(t_{\text{res}} > t) = \frac{T_0}{T_c} \exp\left(-\frac{t}{\tau}\right)$$ where T_0 and τ are characteristic of the FF.

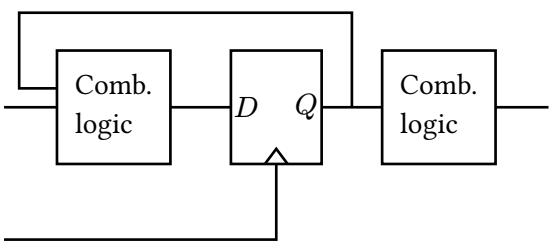
- $P_{\text{fail}} = P(t_{\text{res}} > T_c - t_{su})$ is the probability a single FF fails to resolve before the next clock edge.
- $(P_{\text{fail}})^n$ is the probability for a **synchroniser** of n cascaded FFs to fail to resolve to a valid state.

If input D_0 changes N times per second, the probability of failure is $t_{su}/T_c \times NP_{\text{fail}}$ per second.

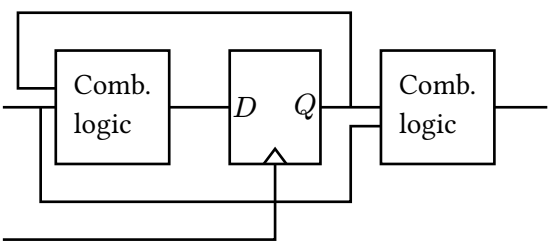
$$MTBF = \frac{1}{t_{su}/T_c \times NP_{\text{fail}}}$$

Finite State Machines

Moore machine's output only depends state.



Mealy machine's also directly depend on input.



State assignment is chosen based on what we are trying to optimise: speed or complexity (FFs used).

Sequential State Assisngment

abc	$a'b'c'$
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	100

Sliding State Assignment

abc	$a'b'c'$
000	001
001	011
011	110
110	100
100	000

Shift Register Assignment

$abcde$	$a'b'c'd'e'$
00011	00110
00110	01100
01100	11000
10001	00011

One-hot State Encoding

$abcde$	$a'b'c'd'e'$
00001	00010
00010	00100
00100	01000
00001	00001

State p and q are equivalent if they produce the same bit sequence for the same input sequence.

$$p \equiv q \iff \lambda(p,x) \equiv \lambda(q,x) \land \delta(p,x) \equiv \delta(q,x)$$

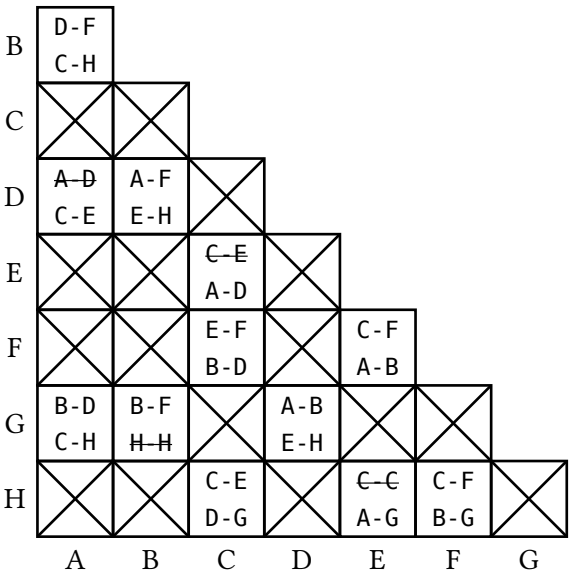
- λ is the output function
- δ is the next state function

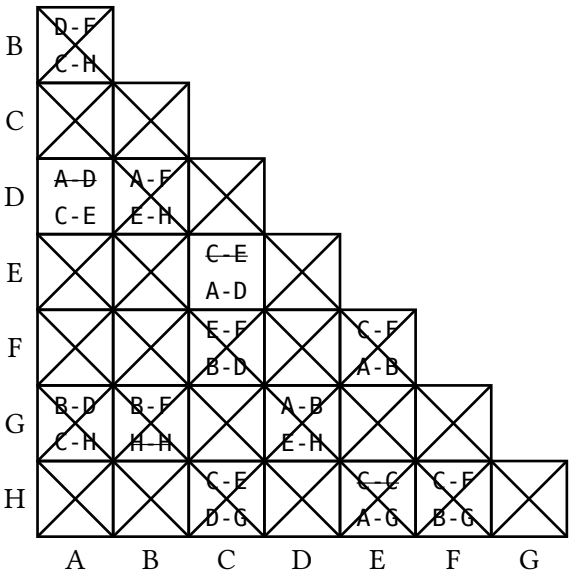
Current state	X=0	X=1	Output
A	D	C	0
B	F	H	0
C	E	D	1
D	A	E	0
E	C	A	1
F	F	B	1
G	B	H	0
H	C	G	1

We can eliminate identical states with **row matching**.

1. Draw the implication table.
2. *(Left)* Cross out states that are not equivalent.
3. *(Right)* The cells not crossed out represents equivalent states.

In example below, $A \equiv D$ and $C \equiv E$

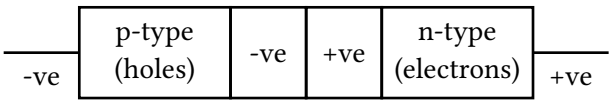




Electricity

Name	Statement
Ohm's law	$V = IR$
Kirchoff's current law	Sum of current entering a junction is zero
Kirchoff's voltage law	In any closed loop the sum of all voltages is zero.

- **N-type silicon** has extra electrons.
- **p-type silicon** has holes.



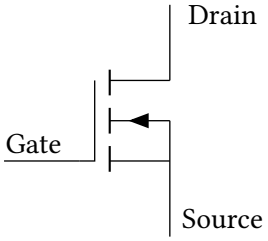
A **P-N junction** is a diode.

- When connected with forward bias, the depleted region shrinks so current flows.
- Reverse bias then depleted region grows.

$$\text{logic 0 noise margin} = \max(V_{\text{input low}}) - \max(V_{\text{output low}})$$

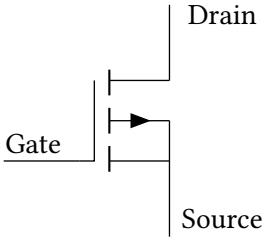
$$\text{logic 1 noise margin} = \min(V_{\text{output high}}) - \min(V_{\text{input high}})$$

N-Channel MOSFET



Location	Voltage
Body	0V
Source	0V
Drain	$+V_D$
Gate (off)	0V
Gate (on)	$+V_G$

P-Channel MOSFET



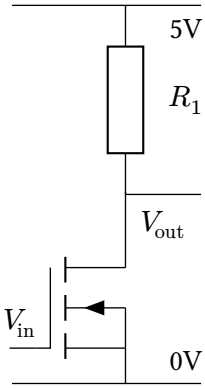
Location	Voltage
Body	$+V_D$
Source	$+V_D$
Drain	0V
Gate (off)	$+V_G$
Gate (on)	0V

Resistance of the transistor changes non-linearly as gate voltage changes.

N-MOS Inverter

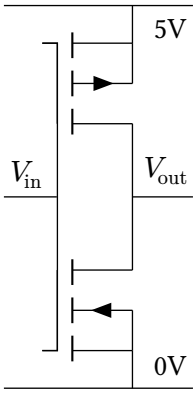
- Slow transistion
- High power consumption

You can find the V_{in} to V_{out} graph using graphical methods.

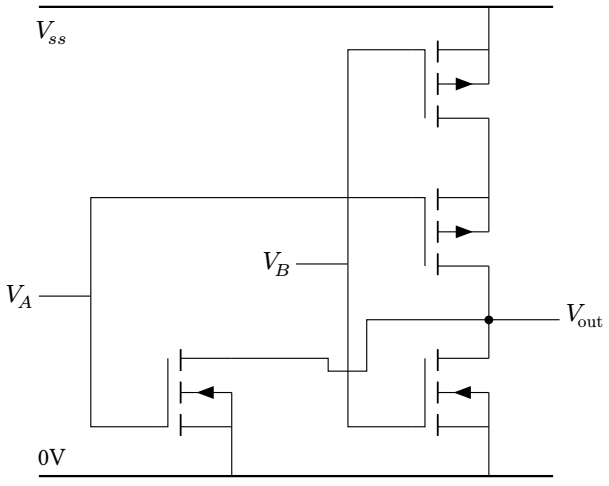


CMOS Inverter

- Much sharper transition
- Current flows briefly only when the input changes.



CMOS NOR Gate



CMOS NAND Gate