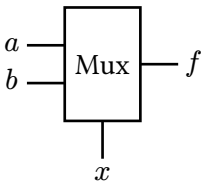
Digital Electronics

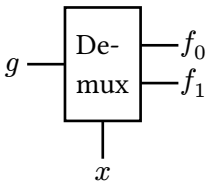
Components

2-to-1 Selector (Multiplexer)



a	b	x	f
X	b	0	b
a	X	0	a

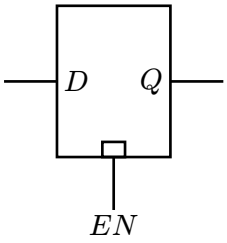
Demultiplexer



g	x	f_0	f_1
g	0	g	0
g	1	0	g

A **decoder** is a demux with g set to 1.

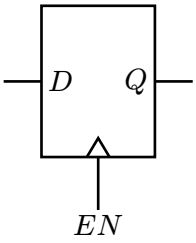
Level-triggered D Flip-flop



A 1 input version of the RS-latch.

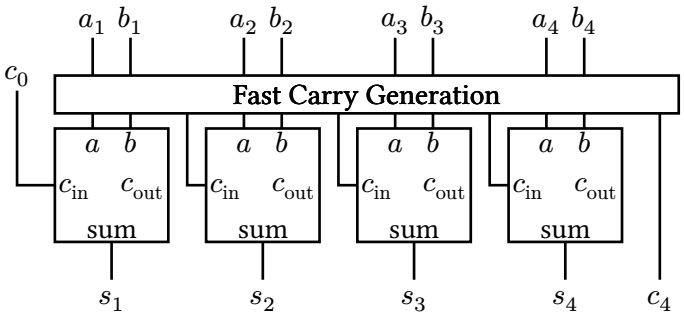
- $EN = 1$ then $Q = D$
- $EN = 0$ then Q unchanged.

Edge-triggered D Flip-flop



Output changes only on a rising edge.

In addition, there are the **programmable logic array** and **ROM**. Multiple memory devices can be connected to the same bus with **tristate buffers** which disconnects from the bus when not selected.



c_{in}	a	b	c_{out}
?	0	0	0
?	0	1	?
?	1	0	?
?	1	1	1

The level of c_4 is reduced $8 \to 5$

Combinatory Logic

Combinatory output depends only on current input.

- **Disjunctive normal form** (sum of product) is the sum minterms.
- **Conjunctive normal form** (product of sum) is the product of maxterms.

Hazards are brief changes in output, multilevel logic can introduce hazards.

- **Static hazards**: output momentarily transitions when isn't supposed to change.
- **Dynamic hazard**: output changes more than once when it's supposed to change once.

Name	Identity
Distribution	$a \cdot (b + c + \cdots) = a \cdot b + a \cdot c + \cdots$ $a + (b \cdot c \cdot \cdots) = (a + b) \cdot (a + c) \cdot \cdots$
Absorption	$a + a \cdot b = a$ $a \cdot (a + b) = a$
Consensus	$a \cdot b + \overline{a} \cdot c + b \cdot c = a \cdot b + \overline{a} \cdot c$ $(a + b) \cdot (\overline{a} + c) \cdot (b + c) = (a + b) \cdot (\overline{a} + c)$
DeMorgan's	$\overline{a + b + c + \cdots} = \overline{a} \cdot \overline{b} \cdot \overline{c} \cdot \cdots$ $\overline{a \cdot b \cdot c \cdot \cdots} = \overline{a} + \overline{b} + \overline{c} + \cdots$

Logic minification with **K-maps** and the **QM-method**.

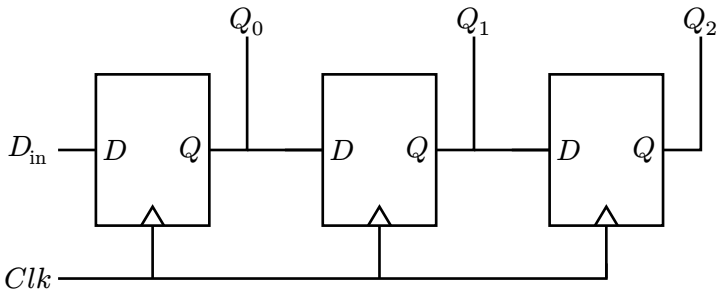
1. List all minterms and don't care terms.
2. Merge terms: tick them and write on the next column.
3. Select the minimum covering set of prime implicants.

Sequential Logic

Sequential logic depends on current input and previous state.

- The **ripple counter** is not synchrnous, propagation delay build up, limiting maximum clock speed before miscounting happens. We used synchrnous counters in lab.
- Counters are used for counting, producing a delay, generating sequences, dividing frequences.

Shift Registers



- It is a synchrnous machine because all FFs are connected to the same Clk.
- Q_n is delayed by n clock cycles.

Used as a **serial data link**:

1. Parallel data in
2. Pass through a wire as serial data
3. Parallel data out

System Timing