2020 Digital IC Design Homework 1: 4-bit binary adder-subtractor

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	25700 (ns)

(your

```
#         508 data is correct
#         509 data is correct
#         510 data is correct
#         511 data is correct
#         512 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : C:/Users/harry/2020ICHW/HW1/AS_tb.v(63)
#    Time: 25700 ns  Iteration: 0  Instance: /AS_tb
# 1
# Break at C:/Users/harry/2020ICHW/HW1/AS_tb.v line 63
```

pre-sim result)

Transcript

```
#         508 data is correct
#         509 data is correct
#         510 data is correct
#         511 data is correct
#         512 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : C:/Users/harry/2020ICHW/HW1/AS_tb.v(63)
#    Time: 25700 ns  Iteration: 0  Instance: /AS_tb
# 1
# Break in Module AS_tb at C:/Users/harry/2020ICHW/HW1/AS_tb.v line 63

VSIM 3>
```

(your post-sim result)

Synthesis Result

Total logic elements	9
Total memory bit	0
Embedded multiplier 9-bit element	0

Flow Status	Successful - Thu Apr 09 21:48:56 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	AS
Top-level Entity Name	AS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	9 / 68,416 (< 1 %)
Total combinational functions	9 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	15 / 622 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

根據投影片的內容，利用邏輯閘及接線的方式稍作修改，就可做完這次作業

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*