2020 Digital IC Design

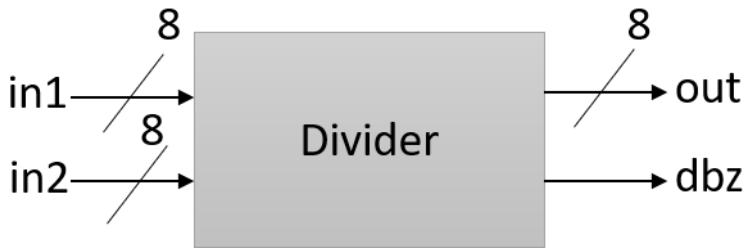
Homework 2: Divider

1. Introduction

The divider is a device that can be used to perform division. It can be usually classified into the signed divider or unsigned divider. Please implement an 8-bit unsigned divider. Any method of implementation is available, but you can not use Verilog build-in divider directly. As you encounter divided-by-zero, you need to set the signal dbz as 1.

2. Design Specifications

2.1 Block Overview



2.2 I/O Interface

Signal Name	I/O	width	Description
in1	Input	8	Dividend
in2	Input	8	Divisor
out	Output	8	
dbz	Output	1	You need to set as 1 when you encounter divided-by-zero.

2.3 File Description

File Name	Description
div.v	RTL code implemented by Verilog
div_tb.v	Test bench for verifying design
cycloneii_atoms.v	Simulation library for gate-level simulation

3. Scoring

3.1 Functional Simulation (pre-sim) [70%]

All of the results should be generated correctly, and then you will get the following message in ModelSim simulation.

```
#       65524 data is correct
#       65525 data is correct
#       65526 data is correct
#       65527 data is correct
#       65528 data is correct
#       65529 data is correct
#       65530 data is correct
#       65531 data is correct
#       65532 data is correct
#       65533 data is correct
#       65534 data is correct
#       65535 data is correct
#       65536 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module div_tb at E:/DIC_HW/DIC_HW2/div_tb.v line 62
```

3.2 Gate-Level Simulation (post-sim) [30%]

3.2.1 Synthesis

Your code should be synthesizable. After synthesizing with Quartus, the file named div.vo will be obtained.

Flow Summary

Flow Status	Successful - Tue Mar 10 10:26:01 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	div
Top-level Entity Name	div
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	104 / 68,416 (< 1 %)
Total combinational functions	104 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	25 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Device : Cyclone II EP2C70F896C8

3.2.2 Simulation

All of the results should be generated correctly using div.vo, and you will get the following message in ModelSim simulation.

```
#       65523 data is correct
#       65524 data is correct
#       65525 data is correct
#       65526 data is correct
#       65527 data is correct
#       65528 data is correct
#       65529 data is correct
#       65530 data is correct
#       65531 data is correct
#       65532 data is correct
#       65533 data is correct
#       65534 data is correct
#       65535 data is correct
#       65536 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module div_tb at E:/DIC_HW/DIC_HW2/div_tb.v line 62
```

3.3 Performance [0 %]

The performance is scored by the logic elements you used and the simulation time in post-sim. The scoring equation is (Total logic elements + total memory bit+ 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns). (The smaller the better).

3.4 Note

You can modify the clock cycle in div_tb when post-sim.

```
`timescale 1ns / 10ps
`define CYCLE 100 // can be modified
module div_tb;
parameter width = 8;
```

4 Submission

4.1 Submitted files

You should classified your files into three directories and compressed to .zip format. The naming rule is HW2_studentID_name.zip.

	RTL category
*.v	All of your Verilog RTL code
	Gate-Level category
*.vo	Gate-Level netlist generated by Quartus

*.sdo	SDF timing information generated by Quartus
	Documentary category
*.pdf	The report file of your design (in pdf).

4.2 Report file

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible, and the flow summary result and minimum CYCLE in post-sim are necessary.

4.3 Please submit your .zip file to folder HW2 in the moodle.

Deadline: 2020-04-14 23:55

5 If you have any problem, please contact by the TA by email :

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