2020 Digital IC Design Homework 3: Approximate Average

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	272544 (ns)

(your pre-sim result)

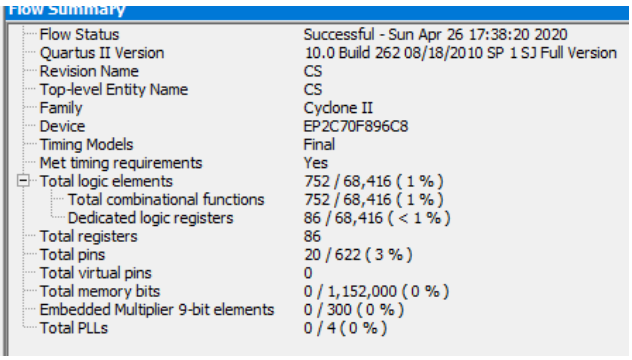
```
#
# All data have been generated success
#
# --------------------PASS-------------
#
# ------------------------------------
#
# ** Note: $finish    : C:/Users/harry
#    Time: 272544 ns  Iteration: 2  In
# 1
```

(your post-sim result)

```
#
# All data have been generated succe
#
# --------------------PASS-----------
#
# ------------------------------------
#
# ** Note: $finish    : C:/Users/har
#    Time: 272544 ns  Iteration: 2
# 1
```

Synthesis Result

Total logic elements	752
Total memory bit	0
Embedded multiplier 9-bit element	0



Flow Summary	
Flow Status	Successful - Sun Apr 26 17:38:20 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	CS
Top-level Entity Name	CS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	752 / 68,416 (1 %)
Total combinational functions	752 / 68,416 (1 %)
Dedicated logic registers	86 / 68,416 (< 1 %)
Total registers	86
Total pins	20 / 622 (3 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

目前只有想到以迴圈的方式來找到 closely value，但整體速度很慢，相要加 clock 調到 130 左右才能 all pass.

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*