

2020 Digital IC Design Homework 5: Sobel

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Simulation Result					
Functional simulation	PASS	Gate-level simulation	PASS	Gate-level simulation time	19660971604 (ps)
<pre># ----- S U M M A R Y ----- # # Congratulations! Sobel X data have been generated successfully # Congratulations! Sobel Y data have been generated successfully # Congratulations! Sobel combine data have been generated successfully # # ----- # # ** Note: \$finish : C:/Users/harry/2020ICHW/HW5/testbench # Time: 19660962500 ps Iteration: 0 Instance: /testbench # 1</pre>				<div>(your post-sim result)</div> <pre># ----- S U M M A R Y ----- # # Congratulations! Sobel X data have been generated successfully # Congratulations! Sobel Y data have been generated successfully # Congratulations! Sobel combine data have been generated successfully # # ----- # # ** Note: \$finish : C:/Users/harry/2020ICHW/HW5/testbench # Time: 19660971604 ps Iteration: 0 Instance: /testbench # 1</pre>	
Synthesis Result					
Total logic elements			1238		
Total memory bit			0		
Embedded multiplier 9-bit element			0		
<div><div><div>Flow Status</div><div>Successful - Thu Jun 18 02:18:23 2020</div></div><div><div>Quartus II Version</div><div>10.0 Build 262 08/18/2010 SP 1 SJ Full Version</div></div><div><div>Revision Name</div><div>SOBEL</div></div><div><div>Top-level Entity Name</div><div>SOBEL</div></div><div><div>Family</div><div>Cyclone II</div></div><div><div>Device</div><div>EP2C70F896C8</div></div><div><div>Timing Models</div><div>Final</div></div><div><div>Met timing requirements</div><div>N/A</div></div><div><div><div>Total logic elements</div><div>1,238 / 68,416 (2 %)</div></div><div><div>Total combinational functions</div><div>1,198 / 68,416 (2 %)</div></div><div><div>Dedicated logic registers</div><div>202 / 68,416 (< 1 %)</div></div><div><div>Total registers</div><div>202</div></div><div><div>Total pins</div><div>81 / 622 (13 %)</div></div><div><div>Total virtual pins</div><div>0</div></div><div><div>Total memory bits</div><div>0 / 1,152,000 (0 %)</div></div><div><div>Embedded Multiplier 9-bit elements</div><div>0 / 300 (0 %)</div></div><div><div>Total PLLs</div><div>0 / 4 (0 %)</div></div></div></div>					
Description of your design					

這次作業讓我學會如何讀寫 MEMORY，花了我非常多的時間

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*