2020 Digital IC Design

Homework 1: 4-bit binary adder-subtractor

1. Introduction

The binary adder-subtractor is a device that is capable of adding or subtracting elements. The following is a circuit which is used to add or subtract, depending on the control signal. Please implement a 4-bit binary adder-subtractor, the inputs adopts 2-complement expression.

2. Design Specifications:

2.1 Block Overview

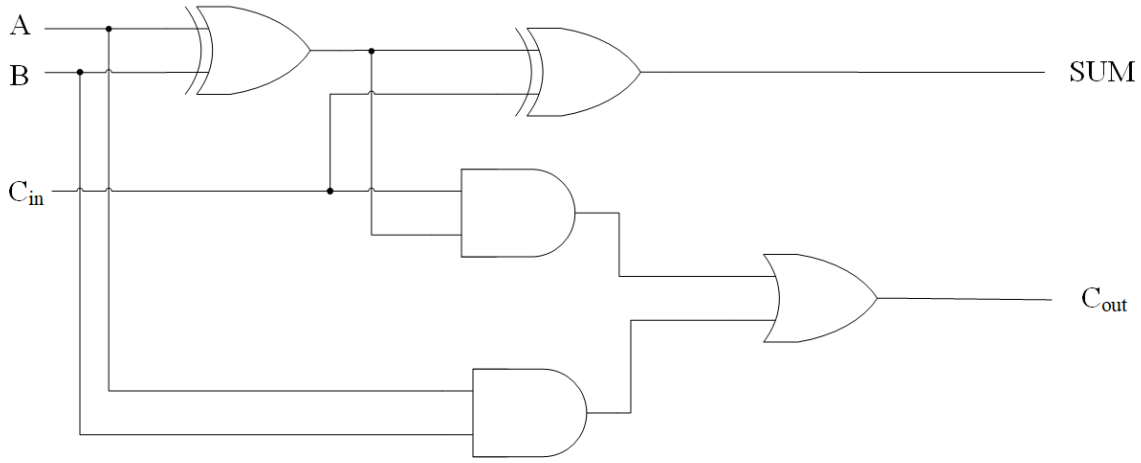


Fig 1. Full adder

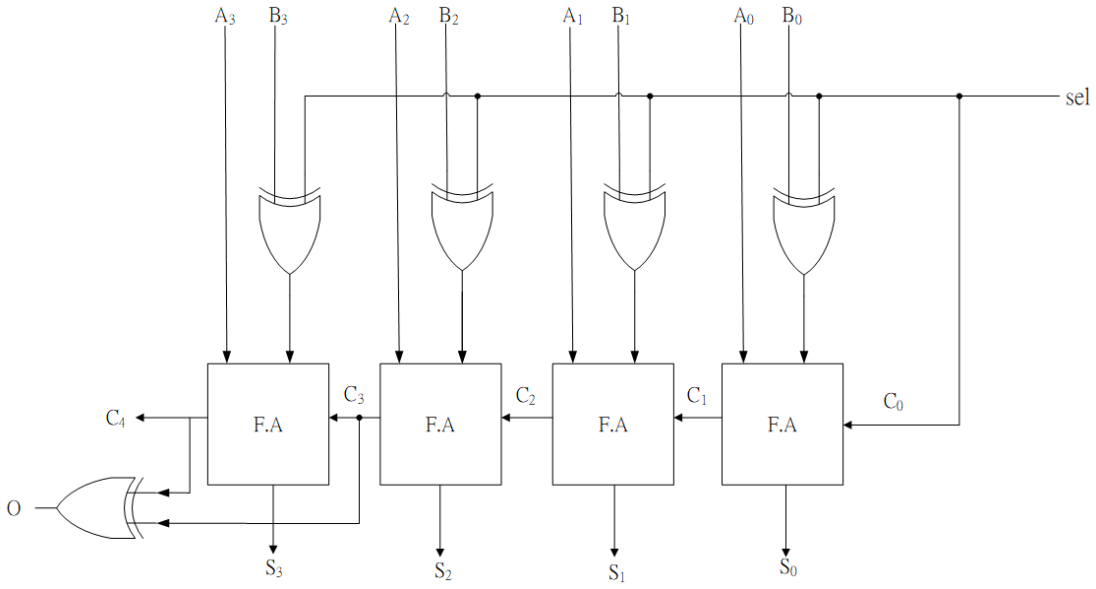


Fig 2. 4-bit binary adder-subtractor

2.2 I/O Interface

Signal Name	I/O	width	Description
sel	input	1	When sel=1, the circuit is a subtractor and when sel=0, the circuit becomes adder.
A	input	4	
B	input	4	
S	output	4	
O	output	1	Overflow

2.3 File Description

File Name	Description
AS.v	RTL code for using Verilog
AS_tb.v	Test bench for verifying design
cycloneii_atoms.v	Simulation library for gate-level simulation

2.4 Requirement

Please use dataflow description or structure description to design 4-bit binary adder-subtractor.

3. Scoring

3.1 Functional Simulation (pre-sim) [70%]

All of the results should be generated correctly. If all of the results are correct, you will get the following message in ModelSim simulation.

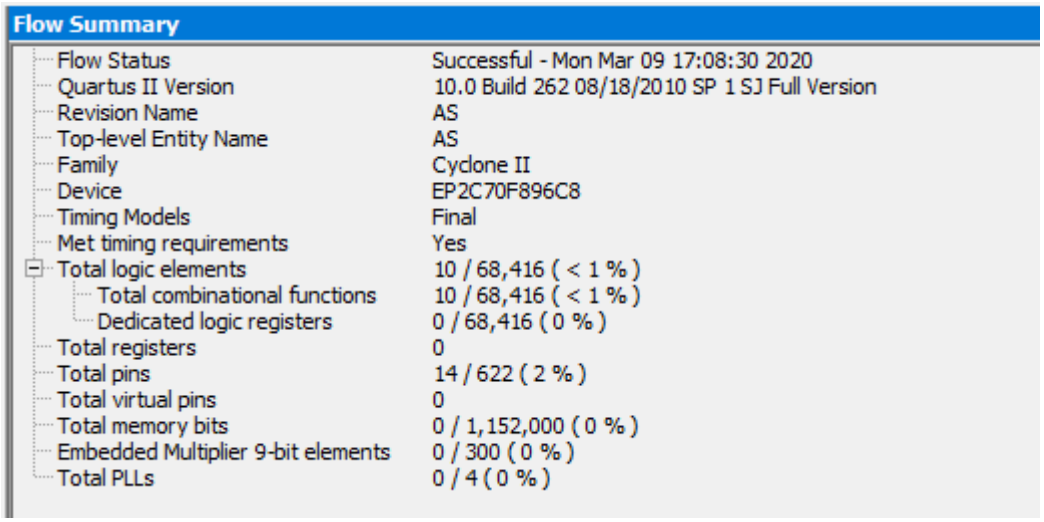
```
#          504 data is correct
#          505 data is correct
#          506 data is correct
#          507 data is correct
#          508 data is correct
#          509 data is correct
#          510 data is correct
#          511 data is correct
#          512 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module AS_tb at E:/DIC_HW/DIC_HW1/AS_tb.v line 63

VSIM 43>
```

3.2 Gate-Level Simulation (post-sim) [30%]

3.2.1 Synthesis

Your code should be synthesizable. After synthesizing with

Quartus, a file named AS.vo will be obtained.



Flow Summary	
Flow Status	Successful - Mon Mar 09 17:08:30 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	AS
Top-level Entity Name	AS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	10 / 68,416 (< 1 %)
Total combinational functions	10 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	14 / 622 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Device : Cyclone II EP2C70F896C8

3.2.2 Simulation

All of the results should be generated correctly by using AS.vo, and you will get the following message in ModelSim simulation.

```
#          503 data is correct
#          504 data is correct
#          505 data is correct
#          506 data is correct
#          507 data is correct
#          508 data is correct
#          509 data is correct
#          510 data is correct
#          511 data is correct
#          512 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module AS_tb at E:/DIC_HW/DIC_HW1/AS_tb.v line 63
```

3.3 Performance [0 %]

The performance is scored by the logic elements you used and the simulation time in post-sim. The scoring equation is (Total logic elements + total memory bit+ 9*embedded multiplier 9-bit element) × (longest gate-level simulation time with *ns*). (The smaller the better).

3.4 Note

You can modify clock cycle in the file named AS_tb in post-sim.

```
`timescale 10ns / 1ps
`define CYCLE 5
`define A_dat "./A.txt"
`define B_dat "./B.txt"
`define O_dat "./O.txt"
`define SUM_dat "./SUM.txt"
module AS_tb;
```

4. Submission

4.1 Submitted files

You should classify your files into three directories and compressed to .zip format. The naming rule is HW1_studentID_name.zip.

	RTL category
*.v	All of your Verilog RTL code
	Gate-Level category
*.vo	Gate-Level netlist generated by Quartus
*.sdo	SDF timing information generated by Quartus
	Documentary category
*.pdf	The report file of your design (in pdf).

4.2 Report file

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible, and the summary results and minimum CYCLE in post-sim are necessary.

4.3 Please submit your .zip file to folder HW1 in the moodle.

Deadline: 2020-04-14 23:55

5. If you have any problem, please contact by the TA by email :

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