2020 Digital IC Design Homework 5: Sobel

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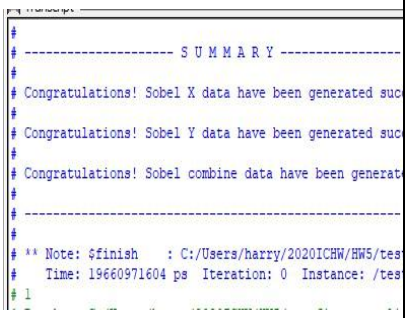
Simulation Result

Functional simulation	PASS	Gate-level simulation	PASS	Gate-level simulation time	19660971604 (ps)

```
#
# ---------------------- S U M M A R Y -----------------
#
# Congratulations! Sobel X data have been generated succ
#
# Congratulations! Sobel Y data have been generated succ
#
# Congratulations! Sobel combine data have been generate
#
# ------------------------------------------------------
#
# ** Note: $finish    : C:/Users/harry/2020ICHW/HW5/test
#    Time: 19660962500 ps  Iteration: 0  Instance: /test
# 1
```

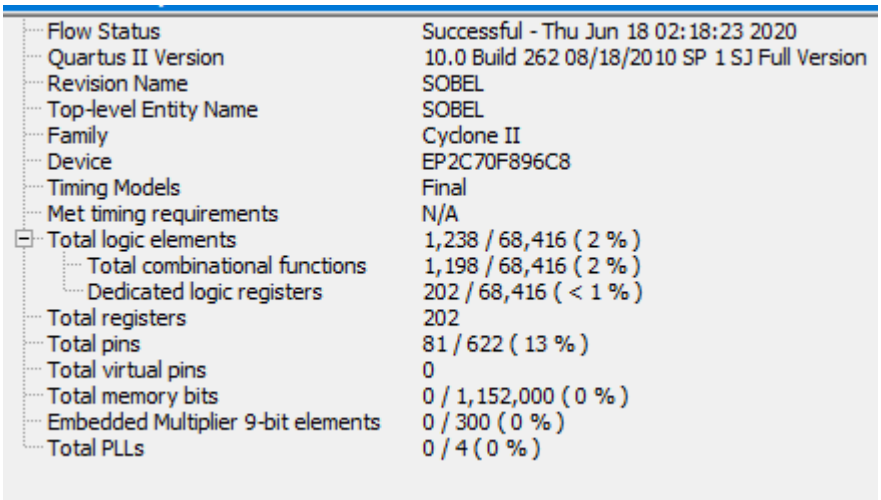
(your post-sim



result)

Synthesis Result

Total logic elements	1238
Total memory bit	0
Embedded multiplier 9-bit element	0



Description of your design

這次作業讓我學會如何讀寫 MEMORY，花了我非常多的時間

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*