2020 Digital IC Design Homework 2: Divider

NAME	范皓翔
Student ID	P76081263

Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	6553610 (ns)

```
#       65532 data is correct
#       65533 data is correct
#       65534 data is correct
#       65535 data is correct
#       65536 data is correct
# ------------------PASS------------------
# All data have been generated successfully!
# ** Note: $finish    : C:/Users/harry/2020ICHW/HW2/div_tb.v(62)
#    Time: 6553610 ns  Iteration: 0  Instance: /div_tb
# 1
# Break at C:/Users/harry/2020ICHW/HW2/div_tb.v line 62
```

(your pre-sim result)

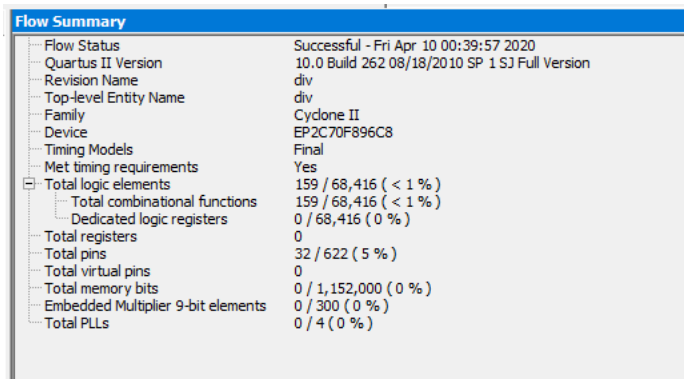
(your po

```
#       65532 data is correct
#       65533 data is correct
#       65534 data is correct
#       65535 data is correct
#       65536 data is correct
# ------------------PASS------------------
# All data have been generated successfully!
# ** Note: $finish    : C:/Users/harry/2020ICHW/HW2/div_tb.v(62)
#    Time: 6553610 ns  Iteration: 0  Instance: /div_tb
# 1
# Break in Module div_tb at C:/Users/harry/2020ICHW/HW2/div_tb.v
```

st-sim result)

Synthesis Result

Total logic elements	159
Total memory bit	0
Embedded multiplier 9-bit element	0



Flow Summary	
Flow Status	Successful - Fri Apr 10 00:39:57 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	div
Top-level Entity Name	div
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	159 / 68,416 (< 1 %)
Total combinational functions	159 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	32 / 622 (5 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

利用以前學過的計組除法器概念，首先比較除數和餘數的大小，除數比較大時向左 shift，且最右邊補 1.

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*