2020 Digital IC Design Homework 1: 4-bit binary adder-subtractor

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| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | | | Gate-level simulation time | 25700 (ns) |
| (your pre-sim result) | | | | | | (your post-sim result) | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 9 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 0 | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 根據投影片的內容，利用邏輯閘及接線的方式稍作修改，就可做完這次作業 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (gate-level simulation time in ns)*