2020 Digital IC Design Homework 2: Divider

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| NAME | | 范皓翔 | | | | | | |
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| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | Pass | | | Gate-level simulation time | 6553610 (ns) |
| (your pre-sim result) | | | | | | (your post-sim result) | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 159 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 0 | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 利用以前學過的計組除法器概念，首先比較除數和餘數的大小，除數比較大時向左shift，且最右邊補1. | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (gate-level simulation time in ns)*