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FPGA-based Spectrum Analyzer with High Area Efficiency by Goertzel Algorithm

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Abstract

FFT algorithm is the popular software design for spectrum analyzer, but doesn't work well for parallel hardware system due to complex calculation and huge memory requirement. Observing the key components of a spectrum analyzer are the intensities for respective frequencies, we propose a Goertzel algorithm to directly extract the intensity factors for respective frequency components in the input signal. Goertzel algorithm dispenses with the memory for z-1 and z-2 processing, and only needs two multipliers and three adders for real number calculation. In this paper, we present the spectrum extraction algorithm and implement a spectrum extractor with high speed and low area consumption in a FPGA (Field Programmable Gate Array) chip. It proves the feasibility of implementing a handheld concurrent multi-channel real-time spectrum analysis IP into a low gate counts and low power consumption CPLD (Complex Programmable Logic Device)chip.

1. Introduction

There three kinds of design architectures for the real-time frequency spectrum analysis: scan-based architecture, real-time FFT(Fast Fourier Transformation)-based architecture, and Scanning-FFT mixed architecture) [1-5]. All have their advantages and disadvantage. Current studies on real-time frequency spectrum analysis are focused on algorithm speed (less than 10µs) and hardware consumption. To reduce hardware requirement, most FFT algorithms are software-based. But the speed requirement of real-time frequency spectrum analysis needs real-time FFT processor. Hardware-based FFT processor implies huge multiplier/accumulator (MAC) units and storage memory, which cost much power and occupy large chip area. Therefore, it is not suitable for hand-held real-time frequency spectrum analyzer. To speed up, many FPGA-based FFT processor adopts high gate count FPGA and its high speed SRAM, for example Xilinx Virtex II chip. All digital concurrent multi-channel scan-based architecture may be the possible solution to achieve high speed and low chip area. The required hardware includes local oscillator and high Q band pass filter. To achieve rather narrow pass-band, a high Q band pass filter is usually more than 500-taped. The hardware consumption is still expensive and the procession speed is reduced. In the following section, we propose the Goertzel algorithm to replace the traditional FIR (Finite Impulse Response) band-pass filter.

2. High area efficiency FPGA-based spectrum analyzer

Spectrum analysis for non-periodic signals commonly requires either on-line or off-line FFT processor. But FFT processor always consumes much MAC units and storage memory, and then suffers from large power dissipation and hardware resource. If we want to build up a real-time and on-line spectrum analysis algorithm in a FPGA chip, the power and hardware issues should be key factor for real system implementation. The possible design is the concurrent multi-channel scan-based architecture. The following section will introduce scan-based real-time spectrum analysis algorithm, and put Goertzel algorithm to replace the high Q pass-band filter which leads to most power and hardware resource.

2.1 Real-time sweep spectral extraction algorithm

The system function block of a real-time sweep spectral extractor is illustrated in Fig. 1 [6]. The mixer combines the input test signal and the reference signal from local oscillator. The output modulated signals have the sum frequency and difference frequency. The central frequency of the FIR band-pass filter is set at the difference frequency to let go the chosen frequency component.

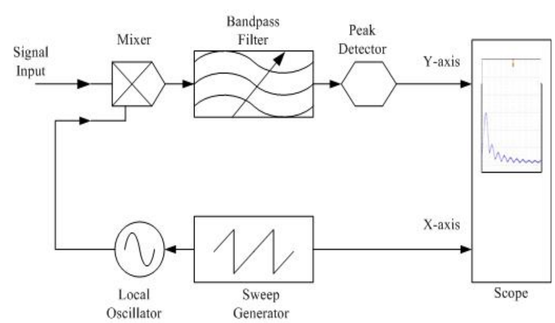

Figure 1. The system function block of a real-time sweep spectral extractor

The following peak detector will detect the signal intensity, and send it into to the X-Y scope. The sweep generator supports the X-axis signal, and pushes the local oscillator to generate the reference signal with the desired frequency. We adopt direct digital synthesis (DDS) technique to tune the reference signal. To meet the rather narrow bandwidth requirement, we need very high Q FIR band-pass filter. It implies hundreds of tap orders.

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2.2 Goertzel Algorithm[7,8]

The main function of both FIR filter and peak detector is to extract the amplitude component of the input. So we may adopt the Discrete Fourier Transform (DFT) to replace them, and directly pick up the amplitude of the specified frequency component. For length of N, the DFT series is:

$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^k \tag{1}$$

Where,

$$k = 0,1,..., N-1 \tag{2}$$

It needs N^2 complex multiplication and N(N-1) complex addition. For length of N, the Goertzel algorithm series is:

$$H_k(z) = \frac{1 - W_N^k z^{-1}}{1 - 2\cos(\frac{2\pi k}{N}) z^{-1} + z^{-2}} \tag{3}$$

Where,

$$k = 0,1,..., N-1 \tag{4}$$

Fig. 2 is the corresponding second order recursive calculation flow. Here, it is apparently that Goertzel algorithm only needs two real multiplications and three real additions to pick up the amplitude of the specified frequency component.

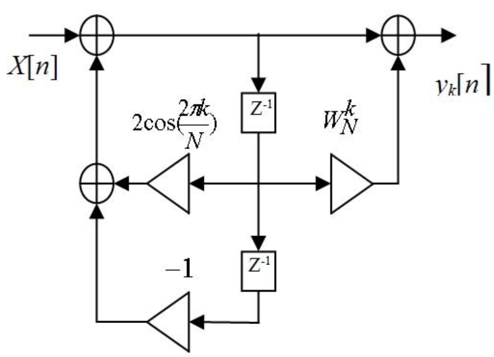

Figure 2. Calculation flow of the second-order recursive algorithm

Embedding Goertzel algorithm into the real-time sweep spectral extractor in Fig.1, we get the new system block with high chip area efficiency, shown as Fig.3. Conventionally, for high frequency resolution, we need narrow pass-band of FIR filter and consume too much chip area. Without pass-band narrowing, the Goertzel algorithm just calculates and extracts the amplitude of the specified frequency component. We can achieve better frequency solution without high chip area requirement.

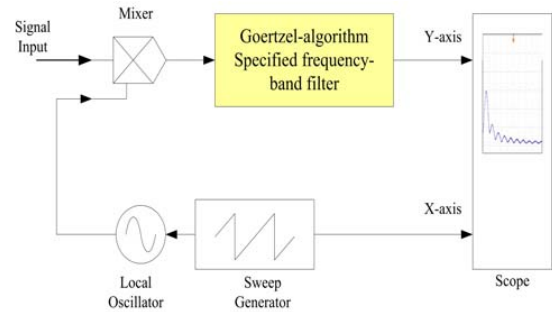

Figure 3. The system function block of a real-time sweep spectral extractor with Goertzel algorithm

3. System simulation and implementation

Here, we use the Matlab/Simulink to build up the desired function modules, shown as Fig. 4.. The Xilinx/System Generator modules are built in to simulate hardware in the loop.

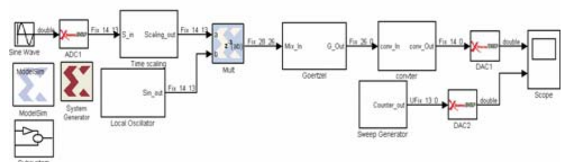

Figure 4. System block of FPGA-based spectrum sensing system with Goertzel algorithm

The Goertzel algorithm is arranged as a concurrent processing architecture, shown as Fig.7.

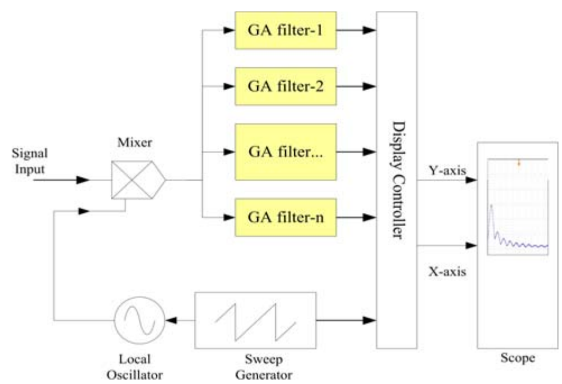

Figure 5. Concurrent processing architecture for sweep spectral extractor

Fig. 6 demonstrates the real-time input signal data access and frame buffering structure. We adopt time-frequency scaling theorem [9] to temporally adjust the frequency span of input signal to meet the specified frequency for Goertzel algorithm. The actual frequency will be recovered before being displayed.

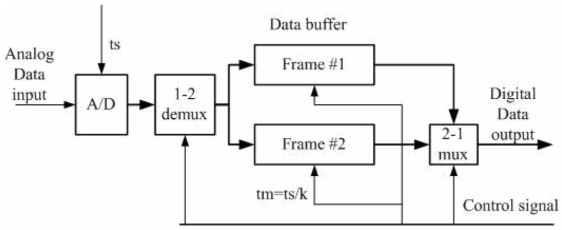

Figure 6. Flow charts for the de-multiplexing and multiplexing of the input data stream access and frame data buffering alternately

The target hardware platform is XtremeDSP development kit provided by Xilinx. It includes two ADC channels (AD6644： 14-bits up to 65 Mps), two DAC channels (AD9772A：14-bits up to 160 Mps), and Virtex-II XC2V3000-4FG676 FPGA chip. We set the 1 kHz frequency resolution of the Goertzel DFT, and analyze the incoming signal with frequencies from 1 kHz to 100 kHz. Fig. 7 is the output spectrum for periodic square wave with frequency of 4 kHz. We notice the odd order harmonics like 12 kHz, 20 kHz, and 28 kHz, of which relative amplitudes meet the Fourier transform prediction.

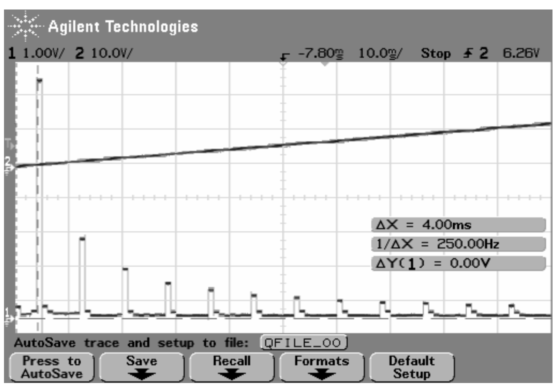

Figure 7. The output spectrum for periodic square wave with frequency of 4 kHz.

Taking 1 kHz of periodic square wave as the example, we compare the FPGA resource utilization for the real-time spectrum analyzer with FIR filter and Goertzel DFT approaches respectively. Table 1 tells that the flip-flops usage decreases from 79% down to 17%, and the LUT (look-up table) usage reduces from 53% down to 19%.

Table 1. Required resource comparison

Logic Utilization	With Goertzel DFT	with band-pass FIR
Number of Slice Flip Flops	17% (5,102 out of 28,672)	79% (22,890 out of 28,672)
Number of 4 input LUTs	19% (5,693 out of 28,672)	53% (15,270 out of 28,672)

4. Conclusions

We have demonstrated a FPGA-based spectrum analyzer with Goertzel DFT algorithm. This approach claims less chip area usage than FIR pass-band filter under the same frequency resolution. The VHDL (VHSIC Hardware Description Language) code can analyze real-time spectral frequency from 1 kHz to 10MHz with 1 kHz resolution. The time-frequency scaling theorem is used to upgrade the frequency resolution. This HDL-type digital IP can be embedded into most time-varying signal analyzer, especially for low cost/power handheld real time spectrum analysis for speech, music, biological signals, biomedical signals, impulse response of wireless channel, sonar acoustic waves, and environmental noises.

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