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Design of Digital Signal Spectrum Analyzer Based on FPGA

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***Abstract*—This paper presents a hardware software co-design of embedded digital spectrum analyzer. As a digital hardware design, it achieves better portability and modularity so that it could be easily deployed and embedded into other systems as a module and conduct arbitrary intermediate nodes spectrum monitoring with ease while such tasks are hard for traditional spectrum analysis instruments to accomplish since most of them only provide limited user interface. Besides, this design implements functions of real-time signal analysis and real-time spectrum display with VGA port, which traditional embedded data observation systems, for example SignalTap II Logic Analyzer, do not have. Furthermore, this design serves as a sample of hardware software co-design of soft-core processor based system, which can be used for reference.**

Keywords—Spectrum analyzer; FPGA; SOPC; Nios II; FFT

I. INTRODUCTION

Spectrum analyzer is a kind of instrument which analyses signal spectrum to provide its frequency-domain feature that is widely used in military, satellite communications, radio monitoring and other fields. In recent years, the popularity of digital devices sparked a new revolution in the field of electronics, and as a result, the spectrum analyzer design also evolved from conventional analog type to digital type. Among the digital systems, field-programmable gate array (FPGA), has advantages of design flexibility, high speed, ease of modification, low power consumption, which results in its widespread usage.

There are basically two kinds of methods to observe digital spectrum. The first approach is using the digital spectrum analysis instrument, which only provides limited user interface and not suitable for analyzing system's internal signal. Another approach is collecting spectrum data from the embedded logic analyzer of FPGA or printing spectrum data to personal computer (PC) through the soft-core processor and then plotting the spectrum with MATLAB. The second approach makes it possible for users to assign internal nodes in the system and monitor the spectrum of them while it is inefficient and incapable of real-time spectrum analysis. To solve these problems, this paper proposes a method of embedded digital spectrum analysis, which not only can analyze signals and display spectrum in real-time with the help of the fast Fourier transform (FFT) IP core, but also is so portable that it can be easily migrated to other systems to monitor spectrum of intermediate nodes. In conclusion, this design has advantages of real-time, stability, high reusability and simple peripheral circuit.

II. SYSTEM OVERVIEW

A. Overall system Scheme

Based on different approaches of signal analysis, there are two kinds of spectrum analyzer implementation schemes, based on the discrete Fourier transform (DFT) of modern digital signal processing technology or based on the frequency sweep tuning method, which belongs to traditional heterodyne signal processing technology. This design chooses the former approach for the ease of implementing DFT based on digital devices.

B. System Top-Level Structure

This design mainly consists of three parts: the signal source for test, FPGA board and video graphics array (VGA) display as is shown in Fig. 1. The major function of this system is analyzing input signals and then displaying their spectrum and energy progress. Besides, this design provides two kinds of different source signal modes and different FFT processing modes, as is shown in TABLE I. .

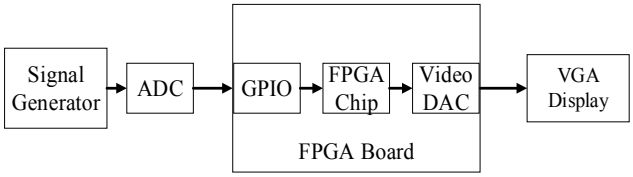

Fig. 1. System Block Diagram

TABLE I. SYSTEM OPTION

Mode	Description
External signal mode	Choose external signals through the ADC circuit to test.
Internal signal mode	Choose internal signals from DDS to test.
CFFT mode	Use FFT algorithm in Nios II to perform FFT.
FFT IP core mode	Use FFT IP core to perform FFT.
DDS frequency adjust	Range:0.5M-5MHz; stepper:0.5MHz

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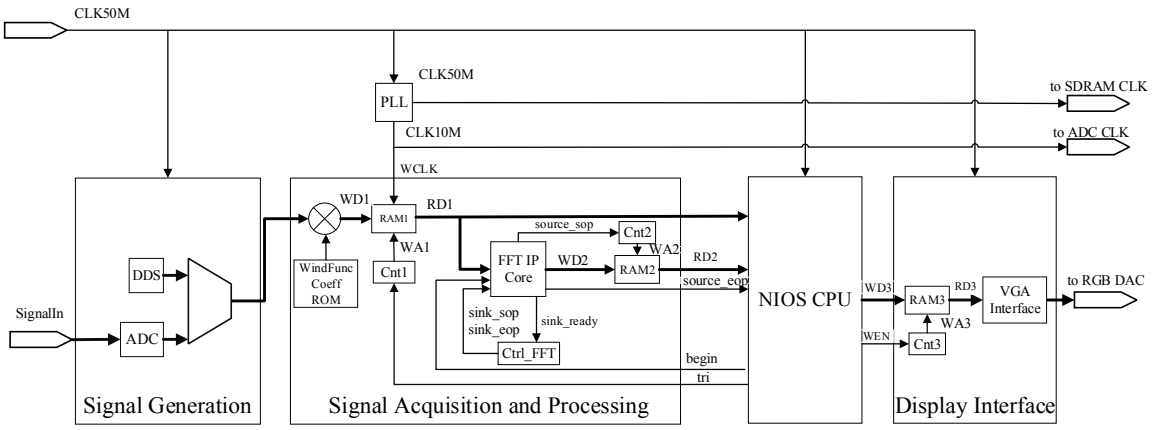

Fig. 2. System Hardware Block Diagram

III. System Hardware Design

The system hardware design includes four modules: signal generation, signal acquisition and analysis, Nios II processor and interface.

Signal generation module: According to test signal mode selection, this module selects output data from analog-to-digital converter (ADC) or sinusoidal signals from direct digital synthesizer (DDS) module within the system as system signal source.

Signal acquisition and analysis: Firstly this module collects data with sampling rate of 10MHz and then applies window function on input data. Here the Hanning window is chosen in order to make tradeoffs between main lobe width and side lobe attenuation. After that, the time-windowing signal is sent to FFT IP core. The key to control FFT IP core work correctly is proper configuration of the signal sink_sop, sink_eop and sink_valid. Both finite state machine and counters are used in the design for controlling those three signals. [1]

As is shown in Fig. 3, sub-figure (a) shows 1MHz sine wave X(t) generated from DDS module. Sub-figure (b) shows signal Xwin(t), which is the signal X(t) after applying window. Sub-figure (c) shows the spectrum of Xwin(t) which is computed using the FFT function in MATLAB. Sub-figure (d) shows the signal's spectrum computed by FFT IP core in fix-point mode. Thus it can be concluded that result from fix-point hardware FFT is basically correct while some high-order harmonic components of the sinusoidal signal aren't fully presented due to limited data width. However, hardware FFT works much faster than software FFT, so it can be used in real-time condition where precision could not be a critical factor.

Nios II processor module: This module produces control signals to make every module within this system work properly. Furthermore, when FFT IP core is selected, the Nios II processor still takes charge of using complex number from FFT IP core to get amplitude and then generates data for display. When CFFT mode is selected, the Nios II processor is responsible to carry on FFT to input data and then generate data for display.

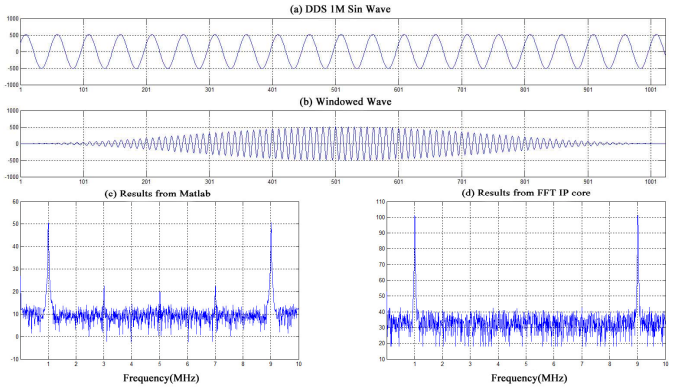

Fig. 3. FFT IP Core Validation

Interface module: This module comprises dual-port RAM module and display interface module. The former are used for data caching and clock domain crossing design between different modules. The latter, whose block diagram is shown at Fig. 4, draws output data from the system on the display according to the VGA timing sequence.

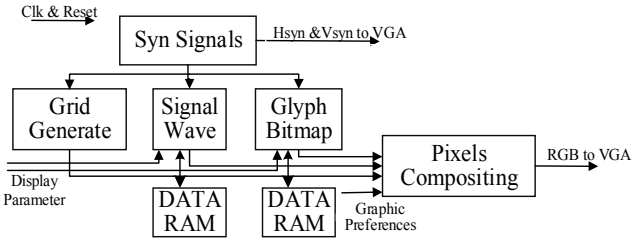

Fig. 4. Display Interface Module Block Diagram

IV. System Software Design

As shown in Fig. 5, the system software design includes five modules: system initialization, mode selection, data

collection, signal analysis and signal display. Three major components of them will be discussed in detail below.

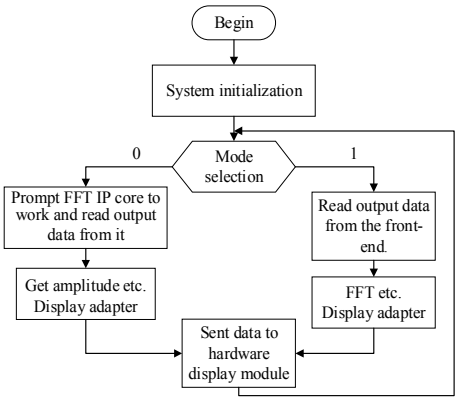

Fig. 5. System Software Flowchart

A. System Initialization Module

After the processor is powered on or reset, it firstly finishes hardware and software initialization, which includes initialization of ports to make every module work in certain states, initialization of logarithmic table to produce binary logarithm and initialization of twiddle factor.

B. Data Acquisition Module

After mode selection process, the system works in a certain mode and begins to acquire data.

FFT IP core mode: In this mode, the processor firstly prompts front-end system to acquire data, and then it monitors the hardware circuit. When a frame of data is gathered, it prompts FFT IP core to work. As soon as FFT is finished, the processor starts to collect output data from FFT IP core.

CFFT mode: In this mode, the processor firstly prompts front-end system to collect data, and then it monitors the hardware circuit. When a frame is gathered, it starts to collect output data from the front-end.

C. Signal Analysis Mode

When processor finishes collecting data from the front-end, the program will treat data differently based on different modes.

FFT IP core mode: In this mode, the program firstly uses complex number and exponential data from FFT IP core to get amplitude by doing quadratic sum and then makes results in log. Among these, the method of lookup tables to take log helps to avoid using intensive computations. Furthermore, the program gets a frame's total energy according to the Parseval's theorem shown below. [2]

$$x(n) \Leftrightarrow X(e^{j\omega}) \tag{1}$$

$$E = \sum_{n=-\infty}^{\infty} |x(n)|^2 = \frac{1}{2\pi}\int_{-\pi}^{\pi} |X(e^{j\omega})|^2 \, d\omega \tag{2}$$

CFFT mode: In this mode, the program firstly assigns the collected data to a complex number array's real part, and sets all its imaginary part to zero. Then this array is used as the input for the FFT computation. The result of the FFT computation is post-processed by doing quadratic sum and then made in log to get amplitude. Lastly, the program gets a frame's total energy according to the Parseval's theorem.

As is shown in Fig. 6, the data meaning of sub-figure (a), (b) and (c) are same to those in Fig. 3. And the sub-figure (d) shows the signal's spectrum computed by Nios II processor. Thus it can be seen that CFFT algorithm's computation precision is higher than FFT IP core at the price of adding computing delay.

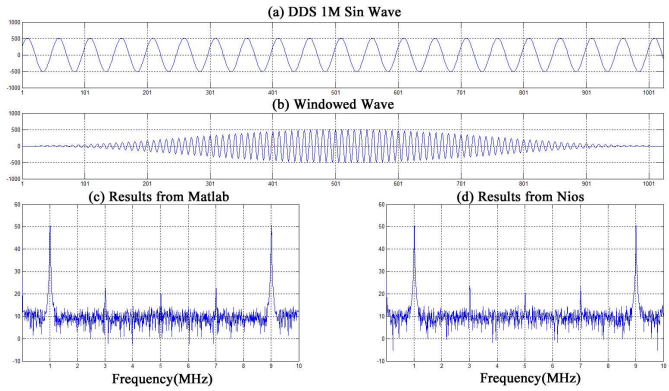

Fig. 6. CFFT Algorithm Validation

V. Entire System Test

This system uses an EP2013 DE0-AD_DA board with an AD9200 chip, a DE0 FPGA board and a VGA display to verify this design, as shown in Fig. 7.

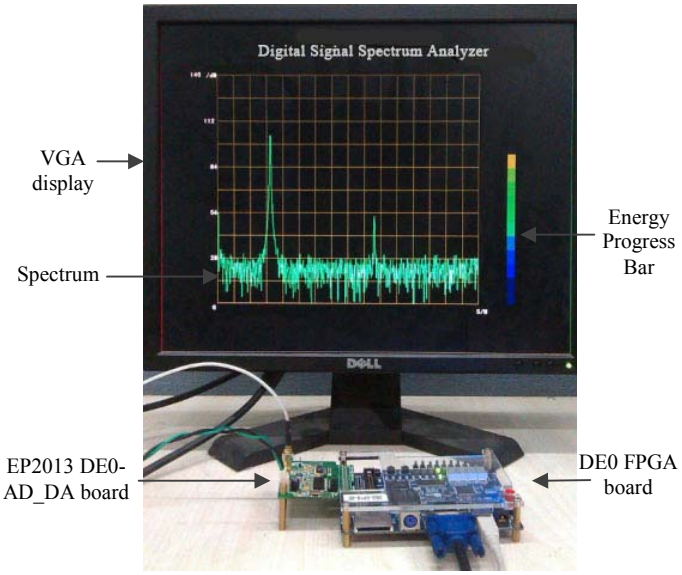

Fig. 7. System Physical Map

A. System Performance

In this system for test, frequency range of display is 0-5 MHz. As there are 16 horizontal grid cells, the precision of each grid is 312.500 kHz/div. The frequency domain resolution of spectrum is 9765.625Hz due to the 1024 point FFT size. Besides, both the vertical axis of spectrum and energy progress bar use logarithmic unit.

B. Test Results

Internal signal mode: In this case, test results are shown in TABLE II.

TABLE II. TEST RESULTS IN TWO MODES AS EXCITATION SIGNAL COMES FROM DDS

FFT IP core		CFFT	
Synthesized frequency (MHz)	***Measured frequency (MHz)***	***Synthesized frequency (MHz)***	***Measured frequency (MHz)***
1	1.03125	1	1.03125
2	2.00000	2	2.00000
3	3.00000	3	3.00000
4	4.00000	4	4.00000

As is shown in TABLE II. , test results in two modes are identical and when synthesized frequency comes to 1.0MHz, measurement results have significant error, because of poor performance of this hardware platform and sparse horizontal grids, which increases reading error. Except for these, other frequency points have high accuracy rate, therefore, this design can measure internal DDS signals precisely.

External signal mode: This design use Tektronix AFG 3102 signal generator [3] to generate seven kinds of sine waves with different frequency as TABLE III. shows, whose amplitudes are 150mv Vpp. The table also presents measuring error in FFT IP core mode and CFFT mode, regarding measurement results from Rohde & Schwarz (R&S) FSW signal and spectrum analyzer[4] as theoretical value.

TABLE III. TEST RESULTS IN TWO MODES COMPARED WITH ACCURATE MEASUREMENT FROM R&S

Input frequency (MHz)	**R&S results (MHz)**	**FFT IP core results (MHz)**	**Absolute error (MHz)**	**Relative error**	**CFFT results (MHz)**	**Absolute error (MHz)**	**Relative error**
1.0	1.0000	1.0313	0.0313	3.13%	1.0313	0.0313	3.13%
1.5	1.5090	1.5000	0.0090	0.60%	1.5000	0.0090	0.60%
2.0	1.9984	2.0000	0.0016	0.08%	2.0000	0.0016	0.08%
2.5	2.4997	2.5000	0.0003	0.01%	2.5000	0.0003	0.01%
3.0	3.0010	3.0000	0.0010	0.03%	3.0000	0.0010	0.03%
3.5	3.4984	3.5313	0.0329	0.94%	3.5313	0.0329	0.94%
4.0	3.9990	4.0000	0.0010	0.03%	4.0000	0.0010	0.03%

As is shown in TABLE III. , with the same input frequency, test results in two modes are identical, so the absolute error curve shown in Fig. 8 belongs to both two modes.

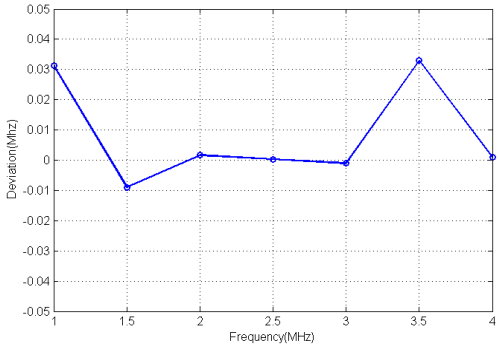

Fig. 8. Absolute Error Curve

As TABLE III. shows, when input frequency comes to 1.0 and 3.5 MHz, measurement results have greater error compared with the precision instrument R&S, which is also relevant to poor performance of this hardware platform and sparse horizontal grids. Except for these, other frequency points have high accuracy rate, therefore, this design is able to measure external analog signals precisely.

VI. CONCLUSION

Besides the basic function of real-time signal analysis and real-time spectrum display, this design adds a function of displaying total energy progress of each frame. Compared with traditional spectrum analysis instruments, this design achieves better portability and modularity so that it can be easily deployed to other FPGA systems to monitor spectrum of intermediate nodes. Compared with traditional embedded data observation systems like SignalTap II Logic Analyzer [5], this design has a stronger ability of spectrum analysis and can display the digital spectrum more intuitively and clearly. This design also has advantages of simple peripheral circuit, simple upgrading and strong ability of function extended.

Furthermore, this design presents a sample of hardware software co-design of soft- core processor, which can be used for reference.

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