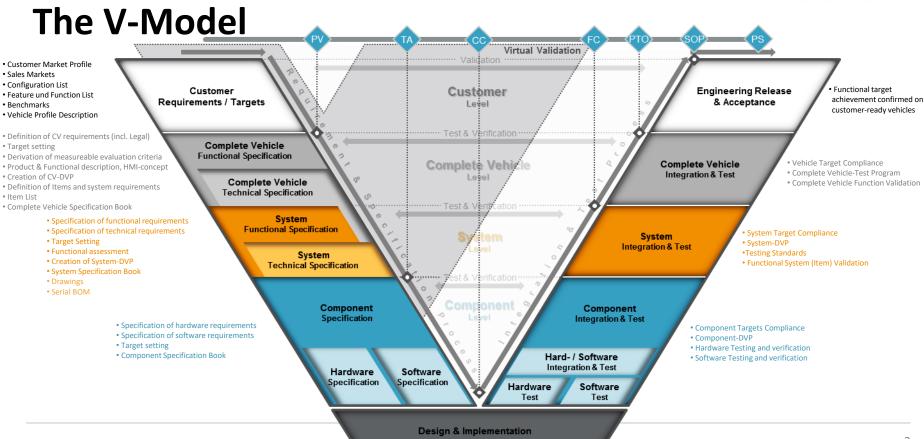


Testing of Automotive Systems (Part I)

Module 6 – HW/SW Tests and Test benches

David Ludwig , Magna Steyr







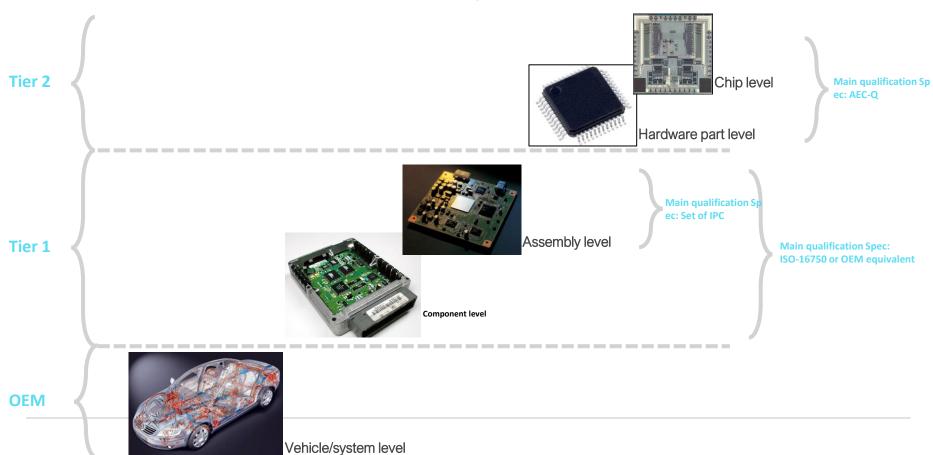
ECU Testing

Hardware

ENGINEERING



HW Standards: Different level definitions in development with focus hardware





Definition of A/B/C/D/E - Samples

A-Sample (Engineering Sample)

Main purpose is to show basic communication and some base functionality is already implemented. It could be either a development board or a design intent housing already

B-Sample (DV-Sample)

All functionality shall be implemented already. All required environmental and EMC tests shall be done.

C-Sample (Off-tool Sample)

100% Off-tool parts – all functionality implemented as well as all **Design Verification (DV) t**asks shall be finished.

D-Sample (PV-Sample)

100% Off-tool and Off-process parts - used to deliver the parts for <u>Product Validation (PV)</u> and <u>Production Part</u> <u>Approval Process (PPAP)</u>

E-Samples (Series Parts)

Serial production parts with continuous conformity testing (CC)



Sample Description

Sample- Category	Use / Purpose	Quality	Software	Manufacturing	Conditions for approval	Testing
A		Customer related functions confirmed. Deviations to specification / functional restrictions are stated in the test report.	Restrictions of functions according specification. Deviations are stated in release notes which are added to the test report.	Hand- work, special manufacturing, modified processes. Partly alternative materials. Rapid prototyping parts. Tacking according internat. standards.	100% testing of characteristics defined in the prototype control plan	Start of testing at MAGNA in special environment with qualified staff. Hardware is not shipped to the customer.
В	DV testing in an extent that the release of the series tools	results. Reliability and lifetime confirmed with	All functions confirmed, which are necessary for the DV testing of the hardware and the operation of the vehicle. All important safety functions confirmed primarily. Deviations are stated in release notes which are added to the test report.	or unhardened steel) and auxiliary devices / fixtures. Target: 100% final material.	100% testing of characteristics defined in the prototype control plan. Prototype process flow chart and control plan supplied	Design verification Testing in vehicles. Defined restrictions for operating
С		Same as B. All functions of the hardware according specification confirmed. Can be flashed in serial production process	Same as B, but all specifications confirmed. All safety functions confirmed.	series process in series	100% testing of characteristics defined in the series control plan. Series process flow chart and control plan supplied	Testing with parts off serial tools. Testing in vehicles. Defined restrictions for operating
D	PV testing PPAP parts Run at rate Release / approval	Same as C Reliability and lifetime confirmed Short-term process capability confirmed. Parts marked like parts from serial production.	Same as D. Documentation finalized.	100% final process at 100% cycle time 100% final tools 100% final material 100% series staff 100% series packing MSA done; IMDS done Parts from / after run@rate	Documentation for process and product approval completed	Product validation Assembly in pre- series vehicles
Series P	Serial production Continuous Conformity Testing	Same as D confirmation of long term process capability	Same as D	Same as D	Same as D confirmation of long term process capability	Assembly in serial vehicles for the customer

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Test Item	Test against	Target Summary	Main Characteristics	Test Bench
Hardware Unit and Integration Testing (HWIT)	Hardware Detailed Design	Verify HW design decisions, functionality	White-box, low level, Hardware	Basic measurement tools, normal working place
	Hardware Architecture Spec	Interfaces between HW Units / Components	White-box, Hardware Component level	Basic measurement tools, normal working place
Hardware Tests (HWT)	HW Requirement Spec	Verify requirements	Mainly black-box	Normal working place HiL Special Lab (climatic, mechanical, chemical chambers
Qualification of HW Comp.	Integrated HW components	Suitability for usage	Testing (functional, climatic) Analysis (simulation, extrapolation)	Special Lab (climatic, mechanical, chemical chambers Computer workplace

HW Development: Hardware Unit and Integration Testing (HWIT) **ENGINEERING**



Verification of:

Hardware Architecture and Detailed Design Specification
Hardware Construction

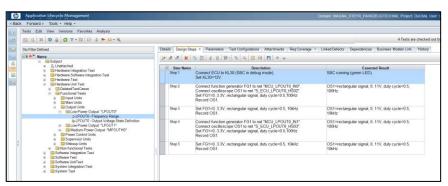
Tasks:

- White Box Testing
- Datasheet Limit/Worst Case Conditions
- Design Decision Limits/Worst Case Conditions
- Electrical Testing
- Error Guessing
- Fault Injection Testing
- Unit Tests
 - HW Functional Testing
- HW Expanded Function Testing
- Integration Tests
- Internal and external Interfaces Functional Testing
- Expanded Interfaces Functional Testing

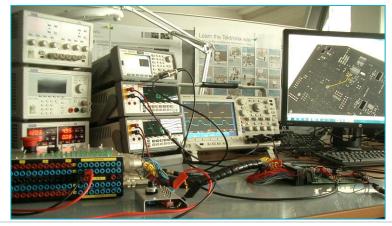
Examples:

- HP ALM Test Specification and Test Steps
- HP ALM Test Results





HP ALM: Hardware Unit Test Specification for Low-Power Output "LPOUT0". Extract with 1 test case and its steps.



HW Unit Test: Measurement setup for frequency range upper limits of medium power output driver.

HW Development: Hardware Testing (HWT) **ENGINEERING**

FH JOANNEUM **Electronic Engineering**

Verification of:

Hardware Requirement Specification (result of Hardware Requirement Analysis)

Tasks:

- Test Plan and Test Specification
- **Black Box Testing**
- Electrical Testing according to OEM/internal standards
- Environmental Testing according to OEM/internal standards

Examples:

- Hardware Qualification Test Plan Overview XGW
- Hardware PV/DV Test Report XGW
- DIAdem Relay Test Issue Report XGW











HiL Testing: Test Bench for electrical Tests

HiL Testing: Test Automation Editor





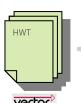


PV/DV Tests: Simulation Boards

PV/DV Test s: Climate Chamber

462450.00 MCU Reset, thus no valid counter value. — Xgw4iCL30 462470.00

PV/DV Test Results Verification: NI DIAdem Report Extract



vector VT System





HW Development: Hardware Testing (HWT) – Test plan ENGINEERING

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Verification of:

Hardware Requirement Specification (result of Hardware Requirement Analysis)

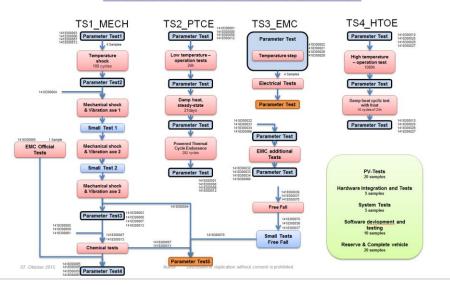
Tasks:

- Specify list of tests to be executed on each sample
- Arrange test samples
- Schedule tests according to development schedule
- Plan and supervise testing budget with PM
- Coordinate testing with external test labs

Examples:

Hardware Qualification Test Plan Overview XGW





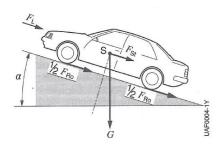


ECU Testing

Hardware in the loop - HiL

EE Testing – Concepts

- Hardware in the Loop and Simulation-based testing
 - testing of electrical functions in an early project phase
 - reproducible testing, automated testing
 - testing is possible long before vehicle prototype is available
 - fault injection made easy



HiL benefits:

- "Virtual Test Drives", ECUs connected to a "mathematical model"
- environmental conditions change on a click (temperature/slope/friction)

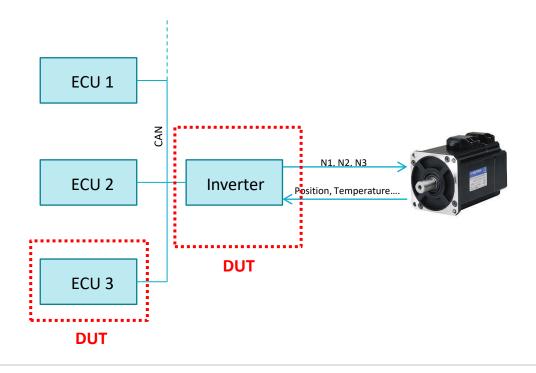
Simulation benefits:

- no complex mathematical models needed
- easy to extend





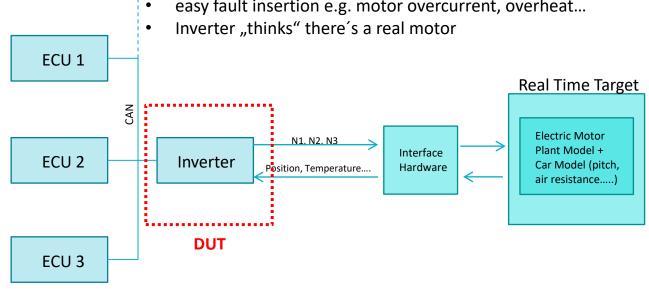
System example - real configuration





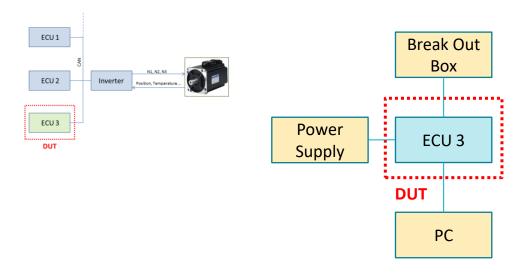
Hardware In the Loop - configuration

- Complete electrical system of the car available
- Mathematical Model of simulated hardware part
- Test bench testing without real electric motor (no moving parts)
- easy fault insertion e.g. motor overcurrent, overheat...

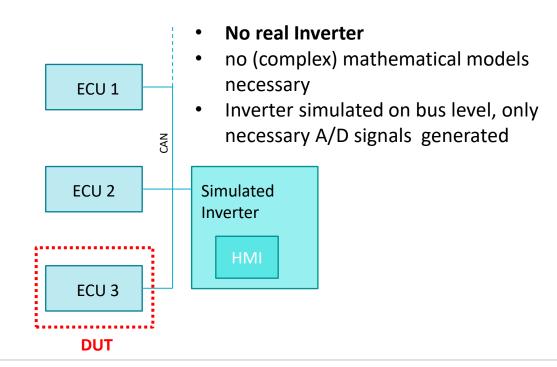




HiL configuration on ECU level



Hardware In the Loop – simulation configuration

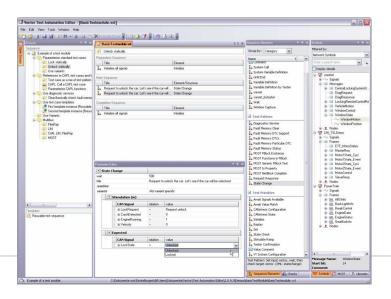




Hardware In the Loop - Tools used

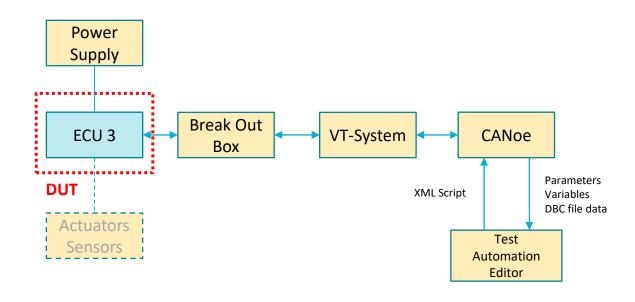
- Test Automation Editor development environment for creating automated ECU tests
- CANoe software tool for development, test, and analysis of entire ECU networks and individual ECUs (LINK)
- VT System Modular Test Hardware comprising bus interfaces, measurement modules, stimulation modules, relay modules...







HiL configuration on ECU level





Input documents and work products

» Input Documents

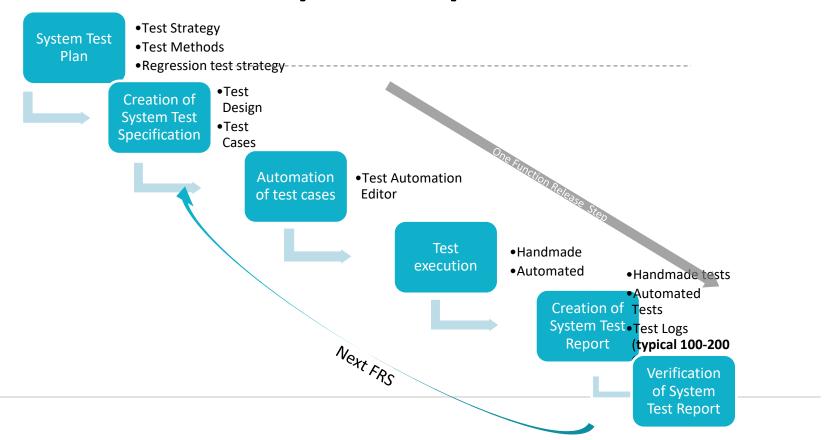
- System Requirement Specification- defined and refined customer requirements/functions on system level
- **Standards (IEEE, ISO)** standardized communication protocols or standardized diagnostic communication in automotive

» Work products

- System Test Plan- defined Test strategy including test methods, test design technics and regression test strategy
- **System Test Specification** including test case specification, test design specification and test environment specification
- System Test Report- Results of all accomplished tests (automated and hand made)
- Traceability Record- All tests have to be traceable to the input document and the next work product



Hardware In the Loop - example



System Test Plan

System Test Plan

4 System Test

4.1 Test Goal

The purpose of the Systems testing process is to ensure that the implementation of each system requirement is tested for compliance and that the system is ready for delivery.

4.2 Test Strategy

4.2.1 Planning and Organization

The test schedule for A-, B-, C-, D-Sample releases can be found in the XGW work product status document APStatus [37].

The project roles for performing the tests can be found in the project role matrix document [38].

Initially, the system requirements specification must be analyzed. The requirements must be prioritized for the impact of these requirements on the operational state of the complete J11 system. Additionally, the requirements must be categorized in safety and non-safety relevant requirements and in functional parts of the system.

For each system requirements a sufficient number of test cases will be defined and documented in the system test specification. The test cases must be developed to demonstrate compliance with the system

Requirements, including the interfaces between system elements. The order of the sequence of the defined test cases shall be derived from priorities and categorization the system requirements in order to find errors earlier in the system development life cycle.

The consistency and bilateral traceability between system requirements and the system test specification including test cases are established by the tool REQTracer. Consistency check is done by review.

The test cases in the test specification includes input test vectors as well as expected results, i.e. output vectors.

4.2.2 Testing Methods

The System test will be done in Black-Box- Testing Method.

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System Test Specification

» Document examples



No.	Test case name	SYSTS0094
	Test case outline	Function test Clamp_50 emergency start
Prio.	Expected test result outline	Clamp_50 activate with emergency start conditions
	Time involved (time effort)	
	,	

Traceability

SYSR0159

Detailed description

Clamp_50_IK (active high HW input)

Clamp_15_1 (active high HW input)

RPM_ENG (PT-CAN, Torque_3)

ST_ENG_RUN (PT-CAN, ENGINE_1)

Clamp_50_IK = 1 (min. 300ms)

ST_ENGINE_RUN)

vehicle speed of is > 10 km/h (V_VEH > 10)

Engine is not running (ST_ENG_RUN~=

Te	est steps:	Test step result
1.	Clamp_15_1 (Analog in) < 3 V	Clamp_50=0
	and	
	Clamp_50_IK = 0	
2.	Clamp_15_1 (Analog in) > 7,5 V	Clamp_50 = 0
	and	
	Clamp_50_IK = 0	
3.	Clamp_15_1 (Analog in)> 7,5 V	Clamp_50 = 1 for a defined time (max. 21 sec)
	and	
l	and and	than Clamp_50 = 0

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System Test Report

No.	SYSTR5418	Test Case Name:	SYSTS0094	
Test type	Α	Test Case Outline:	Function test Clamp_50 emergency start	
Result:	OK	Tester:	Stefan Pfingstl	
OIL Refere	ences			
Annotations and comments				
Test log				
Starter Test Report 1418300024.html				
· -				

No.	SYSTR5419	Test Case Name:	SYSTS0794	
Test type	M	Test Case Outline:	Reset during engine start	
Result:	OK	Tester:	Stefan Pfingstl	
OIL References				
Annotations and comments				
Annotatio	ns and comm	ents		
Annotatio	ns and comm	ents		
Test log	ns and comm	ents		

No.	SYSTR5420	Test Case Name:	SYSTS0795		
Test type	А	Test Case Outline:	During engine start defined outputs shall not be activated:		
Result:	OK	Tester:	Stefan Pfingstl		
OIL References					
Annotations and comments					
Test log					
Starter_Test_Report_1418300024.html					



Test Log (automated test)

7.12 SYSTS0094: Passed

Test case begin: 2014-08-05 13:16:05 (logging timestamp 7085.140305) Test case end: 2014-08-05 13:16:19 (logging timestamp 7099.640305)

Preparation of Test Case

Timestamp	Test Step		Result
1. MC_ABAG	_1 and	l other MCs = 15 (due to MC and Checksum Skript): Passed	
7085.140305		Set specified value. CAN signal 'MC_ABAG_1' on bus Chassis-CAN: 15	
7085.140305		Set specified value. CAN signal 'ALIV_COU_DME' on bus PT-CAN: 15 (Signal ungültig)	-
7085.140305		Set specified value. CAN signal 'ALIV_V' on bus PT-CAN: 15 (Signal invalid)	
7085.140305		Set specified value. CAN signal 'ALIV_GRB' on bus PT-CAN: 15 (Signal invalid)	-
7085.140305		Set specified value. CAN signal 'ALIV_COU_DSC' on bus PT-CAN: 15 (Signal invalid)	
7085.140305		Set specified value. CAN signal 'ALIV_TORQ_1_DME' on bus PT-CAN: 15 (Signal invalid)	
7085.140305		Set specified value. CAN signal 'ALIV_TORQ_3_DME' on bus PT-CAN: 15 (Signal invalid)	
7085.140305	1	Stimulation of the input parameters	pass
7085.140305		Emergency start	-
2. Start condit	itions:	Passed	4
7085.140305		Set specified value. CAN signal 'St_crashOut' on bus Chassis-CAN: 0 (No crash)	
7085.140305		Set specified value. CAN signal 'ST_ENG_RUN' on bus PT-CAN: 0 (Engine off)	
7085.140305		Set specified value. CAN signal 'V_VEH' on bus PT-CAN: 20	
7085.140305		Set specified value. CAN signal 'ST_LK_STRT' on bus PT-CAN: 0 (Kein Motorstart)	
7085.140305		Set specified value. CAN signal 'ST_CT_BRPD_DME' on bus PT-CAN: 0 (Brake not pressed)	
7085.140305		Set specified value.	-



Test file for test automation

```
Tests FRSD1.vxt - Editor
Datei Bearbeiten Format Ansicht
<?xml version="1.0" encoding="iso-8859-1"?>
<!--Vector Test Automation Editor 2.1.28.0-->
<testmodule title="Tests FRS D1" version="1.0" xmlns="http://www.vector-informatik.de/CANoe/TestModule/1.26">
 <testgroup title="Routing">
    <preparation>
      <set title="Kev pos. 1">
        <sysvar name="RelayVBatt" namespace="VTS::M12_Ch16_CL_R">1</sysvar>
        <sysvar name="RelayVBatt" namespace="VTS::M12_Ch14_CL_15_1">0</sysvar>
<sysvar name="RelayVBatt" namespace="VTS::M12_Ch13_CL_50_IK">0</sysvar>
      <wait title="Wait" time="500" />
      <set title="Key pos. 2">
        <sysvar name="RelayVBatt" namespace="VTS::M12_Ch16_CL_R">1</sysvar>
        <sysvar name="RelayVBatt" namespace="VTS::M12_Ch14_CL_15_1">1</sysvar>
        <sysvar name="RelayVBatt" namespace="VTS::M12_Ch13_CL_50_IK">0</sysvar>
      <wait title="Wait" time="500" />
    </preparation>
    <testcase title="SYSTS0109" ident="">
      <preparation>
        <vardef name="Cycle" type="int" default="0">1</vardef>
        <set title="MC_IPC_2 = 15">
          <cansignal name="MC_IPC_2">15</cansignal>
        </set>
      </preparation>
      <for_loop title="Cycle" loopvar="Cycle" stopvalue="3" startvalue="0" increment="1">
        <set title="N_TempEx = -40">
          <cansignal name="N_TempEx">-40</cansignal>
        <wait title="Wait" time="1s" />
      </for_loop>
      <statechange title="N_TempEx - TEMP_EX = -40" wait="1s">
          <cansignal name="N_TempEx">-40</cansignal>
        </in>
        <expected>
          <cansignal name="TEMP_EX">-40</cansignal>
        </expected>
      </statechange>
```



System Testbenches



Network testbench

- Easy accessible ECUs
- All ECUs are connected with supply and bus communication wires to the test bench
- E/E system tests can be done before vehicle building starts
- Automated tests for diagnostic, bus errors, buslogic, management, gateway
- Fast hardware replacement
- No influence from wiring harness





Network testbench – test content

- Flash verification
- check of the raw data
- check of logistic data for/after flash
- check the bus behavior by ECU flash
- switch off bus at ECU flash





Subsystem (domain) testbench

- Automated validation of the complete function-network
- Automation of the validation steps incl. automated test report generating, by plugging and switching via Robot for all customer-, long-term-, voltage-, diagnosis- and coding tests.
- Automation with 4 engineering tools:
 - TestStand
 - LabView
 - CANoe
 - Katana 4D (Robot)



Subsystem (domain) testbench – test content

- System functions (partly automated):
 - Pinning / wiring (pinning, coding)
 - Bus verification (CAN, LIN, Ethernet, etc.)
 - Bus-Physic (Error Frames, ramp up/down time, voltage level, load resistor, error simulation)
 - Bus-logic (message errors, service messages)
 - Bus load (stress impact, power up/down, rest bus simulation stress load)
 - Hardware-Signals 1:n connections
 - Voltage tests (under voltage, cranking profile, etc.)
 - Failure simulation (signal failure, cable failure, ECU malfunction, invalid signals)
 - Misuse tests (reverse polarisation, short cut, etc.)
 - Flash, diagnostics
 - Gateway tests





Powertrain Sub System Test Bench

Test content:

- •Verification of local buses (CAN-High, CAN-Low, LIN, etc.)
- •Bus-Physic (Error Frames, ramp up/down time, voltage level, load resistor, error simulation)
- •Energy-Management (quiescent current, power up/down)
- •Bus-logic (message errors, service messages)
- •Failure simulation (signal failure, cable failure, ECU malfunction, invalid signals)
- •Bus load (stress impact, power up/down, rest bus simulation stress load)
- Misuse tests
- •Flash, diagnosis, gateway
- •customer function tests (checklist)
- •HV function validation with all HV components
- •HW/SW development platform





ADAS Sub System Test Bench

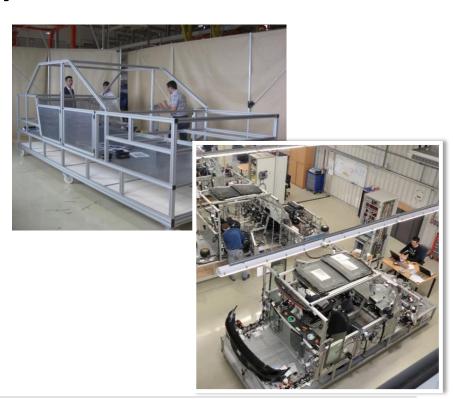
Test content:

- Base customer function testing (with original Components)
- Static maneuver testing (Ideal virtual world)
- Failure/Manipulation/Stress testing (Wiring/ECU/Sensor/Actuator failures)
- HMI Validation (functionally)
- EE maturity monitoring
- Vehicle Configuration and Vehicle variant testing
- Safety robustness validation
- Automated testing, Repetitive testing, Long-time testing and Variation testing
- Free and stochastic testing and error analysis



Laboratory Vehicle (Labcar) - Overview

- Aluminium frame
- Easy accessible ECUs and harness
- Fast hardware replacement without disassembling the complete vehicle
- Original vehicle wiring harness and all ECU's, sensors and actuators are integrated into the test platform.
- Complete system tests can be done before vehicle building starts
- Automated test sequences (LabVIEW, CANoe, C#)
- HIL-Simulation (NI, dSPACE)
- Residual bus simulation for missing ECU's



Laboratory Vehicle (Labcar) – test content

- E/E system function tests
 - wiring harness validation
 - flashing/coding verification
 - physical/logical bus layer tests (CAN,LIN, Ethernet)
 - clamp control tests
 - network management tests (Autosar)
 - hardwired signal measurements
 - voltage tests according specification (ISO 16750-2, LV124,...)
 - quiescent current measurements
 - power management functions
 - diagnostic function tests
 - gateway tests
- Customer function tests



Vehicle Intensive Test (VIT)

- Assembling and Configuration of special measurement equipment
- Assembling of data logging equipment for AnalysisVehicle upgrades incl. flashing of the control units and error analysis
- Mechanical and electrical Vehicleupgrades
- Commissioning of complete vehicles at the customer and at the PT Shop incl. Flashing, Coding and Functioncheck.





Vehicle Intensive Test (VIT) – test content

- Validation of system and customer function tests incl. stochastic tests during off-duty testdrives
- "Free testing"
 - Reproduce typical consumer behavior
 - Reproduce misuse
- Summer/wintertestdrives and special component trails on different countries. (e.g. head unit, navigation)
- Support of product demonstrations on trade shows
- Vehicle build up support on the in-plant production line





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Tools: Data Loggers





EMC compliant?	yes	no				
Placement close to ECU's?	yes	not always				
Interfaces for all bus technologies?	yes	no				
Testing without manual?	yes	no				
Invisible for the driver?	yes	no				
Temperature range (-40° to 60°C)?	yes	no				
Shock resistant?	yes	no				
Autonomous logging?	yes	no				
Second driver needed?	no	sometimes				





System Testing

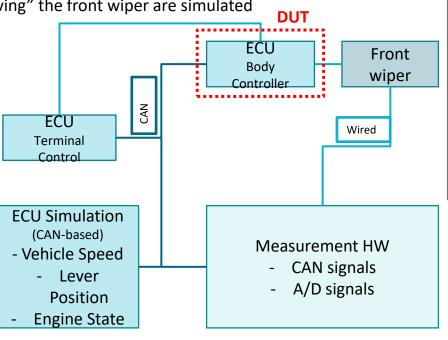
Front Wiper Example

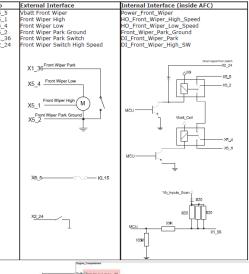
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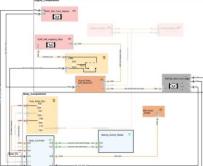
Hardware In the Loop - example

ECUs which are operating the front wiper assembly are physically available

ECUs which are not "driving" the front wiper are simulated









Front wiper testing – ECU Simulation

From specification
5.3.2 Interface Requirements
5.3.2.2 CAN Signal Inputs

- Engine management system (EMS) simulation for Engine State
- Electronic stability control (ESC) simulation for Vehicle Speed
- Steering column modules (SCM) simulation for Lever Position

Signal Logical Name	Description						
C_FrontWiper_LowSpeed_SW_ST	Front wiper low speed switch input on CAN - SCM						
C_FrontWiper_HighSpeed_SW_ST	Front wiper high speed switch input on CAN - SCM						
C_FrontWiper_IntermSpeed_SW_ ST	Front wiper intermittent speed switch input on CAN - SCM						
C_FrontWiper_MistMode_SW_ST	Front wiper mist mode switch input on CAN - SCM						
C_FrontWiper_Interval_SW_ST	Front wiper interval switch input on CAN - SCM						
C_FrontWasher_SW_ST	Front washer switch input on CAN - SCM						
C_VehicleSpeed_ESC	Speed information from ESC ECU- ESC						
C_EngineState_EMS_ST	Engine state status from EMS ECU - EMS						



Front wiper testing – Measurement

- A/D signals to monitor
- CAN signals

From specification

5.3.2.2 Digital Inputs

Signal Logical Name	Description
HW_Ignition_ST	KL15 power supply input
HW_FrontWiper_Park_SW_ST	Front wiper park switch status

5.3.2.3 Digital Outputs

Signal Logical Name	Description					
HW_FrontWiper_OnOff_CMD	Front wiper power enable relay output					
HW_FrontWiper_HighLow_CMD	Front wiper high/low speed relay output					
HW_FrontWasher_CMD	Front washer output					
HW_HeadlampWasher_CMD	Headlamp washer output					



Front wiper testing – Speed Mode Test

From specification

5.3.5 Function Requirements

5.3.5.4 Front Wiper Intermittent Mode

Dwell Time of Front Wiper Intermittent Speed Class Mode

ID: FRS AFC FWP 018:

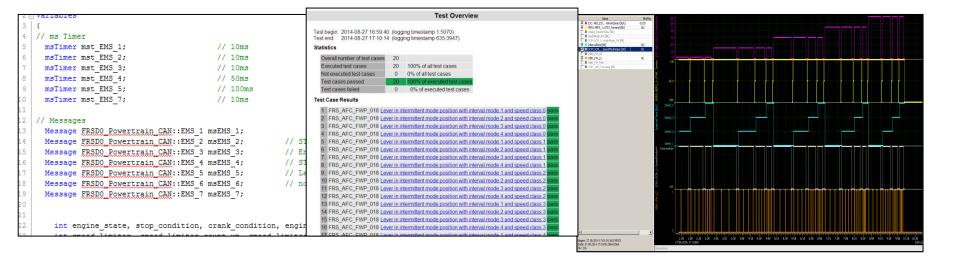
There are 5 speed class variations available with 4 dwell times in each class. The dwell time should only be changed from one vehicle speed class to another vehicle speed class when the wiper motor is in park position.

Interval Adjust switch	Vehicle speed class (kph)									
position	V0 (<5)	V1 (32)	V2 (<64)	V3 (<96)	V4 (>=96)					
Interval 1, dwell time in s	24	16	12	10	8					
Interval 2, dwell time in s	15	10	8	6	4					
Interval 3, dwell time in s	8	5	4	3	2					
Interval 4, dwell time in s	3	2	2	1	1					
Default, dwell time in s	8	5	4	3	2					

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Wiper Speed Mode Testing – Test sequence

- Prepare test environment (supply voltage, parameter sets, simulated ECUs...)
- Prepare test modules
- Start testing
- Test report generation

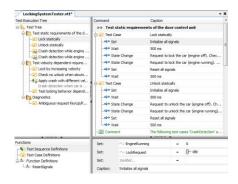




Hardware In the Loop - Tools used

- vTESTstudio development environment for creating automated ECU tests
- CANoe software tool for development, test, and analysis of entire ECU networks and individual ECUs (LINK)
- VT System Modular Test Hardware comprising bus interfaces, measurement modules, stimulation modules, relay modules...









Laboratory exercise 28/10/22

Preparation

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Lab Exercise overview

- Meet 28/10 at Magna Steyr Main Entry Liebenauer Hauptstr.317 at 11.30
 - Be on time, access takes a while!
- Lab time 12.00h-16.00h (approx.)
- Contents: 4 exercise parts
- Tools used: CANoe, Measurement equipment (all onsite)
- Please bring your own laptop and USB stick for notes, save CAN-Traces etc.

The exercises must be documented in a test report

<u>Due date test reports 04/11 (will be part of grading)</u>

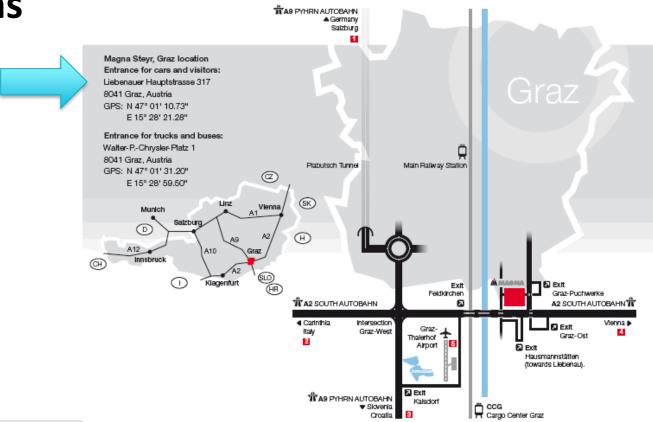
Template provided via moodle

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Directions





Roof Console

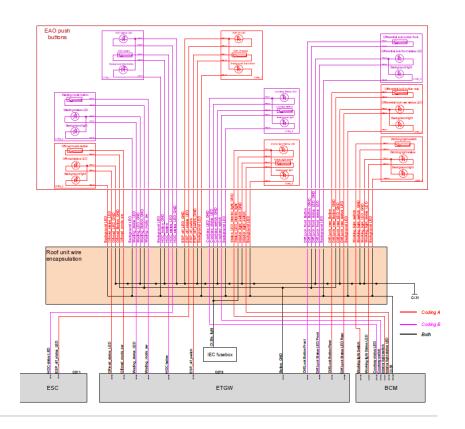
SYSTEM-SCHEMATICS of Roof Console



Task 1: Connect all the buttons on the Roof Console to the wiring harness and check the correct pinning according the system schematics

Find this document on USB drive:

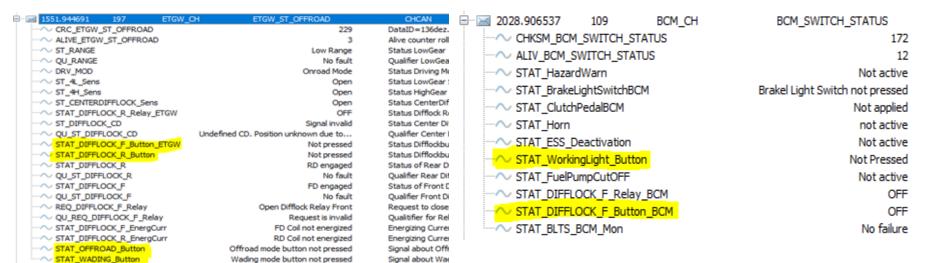
RoofPannelPinning.pdf





Check the functionality of the Roof-panel switches on CHASSY-CAN:

→ For following switches there is no CAN signal available, therefore it is only possible to check the correct pinning or the functionality itself : ESP-,HDC-,Curtesy-,Iterior light- Button





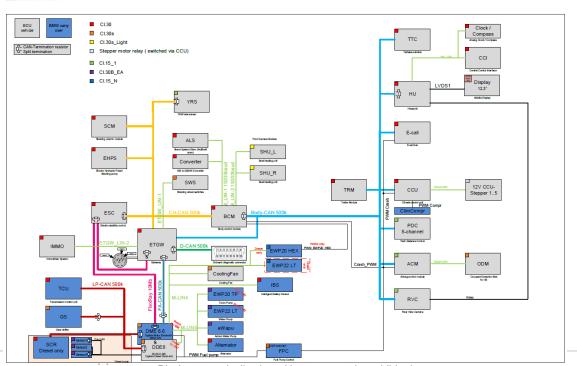
CAN-Communication



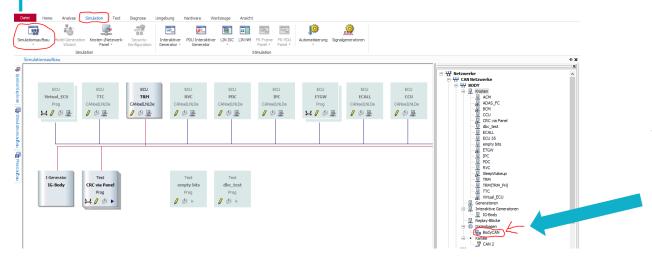
Overview Complete Architecture







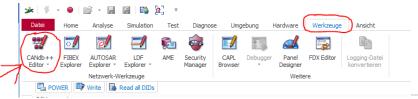




Including the .dbc file

How to find the CAN

database:



CAN-Database/Matrix → .dbc



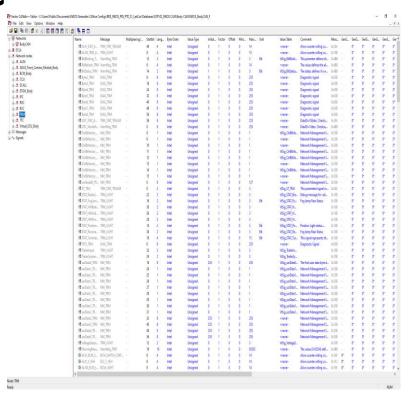
Task 2: Check the CAN-communication according the .dbc file for the BODY- and CHASSY-CAN network:

[BODY-CAN:]

- 1.) Check the CAN for error-messages (are shown in color in CANoe) (why?)
- **2.)**Check if all nodes are sending on CAN network (If not why?)
- **3.)** Search for CAN ID: 3FA on the active Bus network(Body-CAN) → (Is it sending correctly?)

[CHASSY-CAN]

4.)Check the cycle times of all messages transmitted from BCM



All .dbc files also provided on USB drive



SIMULATION



Simulation of a disconnected ECU

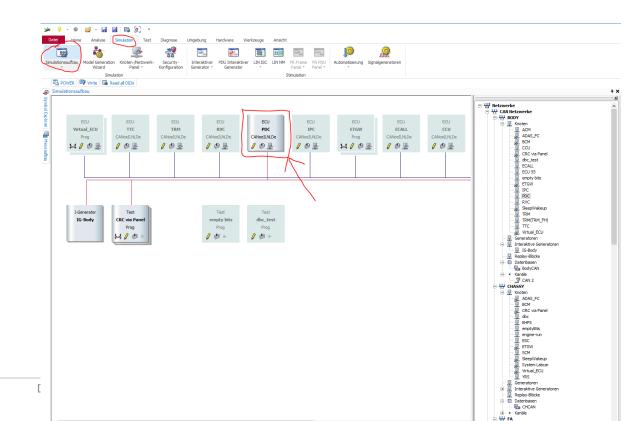
Task 3:

1.)

Disconnect the PDC(**P**ark**D**istance**C**ontrol) unit from wiring harness.

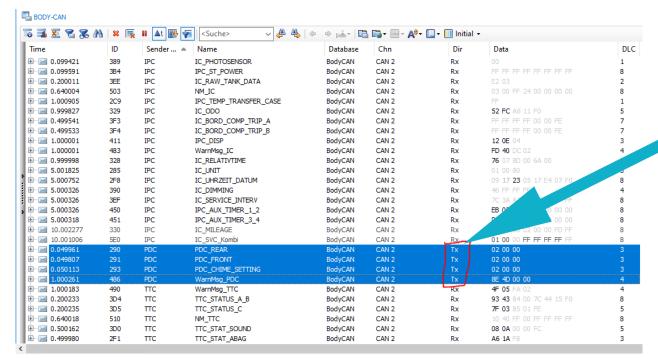
2.)

Activate the PDC simulation node and start the measurement



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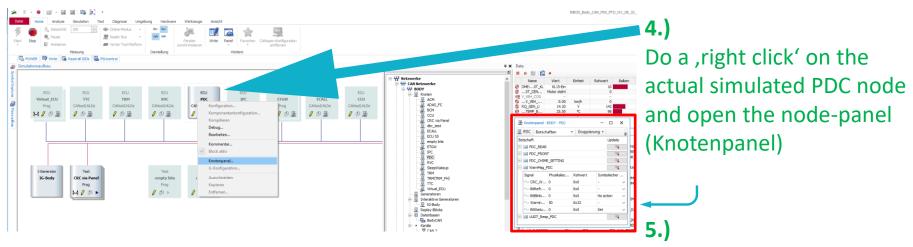
Check if the Simulation works correctly



Tx→ means that those messages are transmitted by our simulation

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Simulation of a Warning which should be shown to the driver



Simulate the warning ID:50 and send it with "SET" to activate and "RESET" to deactivate the warning message

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Check if the warning gets displayed correctly to the driver

1.)

The warning must be added to the list (Active warning message menu)

2.)

On IPC(Instrument Panel Cluster) part, all the warnings from the list must get displayed intermittened



Settings → Vehicle Functions → Vehicle Information → Active warning and Status Messages



Problem finding



provided on USB drive

Component Data Sheet CDS

Task 4: After an Gateway software update, the functionality of the Steering wheel switches is not given anymore. The SWS (**S**teering **W**heel **S**witches) worked correctly

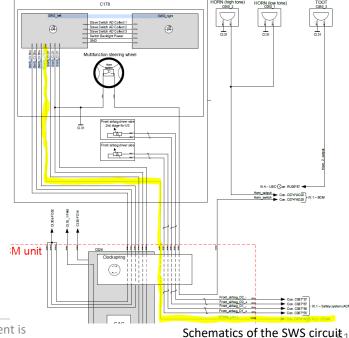
before the SW update.



Gateway ECU (ETGW)

Discuss together:

- 1.) What could lead to the problem?
- 2.) What can be done to find out the root cause?



Component Data Sheet CDS Current implementation: Imp

Implementation with new Gateway

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Software

	Pin Number	I/O Type	Clamp Definition	Signal Definition	Drive Definition - High/LowSide/PWM - int. Relay	wire size mm²	Crimp Conntact	Socket Number	Pin Number	r I/O Type	Clamp Definition	Signal Definition	Drive Definition - High/LowSide/PWM - int. Relay	wire size mm²	Crimp Conntact
				4										7	
	1	BUS	LIN1	Steering wheel switches	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)		1	BUS	LIN1	reserved, not needed	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)
	2	BUS	LIN2	Immobilizer	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)		2	BUS	LIN2	Immobilizer	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)
	3								3	BUS	LIN5	Steering wheel switches	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)
	4	BUS	LIN3		20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)		4	BUS	LIN3	reserved, not needed	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)
	5	BUS	LIN4		20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)		5	BUS	LIN4	reserved, not needed	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2)
	6								6				1 11 51 511		
	7	I/O_IN	Hall1PWMK	4H/L hall PWMK	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)		7	I/O_IN	Hall1PWMK	4H/L hall PWMK	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)
	8	I/O_IN	Hall1PMW	4H/L hall PWM	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)		8	I/O_IN	Hall1PMW	4H/L hall PWM	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)
	9	I/O_IN	Hall2PWMK	center diff.lock hall PWMK	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)		9	I/O_IN	Hall2PWMK	center diff.lock hall PWMK	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)
	10	I/O_IN	Hall2PWM	center diff.lock hall PWM	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)		10	I/O_IN	Hall2PWM	center diff.lock hall PWM	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)
	11	I/O_IN	Hall3PWMK		Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)		11	I/O_IN	Hall3PWMK	reserved, not needed	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)
	12	I/O IN	Hall3PWM		Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)		12	I/O_IN	Hall3PWM	reserved, not needed	Lowside 5V PWM	0.35	MQS (0.25-0.35mm2)
	13	_					,		13		ACNIDA			0.05	
	14	ANALOG GND	AGND1	analog GND buttons		0.35	MQS (0.25-0.35mm2)		14	ANALOG_GND	AGND1	analog GND buttons	1 11 51150	0.35	MQS (0.25-0.35mm2)
	15	I/O IN	AIM1	front diff.lock button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)		15	I/O_IN	AIM1	front diff.lock button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)
	16	I/O IN	AIM2	rear diff.lock button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)		16	I/O_IN	AIM2	rear diff.lock button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)
	17	I/O IN	AIM3	wading mode button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)		17	I/O_IN	AIM3	wading mode button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)
	18	I/O IN	AIM4	offroad mode button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)		18	I/O_IN	AIM4	offroad mode button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)
	19		7 411	Sill Gud Tita 22 22 22 22	Edward C :	0.22	mao (o.zo z.zzz,		19	BUS	CAN6P	Station Wagon -> reserved Pickup GSR -> HMI-CAN high	2Mbit/s 120R-Termination wakeup	0.35	MQS (0.25-0.35mm2)
	20								20			Pickup GSR -> mivii-CAN nign	4		
	21								20	DUE	LING	d not needed	COLPd Masternada universa	0.5	**00 (0.5.0.75
	22								21 22	BUS	LIN6 LIN7	reserved, not needed	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2) MQS (0.5-0.75mm2)
	23	DIGITAL GND	DGND1	digital GND 4H/L hall		0.35	MQS (0.25-0.35mm2)		22	DIGITAL GND	DGND1	reserved, not needed digital GND 4H/L hall	20kBd Masternode wakeup	0.5	MQS (0.5-0.75mm2) MQS (0.25-0.35mm2)
	24	I/O OUT	Hall1+	supply 4H/L hall	Highside CV 5V	0.35	MQS (0.25-0.35mm2)		23	I/O OUT	Hall1+	supply 4H/L hall	Historida CV/ EV/		
	25	DIGITAL GND	DGND2	digital GND center diff.lock hall		0.35	MQS (0.25-0.35mm2)		25	DIGITAL GND			Highside CV 5V	0.35	MQS (0.25-0.35mm2) MQS (0.25-0.35mm2)
	26	I/O OUT	Hall2+	supply center diff.lock hall	Highside CV 5V	0.35	MQS (0.25-0.35mm2)		26	I/O OUT	Hall2+	digital GND center diff.lock hall supply center diff.lock hall	Highside CV 5V	0.35	MQS (0.25-0.35mm2)
	27		Hall3+	supply center uninock nam		0.35	MQS (0.25-0.35mm2)		27	1/O_OUT	Hall3+	reserved, not needed	Highside CV 5V	0.35	MQS (0.25-0.35mm2)
Α -		I/O_OUT	maii3+		Highside CV 5V	0.35	MQS (0.25-0.35ffm2)	Α	28	1/0_001	папэт	reserved, not needed	nighside CV 5V	0.35	MUS (U.Zo-U.SSIIIIIZ)
	28	L/O IN	AIDMA		TO LITE WHILE CAND COURT OF A DOCUMENT	0.25	***********************		29	I/O IN	AIPM1	coolant level sensor 1	High/Lowside GND/30BL/5V ADC/PWM	0.35	MQS (0.25-0.35mm2)
	29	I/O_IN	AIPM1		High/Lowside GND/30BL/5V ADC/PWM	0.35	MQS (0.25-0.35mm2)		30	1/O_IN	AIPM2	coolant level sensor 2	High/Lowside GND/30BL/5V ADC/PWM	0.35	MQS (0.25-0.35mm2)
	30	I/O_IN	AIPM2		High/Lowside GND/30BL/5V ADC/PWM		MQS (0.25-0.35mm2)		31	1/0_IN	AIPM3	reserved, not needed	High/Lowside GND/30BL/5V ADC/PWM	0.35	MQS (0.25-0.35mm2)
	31	I/O_IN	AIPM3		High/Lowside GND/30BL/5V ADC/PWM	0.35	MQS (0.25-0.35mm2)		32	I/O IN	AIPM4	reserved, not needed	High/Lowside GND/30BL/5V ADC/PWM	0.35	MQS (0.25-0.35mm2)
	32	I/O_IN	AIPM4		High/Lowside GND/30BL/5V ADC/PWM		MQS (0.25-0.35mm2)		33	ANALOG GND	AGND2	reserved, not needed	Tilgii/Lowside GND/30DL/3V ADG/T VVIVI	0.35	MQS (0.25-0.35mm2)
	33	ANALOG_GND			4	0.35	MQS (0.25-0.35mm2)		34	I/O IN	AIM7	reserved, not needed	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)
	34	I/O_IN	AIM7		Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)		35	I/O IN	AIM6	ESP button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)
	35	I/O_IN	AIM6	ESP button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)		36	I/O IN	AIM5	HDC button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)
	36	I/O_IN	AIM5	HDC button	Lowside 5V ADC	0.35	MQS (0.25-0.35mm2)			_		Station Wagon -> reserved			· · · · · · · · · · · · · · · · · · ·
	37								37	BUS	CAN6N	Pickup GSR -> HMI-CAN low	2Mbit/s 120R-Termination wakeup	0.35	MQS (0.25-0.35mm2)
	38						-	.—	38			Fickup Gold -> Tilling at low	•		
	39	I/O_IN	DIM5	handbrake switch NC	Lowside CC 30BL wakeup	0.35	MQS (0.25-0.35mm2)	. 10	39	I/O IN	DIM5	handbrake switch NC	Lowside CC 30BL wakeup	0.35	MQS (0.25-0.35mm2)