Biasing & Swing limits

In the operating region, all MOSFETs are in saturation.

The current mirror M_{00} sets current $\frac{32}{9} I_0$ in M_0 and $\frac{160}{9} I_0$ in M_6 by setting their gate voltages as:

$$V_{GS00} = V_{GS0} = V_{GS5} = V_{Tn} + \sqrt{\frac{2I_0}{9k_{00}}}$$

$$= 0.5 + \sqrt{\frac{2 \times 200\mu}{9 \times 400\mu}} = 1V$$

As M_5 is in saturation:

$$40 I_0 = \frac{k_5}{2} \times 640 \times (V_{SG5} - V_{TP})^2$$

$$40 \times 200\mu = 100\mu \times 320 \times (5 - V_{GS5} - 0.5)^2$$

$$\Rightarrow V_{GS5} = 4V \quad \text{(gate voltage of } M_5\text{)}$$

For differential pair, $V_{D1} = V_{D2} = V_{GS5} = 4V$

For M_1, M_2 to be in saturation:

$$V_{D1} \geq V_{G1} - V_{Tn}$$

$$4 \geq V_i - 0.5 \Rightarrow \boxed{V_i \leq 4.5V}$$

If M_1, M_2 are in saturation,

$$V_i - V_{tail} = V_{TN} + \sqrt{\frac{2\left(\frac{8I_o}{2}\right)}{16k_1}}$$

$$= 0.5 + \sqrt{\frac{8 \times 200\mu}{16 \times 400\mu}} = 1V$$

For M_0 to be in saturation,

$$V_{tail} \geq V_{GS0} - V_{TN}$$

$$V_{tail} + 1 \geq 1 + 1 - 0.5$$

$$\Rightarrow \boxed{V_i \geq 1.5V}$$

Hence, input voltage, $V_i = V_{icm} + V_{cm} \pm \frac{V_d}{2} \in [1.5, 9.5]V$

For M_6 to be in saturation,

$$V_o \geq V_{G6} - V_{TN} \Rightarrow \boxed{V_o \geq 0.5V}$$

For M_5 to be in saturation,

$$V_o \leq V_{G5} + V_{TP} \Rightarrow \boxed{V_o \leq 9.5V}$$

Hence, output voltage, $V_o = V_{o\,bias} + V_{out} \in [0.5, 9.5]$ V