DESIGNING OF RING OSCILLATOR (RO) PHYSICAL UNCLONABLE FUNCTION (PUF) BY USING 3 - TRANSISTOR XOR GATE

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ABSTRACT :

Physical Unclonable Function (PUF) is primarily used for security purposes. Security has become a major concern these days. Therefore, to prevent this issue PUFs are inserted into the system during manufacturing only. Light weight electronic devices have appeared as optimistic electronic equipment. PUF is a kind of key generation and authentication circuit in light weight electronic chips. PUF provides a unique identification ID based on the characteristics of the system and the output of PUF is generated in the digital format. So, that no one can replicate the original system. Therefore these PUFs are very useful devices in securing the system designs. Hence, PUF is an encouraging security primitive. PUFs are mainly used in various fields like information security. These devices have an unpredictable property since they have uniqueness and reliability. In this paper we are designing a new Ring Oscillator (RO) Physical Unclonable Function (PUF) by using 3 transistor XOR gates for increasing the speed of the operation.

INTRODUCTION :

In the project we are going to implement the RO PUF design which is shown in fig-1.

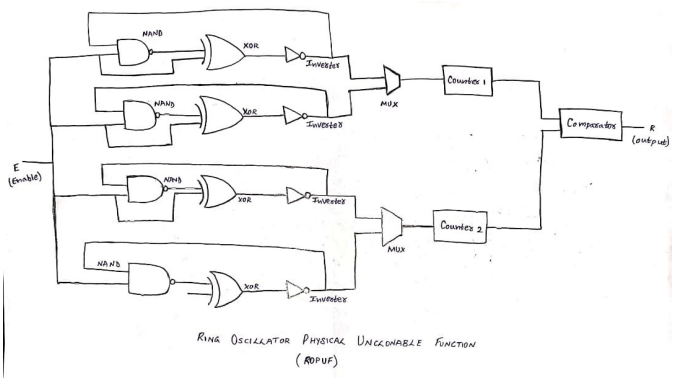

Fig - 1

In this RO PUF we have used the nand gate, xor gate, inverter, 2x1 mux, a 4 bit counter and a comparator. RO i.e Ring Oscillator, the basic structure of ring oscillator is it consists of nand gate, xor gate and a inverter. So, in this project we have used 4 ring oscillators. We have used 4 ring oscillators and the output of this 4 ring oscillators are connected to the 2x1 mux. The operation of this RO PUF is, firstly one of the inputs of 4 nand gate are connected to the enable pin and the other input of 4 nand gates are connected to the inverter output. Then the output of nand gate is connected to one of the input of xor gate and the one of the input of nand gate is also connected to the input of xor gate as you can see in the fig-1. Now, the output of xor gate is connecter to an inverter which is nothing but a not gate and the output of inverter is given to the input of the 2x1 mux. And mux consists of select lines so these are the challenges in this project. Then the output of mux is given to input of the counter which we have taken. Finally the output of counter is connected to the input of comparator. So, this comparator will compare the output and give us

the final output which is unique id in this project. Like this RO PUF is developed in this project.

IMPLEMENTATION :

In this project firstly we have implemented all the basic gates such as nand gate, xor gate, inverter, 2x1 mux, counter and comparator which are required for this project. Then finally we have combined altogether and given the connection then we have generated the output.

NAND GATE :

By using the CMOS we have developed the nand gate schematic. This schematic diagram is shown in fig - 2. It consists of both PMOS and NMOS. And the output is shown in fig - 4. We verified our output based on the nand gate truth table which is shown in fig - 5. And the specifications which we have used is listed below.

Length of PMOS → 240n M
Length of NMOS → 120n M

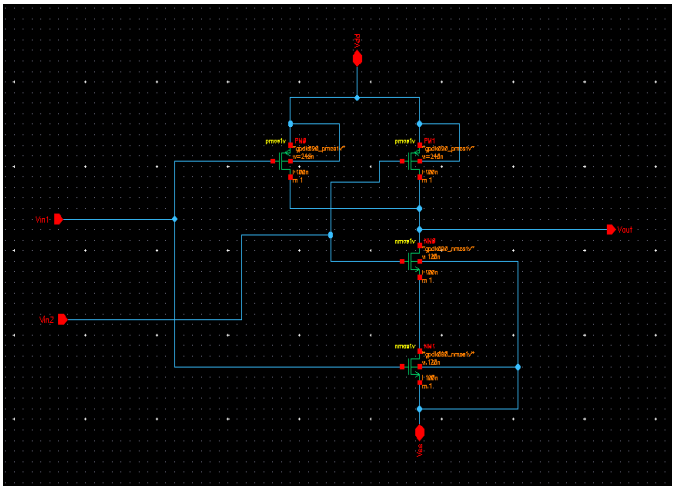

Fig - 2 : NAND GATE SCHEMATIC

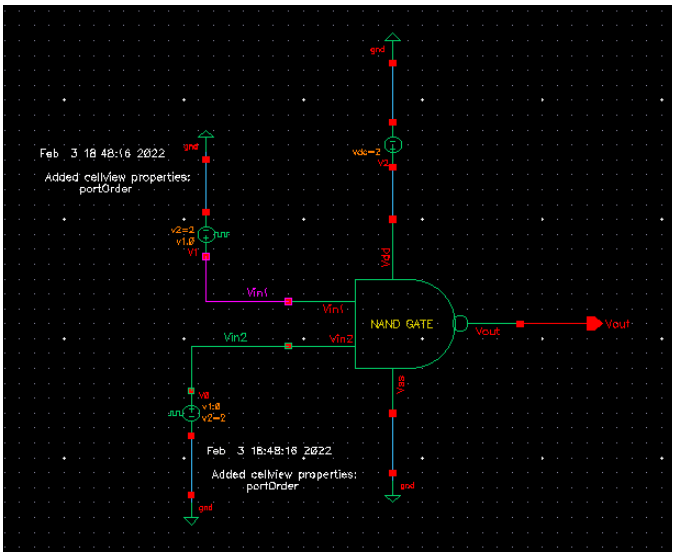

Fig - 3 : NAND GATE TEST

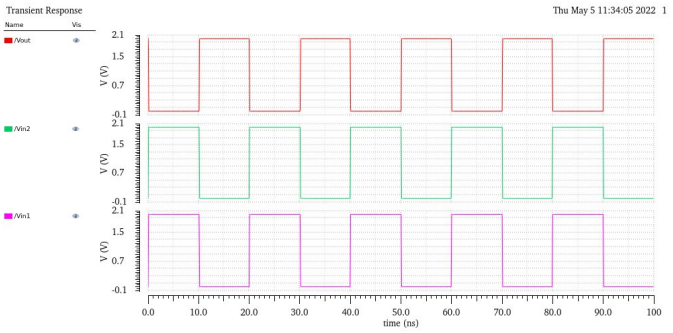

Fig - 4 : NAND GATE OUTPUT

INPUT		OUTPUT
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

Fig - 5 : NAND GATE TRUTH TABLE

XOR GATE :

By using the CMOS we have developed the xor gate schematic. This schematic diagram is shown in fig - 6. It also same as nand gate schematic which consists of both PMOS and NMOS. And the output is shown in fig - 7. We verified our output based on the xor gate truth table which is shown in fig - 9. And the specifications which we have used is listed below.

Length of PMOS → 520n M
Length of NMOS → 240n M

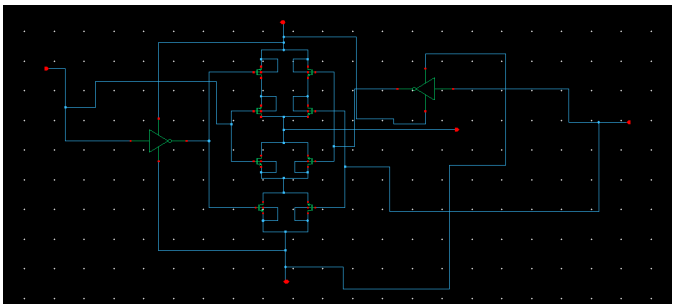

Fig - 6 : XOR GATE SCHEMATIC

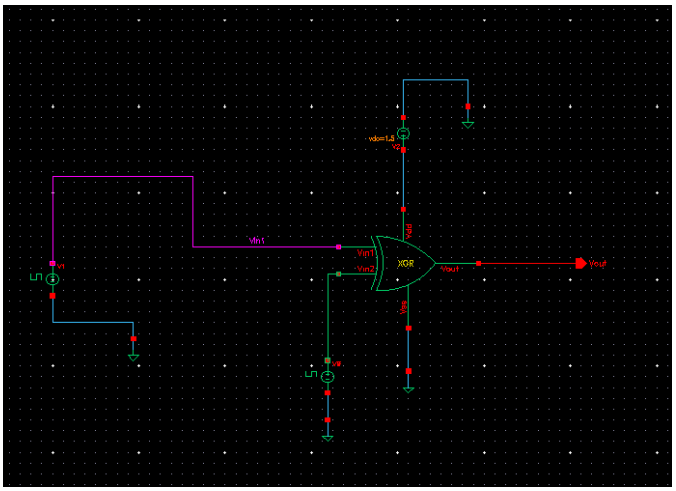

Fig - 7 : XOR GATE TEST

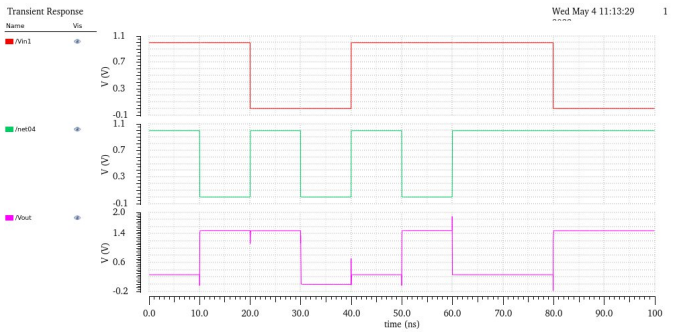

Fig - 8 : XOR GATE OUTPUT

INPUT		OUTPUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Fig - 9 : XOR GATE TRUTH TABLE

INVERTER :

By using the CMOS we have developed the inverter schematic. This schematic diagram is shown in fig - 10. Inverter means if the input is 1 then the output will be 0 and vice versa if the input is 0 then the output will be 1. And, It also same as xor gate and nand gate schematic which consists of both PMOS and NMOS. And the output is shown in fig - 12. And the specifications which we have used is listed below.

Length of PMOS → 240n M
Length of NMOS → 120n M

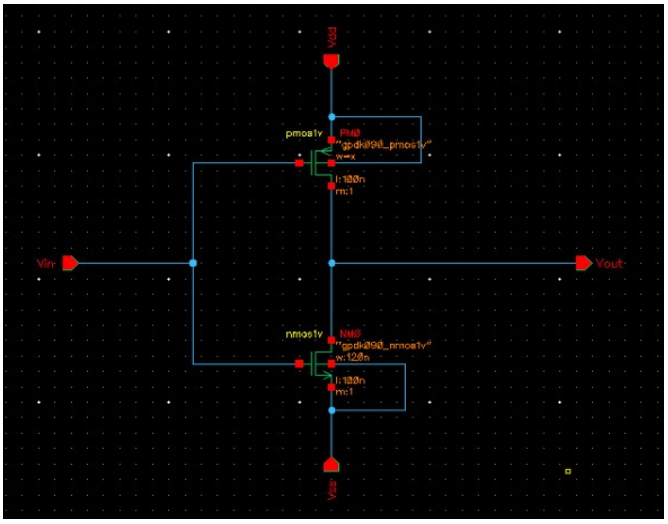

Fig - 10 : INVERTER SCHEMATIC

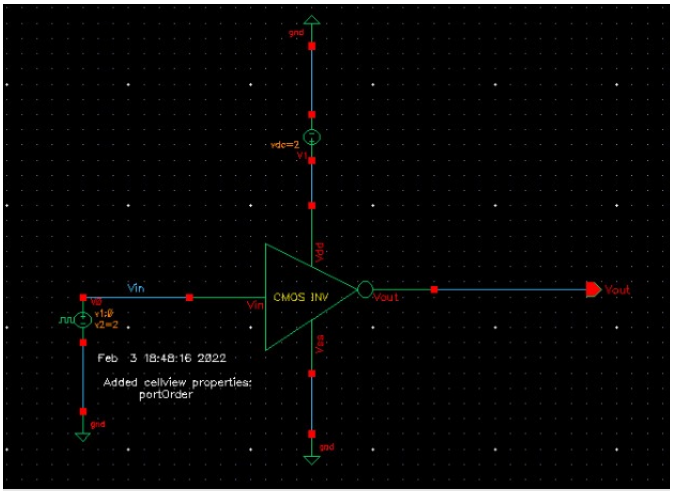

Fig - 11 : INVERTER TEST

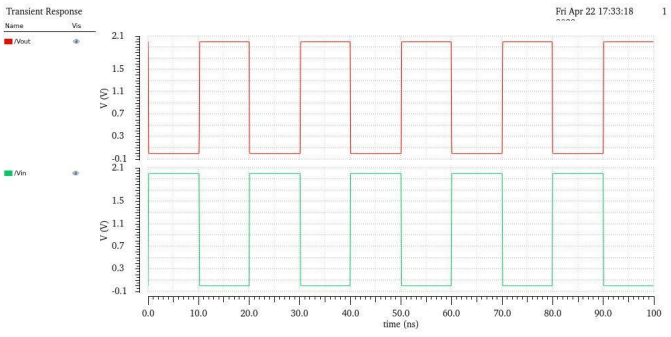

Fig - 12 : INVERTER OUTPUT

2X1 MUX :

Here in this project2x1 mux is used. 2x1 mux means it consists of 2 inputs, 1 select line and 1 outputs. In this mux we will get the output based on the select line if the input is 0 then we will get the first output. Whereas if the output is 1 then we will get the second output. We have implemented this mux by using the transmission gate logic. The mux
schematic is shown in fig - 13, the mux schematic test is shown in fig-14 and the main part which is mux output is shown in fig-15. And the specifications which we have used is the mux schematic while designing is listed below.

Length of PMOS → 240n M
Length of NMOS → 120N M

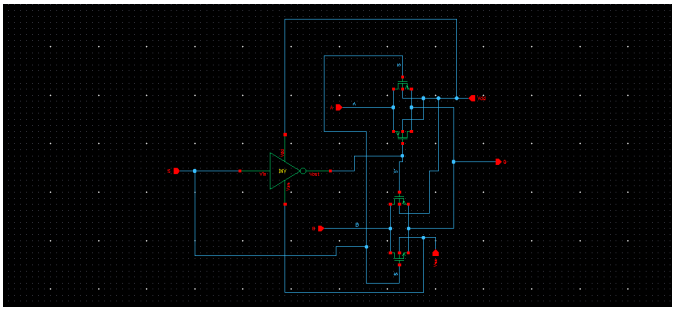

Fig - 13 : 2x1 MUX SCHEMATIC

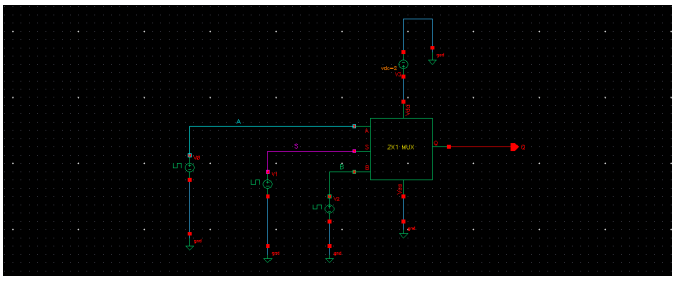

Fig - 14 : 2x1 MUX TEST

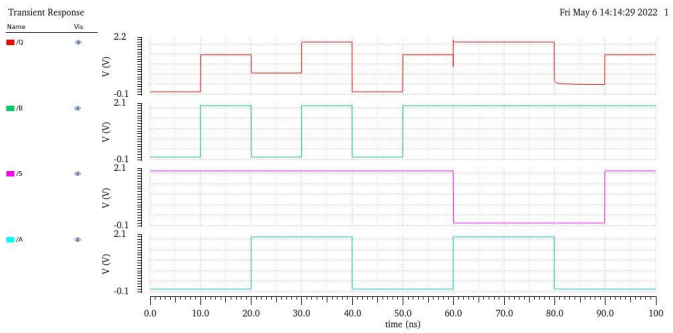

Fig - 15: 2x1 MUX OUTPUT

YET TO BE IMPLEMENTED :

We need to yet implement the counter and comparator. Counter is used for the counting purpose whereas the comparator is used for the comparing. So comparator will give the final output by comparing the bits. So it will provide us the unique id.

CHALLENGES FACED :

- During this project the challenges which we have faced during this project is listed below.
    - While implementing the xor gate we have faced some challenges like not getting full swing…etc.
    - As we known already we don't get the full swing for xor gate. So, by changing the sizing we have rectified this problem.
    - The same challenge is faced while designing the nor gate.
    - While designing the final design we have got the some of the errors we have rectified it successfully.
    - We have failed to implement the comparator and counter.

REFERENCES :

Our reference paper is;

Transformer PUF : A Highly Flexible Configurable RO PUF Based on FPGA | IEEE Conference Publication | IEEE Xplore