Navin kumar p

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SUMMARY

Seeking a challenging DFT Engineer role to utilize my strong technical skills and knowledge in the field. Eager to contribute my expertise in design for testability and ensure efficient testing processes. A quick learner with a passion for innovation and problem-solving, ready to make a positive impact in the industry.

EDUCATION

Degree	Institute	Year	Score
Class 10th	**Rajavignesh hr sec school**	2018	67.4
Class 12th	**Swami matric hr sec school**	2020	57.83
B. Tech (Electronics & Communication)	**Saranathan Engineering College**	2024	7.4

INTERNSHIPS & PROJECTS

Internship at pricol limited (jan&2024 - march&2024)

- pricol limited `
- working in testing and manufacturing

Project

- Clap switch circuit electronic project (2nd year).
- Public water quality monitoring system (3rd year).
- Solar pannel pv system.

MBIST and Scan Insertion on 2 small designs

Design 1 (Communication Chip):

DFT Implementation for Hierarchical Scan Architecture

- Designed and optimized scan architecture for a hierarchical design with CoreB and multiple CoreA instances.
- Configured internal and external scan chains, optimizing length and compression ratios.
- Achieved 8x compression for CoreA and 10x for CoreB, enhancing test efficiency.
- Focused on scan chain length optimization and compression efficiency for improved testability.

Design 2 (Navigation Chip):

DFT Optimization for High Compression Scan Architecture

- Designed and implemented scan architecture with 106 scan chains, each 420 flops long, achieving an optimized 53x compression ratio.
- Focused on scan chain balancing, test coverage improvement, and compression efficiency to minimize test time and data volume.
- Ensured efficient hierarchical DFT integration for improved testability and fault coverage.

SKILLS

- **Design For Testability**
  - Scan Insertion
  - DRC Analysis during Scan Insertion
  - Scan Compression (EDT)
  - ATPG Pattern Generation in Compressed mode and Bypass Mode
  - Coverage Analysis and Improvement
  - On-Chip Clock Controller
  - Scan Pattern Simulation
  - JTAG and Boundary Scan
  - MBIST Insertion
- **Digital Design**
  - Combinational and Sequential Circuit Design
- **Basics of Static Timing Analysis**

SOFTWARE SKILLS

- Automation Languages: TCL
- Operating Systems: Linux and Windows
- Text Editor: GVIM
- EDA Packages : Tessent (Scan, TestKompress, MBIST), Questa Sim and Design Compilers

DECLARATION:

I do hereby declare that the particulars of information and facts stated above are true, correct, and complete to the best of my knowledge and belief.

Date:

Place: