EE3113/3301/5184: Introduction to VLSI Design

Homework Assignment 3 **Deadline: Wed, 16th Dec 2020**

1. **Impact of Sizing on Performance**

   Design and implement an inverter such that $V_M = V_{DD}/2$ using TSMC 180 nm technology.

   (a) Investigate the impact of scaling factor $S > 1$ on the performance of inverter in (i) no external load, and (ii) $C_L = 20pF$ conditions. Tabulate your results.

   (b) What is the impact of increasing W_p or W_n on t_{pHL} and t_{pLH}? Substantiate your answer by performing simulations and tabulating results.

2. **Ring Oscillator**

   Simulate the transient response of a 7 stage ring oscillator circuit by cascading unit inverters.

   (a) Plot the time response over 10 periods and calculate the frequency of oscillation

   (b) Estimate the propagation delay of the circuit and compare with result in 1(a).

   (c) What is the frequency of oscillation when the inverters are sized up by a factor 'S'? How does the sizing impact the power consumption?

   (d) Suggest a modification to ring oscillator circuit so that a control signal can be used to turn the oscillator *on/off*.

3. **Sizing of Inverters**

   In order to drive a large capacitance ($C_L = 20pF$) from a minimum size gate (with input capacitance $C_i = 10fF$), you decide to introduce a two-staged buffer as shown in Figure 1. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size.

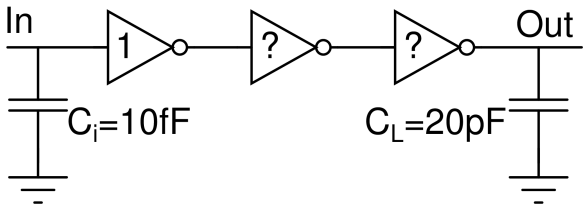

Figure 1

   (a) Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

   (b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

   (c) Describe the advantages and disadvantages of the methods shown in (a) and (b).

   (d) Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V?

4. **CMOS Logic**

   Design a complex CMOS logic gate that implements the function

$$f(A;B;C;D) = \overline{A.(B.(C+D)+C.D)}$$

How do you size the gate to improve it's performance?

5. A particular technology has the following parameters: $V_{th,n} = 0.2\ V$ and $|V_{th,p}| = 0.3\ V$, $R_n = 2\ k\Omega * \mu m$, $R_p = 3\ k\Omega * \mu m$ at $V_{DD} = 1\ V$. Draw the VTC of the gate below with $W_p = W_n = 1\ \mu m$.

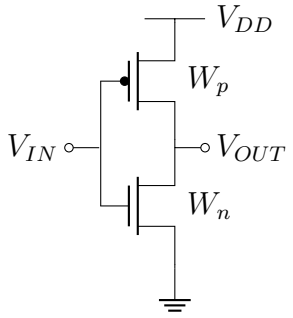

Figure 2

Optional Questions

You do not need to submit the following questions, but it is highly recommended that you analyze and answer them.

6. **Clock Distribution**
Consider the H-tree clock distribution network in Fig. 3. The inverter 1 is a minimum sized inverter with input capacitance of 10 fF. Your goal is to minimize the delay between IN and Clk_1 in the given schematic by choosing appropriate sizes of the inverters. You donot need to worry about the delay in Clk_2, Clk_3 and Clk_4 branches while answering this question. You may assume $\gamma = 1$.

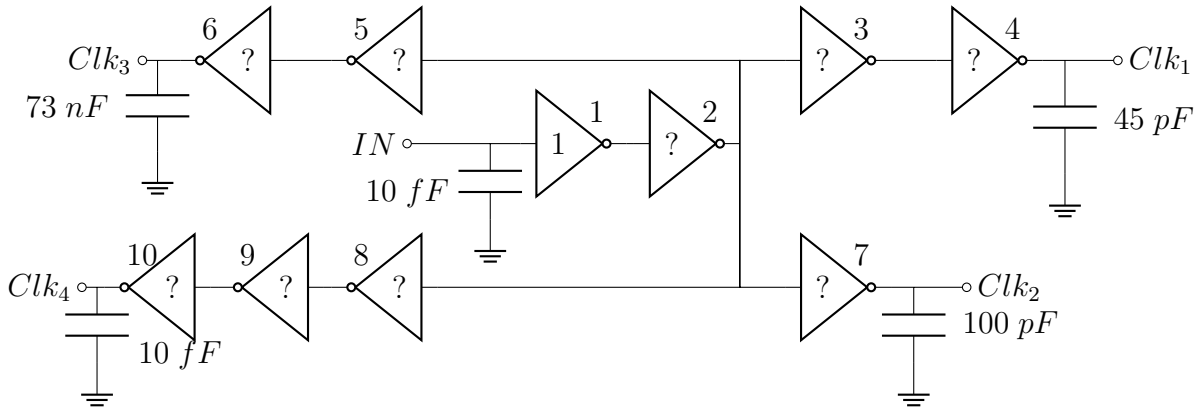

Figure 3

(a) Some inverter sizes may not influence the delay between IN and Clk_1. Clearly mark those with a symbol 'X' in the picture above.

(b) Let the size of remaining inverters be S_i for i^{th} inverter. Write down the expression for time delay between IN and Clk_1.

(c) Determine the sizes of remaining inverters so that the above delay is minimized subject to the constraints specified.

7. **Logical Effort and Gate Sizing**

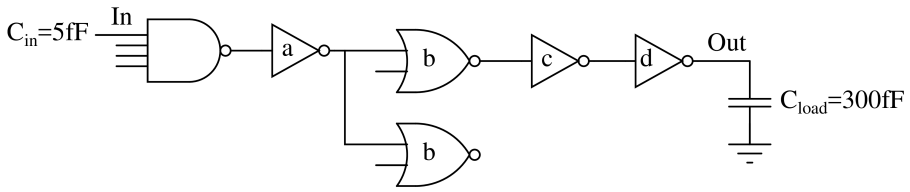

Figure 4

(a) What is the path effort from In to Out?

(b) What effective fanout/stage(EF) minimizes the delay of this chain of gates?

(c) Size the gates to minimize the delay from In to Out.

8. **Scaling trends in VLSI circuits**

(a) Sketch the variation of t_{pHL}, t_{pLH}, and t_p as a function of PMOS/NMOS transistor size ratio β for the generic 0.25 μm technology.

(b) Sketch the functional dependence of $t_p(normalized)$ on effective fanout per stage in a inverter chain in Fig. 8(b). Clearly indicate the effective fanout at which optimal delay is achieved. You may consider $\gamma = 1$, and also account for parasitic overheads.