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Design of QCA-Serial Parallel Multiplier (QSPM) with Energy Dissipation Analysis

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***Abstract* — This letter presents an efficient single-layer serial-parallel multiplier (SPM) in Quantum-dot Cellular Automata (QCA). We have designed a bit-serial adder (BSA) using a fully utilized majority gate (MV), and a modified E-shaped exclusive-OR (E-XOR) gate. The cell-interactive properties of the QCA cell have been utilized to realize the proposed E-XOR gate. This new gate leads the proposed SPM to achieve a reduction in cell count and area by 30% and 19%, 29% and 24%, 30% and 22%, 32% and 39%, and 36% and 46% for 4-, 8-, 16-, 32-, and 64-bit multipliers, respectively. All proposed circuits have been simulated and verified by using QCADesigner with a coherence vector simulation engine. In addition, the average switching and leakage energy dissipation are estimated using QCAPro tool.**

***Index Terms*— Serial-Parallel Multiplier (SPM), Bit-serial adder (BSA), XOR gate, QCADesigner, QCAPro**

I. Introduction

QUANTUM-DOT cellular automata (QCA) is being considered as a promising alternative for complementary metal–oxide–semiconductor (CMOS) technology, in which data is computed in terms of cell polarization and can be transmitted to the next neighboring cells by utilizing Coulomb interaction. Several studies showed that this nanotechnology is proficient in maintaining high device density [1], ultra-low energy competence [2], and fast computing performance [3]. For this reason, in the last few years, QCA based logic circuits have gained a lot of attention.

The elementary component of QCA technology is a QCA cell, a square nanostructure populated with four quantum dots, and a pair of moveable electrons, which are capable to switch the position between adjacent dots [4]. Due to the Coulomb interaction, electrons come across mutual repulsion and located diagonally to each other. More precisely, an individual cell must be in either of the two energy states, known as cell polarization and symbolized as *P=+1 (binary 1)* and *P=-1 (binary 0)*. Besides, in order to execute logical operations and signal propagation, semiconductor QCAs have four-phases of clocking scheme with a 90^0 phase shift to each other [5].

QCA technology not only offers a novel designing pragmatic but also facilitates a revolutionary computing architecture. Up-to-dates, several elementary logic gates have been successfully fabricated and tested [6]-[7]. Moreover, some complex designs including memory unit [8], arithmetic logic unit (ALU) [9]-[15] and microprocessor [16] have been reported. However, the physical implementation of such a design is not still possible because of the complex structural trade-off. More precisely, multilayer design has significant geometric complexity in terms of physical implementation [17]. Hence, a fully utilized-majority voter gate with the single-layer design is considered as the best candidate for physical implementation.

There are very few literatures on QCA based multiplier. Kim and Swartzlander in [12], introduced Wallace and Dadda quasi-modular multiplier, which was the first QCA parallel multiplier. The first serial-parallel multiplier (SPM) based on a multi-layer carry flow adder was reported in [13]. This multi-layer design was realized by utilizing the concept of FIR filter network, and achieved lower latency, area, and cell complexity. Further enhancement was reported in [14] that utilized a similar concept and proposed two different multi-layer SPMs based on two different tile-based adders. Recently, Arani and Rezai in [18] introduced another multi-layer design of a 4-bit SPM that required 264 cells and occupied 0.27 μm^2 of area. However, this design is less fault-tolerant, computationally expensive, and power-hungry, because of the extensive use of half-cell translation inverter gates. Moreover, in [19] Yang and Afrooz reported a coplanar *2x2* array multiplier that required 493 cells and 0.72 μm^2 of area.

In this brief, we have proposed a simplified single layer serial-parallel multiplier (SPM) based on a new bit-serial adder, which is designed by one fully utilized majority gate and one modified E-shape XOR (E-XOR) gate. The proposed module is robust in nature and suitable for designing large QCA circuits. Although the underlying designing principles are based on semiconductor QCAs, the design can be applied to molecular QCAs as well.

II. Proposed Design

A. Bit-serial Adder

The fully-utilized majority gate based full-adder (FA) [13] can be realized by equation 1, which shows that three majority and two inverter gates are required to generate the *Sum*, and one majority gate is required to produce C_{out}.

$$\begin{aligned} Sum &= a_i b_i C_{in} + a_i \overline{b_i}\,\overline{C_{in}} + a_i b_i \overline{C_{in}} + \overline{a_i}\,\overline{b_i} C_{in} \\ &= M(\overline{M}(a_i, b_i, C_{in}), M(a_i, b_i, \overline{C_{in}}), C_{in}) \quad \cdots\cdots\cdots (1) \\ C_{out} &= M(a_1, b_1, C_{in}) \end{aligned}$$

where a_i, b_i are the two input-bit and C_{in} is the carry-in bit.

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However, it makes the design more complex and less effective in terms of implementation. To minimize the designing complexity, we propose a robust and expandable E-shaped three-input exclusive-OR (E-XOR) by modifying a conventional three-input XOR gate [20] and utilizing the explicit cell interactive characteristics. We call it E-XOR, as shown in Fig. 1 (a). It is worth mentioning that the conventional XOR gates [20]-[21] perform well at arbitrary word size, like 1-bit or 2-bits, but for higher bit-design, it cannot achieve the expected optimization. Hence, we modify the XOR gate to achieve higher designing optimization at higher-order design. Moreover, the average dissipated energies by the proposed E-XOR gate are 33.45 meV, 42.56 meV, and 52.45 meV at 0.5 E_k, 1.0 E_k, and 1.5 E_k tunneling energy levels, respectively. The reported one-bit BSA is modified from a one-bit FA by connecting the carry-in and carry-out internally. Fig. 1b shows the schematic diagram and Fig. 1c shows the QCA representation with the carry signal propagation of BSA. By employing the proposed E-XOR gate, the proposed BSA can be realized by only two majority operations, and equation (1) can be written as:

$$Sum = D^{-2}.\left[Mx(a_i,b_i,C_{in})\right] \qquad C_{out} = D^{-2}.\left[M(a_i,b_i,C_{in})\right] \ldots\ldots (2)$$

where $C_{in0} = 0$ $\quad C_{in1} = D^{-4}.C_{out0} = D^{-4}.\left[D^{-2}.\left[M(a_0,b_0,C_{in0})\right]\right]$, and D and Mx indicates the delay and E-XOR operation, respectively.

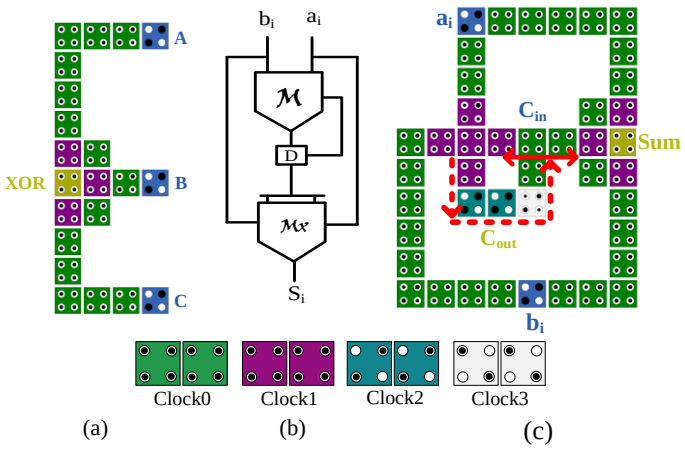

Fig. 1. (a) E-shape 3-input Exclusive-OR gate (b) schematic diagram of the proposed bit-serial adder (BSA), and (c) QCA circuit representation; where different color blocks indicate different clock zone in QCA

B. Serial Parallel Multiplier Design

The proposed multiplier is realized by employing a one-bit BSA block, shown in Fig. 1 (c). The main design utilizes the structure of a finite impulse response (FIR) [22] filter, where the output of the filter is expressed as:

$$y_i = \sum_{j=0}^{n-1} b_j a_{i-j} \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Considering the full-cycle delay (T^{-1}), the relation (3) can be expressed as:

$$y_i = \sum_{j=0}^{n-1} b_j a_{i-j} \;\; = \sum_{j=0}^{n-1} b_j T^{-j} a_i \;\; = \left(\sum_{j=0}^{n-1} b_j T^{-j}\right) a_i \ldots\ldots\ldots (4)$$

The same latency factor is required for both top and bottom lines to maintain the pipeline structure, as shown in Fig. 2. By applying the $T^{-\frac{1}{2}}$ delay factor to every unit, the equation (4) can be written as:

$$T^{-\frac{1}{2}}\left(b_{n-1}T^{-\frac{3}{2}(n-1)} + T^{-\frac{1}{2}}\left(b_{n-2}T^{-\frac{3}{2}(n-2)} + \ldots\ldots + T^{-\frac{1}{2}}\left(b_0T^0\right)\right)\right)a_i$$
$$= T^{-\frac{n}{2}}b_{n-1}T^{-(n-1)}a_i + T^{-\frac{n}{2}}b_{n-2}T^{-(n-2)}a_i + \ldots\ldots + T^{-\frac{n}{2}}b_0a_i$$
$$= T^{-\frac{n}{2}}\left(\sum_{j=0}^{n-1} b_jT^{-j}\right)a_i \quad = T^{-\frac{n}{2}}y_i \qquad \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

The above correlations can be deployed to an un-signed SPM. The single-bit multiplication can be achieved by a one-bit FA and an "AND" gate. The carry propagation handling is the basic difference between the multiplication network and the FIR filter network. The internal carry propagation is used in FIR network, whereas separate carry flows are required for the multiplication network; therefore, proper latency adjustment is needed to realize the multiplication network.

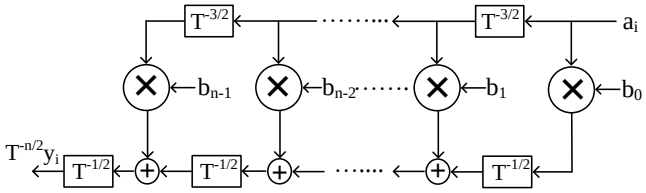

Fig. 2. Pipelined FIR filter network

Now let us assume the multiplier (a_i), multiplicand (b_i), the product of the multiplication (P_i) at the i^{th} position, and the sum (S_{ij}) and carry-out (C_{ij}) of the FA at the i^{th} time and the j^{th} position, where $0 \le i \le 2n\text{-}1$ and $0 \le j \le n\text{-}1$. We also assume that the sum and carry-out generation both requires at least $T^{-\frac{1}{2}}$ delay. Then the representation becomes:

$$\left(S_{ij},C_{ij}\right) = Add\left(b_jT^{-\frac{3}{2}j}a_i, T^{-\frac{1}{2}}S_{i(j-1)}, T^{-1}C_{ij}\right)$$
$$= Add\left(b_ja_{i-\frac{3}{2}j}, S_{\left(i-\frac{1}{2}\right)(j-1)}, C_{(i-1)j}\right) \qquad \ldots\ldots\ldots\ldots\ldots (6)$$

Using a one-clock-cycle self-feedback loop, Fig. 2 can be restructured in Fig. 3 to optimize the output latency.

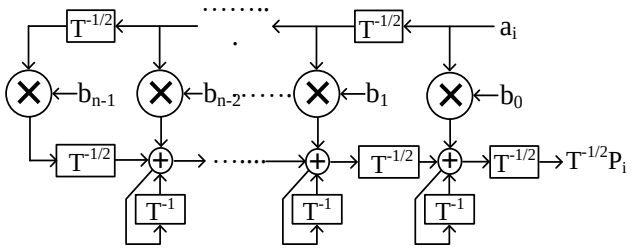

Fig. 3. Representation of FIR filter network for QCA.

According to the QCA clocking scheme, one clock cycle equal to four clock zone, and each clock zone equal to a 0.25 clock delay denoted as $D^{-1} = Z^{-1/4}$ and $D^{-4} = Z^{-1}$. Considering that a logical "AND" operation requires D^{-1} clock delay, and the carry-out and sum of an FA require only two clock zone (D^{-2})

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delay. Normally, the wire does not require any clock delay; however, depending on the wire length, some clock delay is introduced. For synchronizing the operation, the top and bottom-line signals are delayed by one clock cycle. Finally, the QCA equivalent SPM network is presented in Fig. 4.

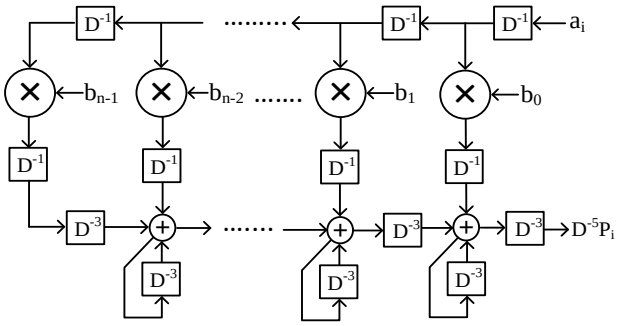
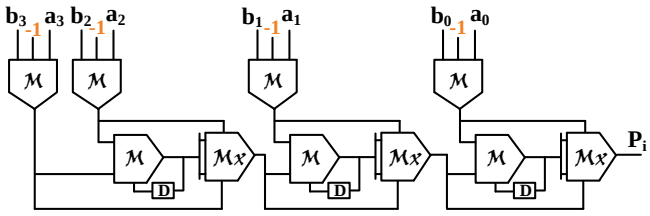
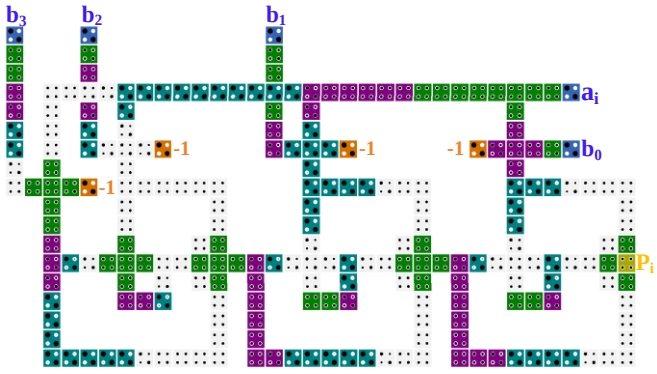


Fig. 4. Proposed SPM network for QCA

To implement the proposed multiplier network, three clock zone feedback loops is used to connect the carry-in and carry-out internally. Figs. 5a and 5b represent the schematic block diagram and QCA circuit design of 4-bit SPM, respectively. Here, a_i is the serial input, and the serial product P_i is generated after 1.25 clock cycle.



(a)



(b)

Fig. 5. Proposed SPM (a) schematic QCA representation, (b) simulated circuit layout

III. Energy Dissipation Analysis

Energy dissipation is one of the significant factors to evaluate the designing efficiency of an electronic device. For QCA circuit, the upper bound power estimation model [23] is the most popular power approximation model, and QCAPro [24] is the most accustomed power estimation tool. In this brief, power dissipation analysis is done by employing the QCAPro tool. Assumed that all the QCA cells dissipate the same amount of power; so, the total dissipated power can be expressed as:

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right] = P_1 + P_2 \quad \ldots\ldots\ldots\ldots (7)$$

Here, $\vec{\lambda}$ *and* $\vec{\Gamma}$ are the three-dimensional energy vectors that modeled the QCA cell state. In particular, Coherence vector $\vec{\lambda} = (\lambda_x, \lambda_y, \lambda_z)$ indicates the current state of a cell, and the state energy vector $\vec{\Gamma}$ signifies the steady state of the cell.

Now, considering the time period of [-T, T] the total energy dissipation is estimated as:

$$E_{diss} = \frac{\hbar}{2}\int_{-T}^{T}\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}dt = \frac{\hbar}{2}\left(\left[\vec{\Gamma}.\vec{\lambda}\right]_{-T}^{T} - \int_{-T}^{T}\vec{\lambda}.\frac{d\vec{\Gamma}}{dt}dt\right) \ldots\ldots\ldots (8)$$

Finally, the power dissipation model can be expressed as:

$$P_{diss} = \frac{E_{diss}}{T_c}\left\langle \frac{\hbar}{2T_c}\vec{\Gamma}_+ \times \left[\frac{\vec{\Gamma}_-}{|\vec{\Gamma}_-|}\tanh\left(\frac{\hbar|\vec{\Gamma}_-|}{k_B T}\right) - \frac{\vec{\Gamma}_+}{|\vec{\Gamma}_+|}\tanh\left(\frac{\hbar|\vec{\Gamma}_+|}{k_B T}\right)\right]\right\rangle \quad (9)$$

Power dissipation of each cell can be estimated by computing the kink energy for the *n-th* combination to the *m-th* combination as expressed below:

$$G_{i-} = \sum_{j\in N(p_i)} E_k f_j p_{j|n} \text{ and } G_{i+} = \sum_{j\in N(p_i)} E_k f_j p_{j|m} \ldots\ldots (10)$$

where, $p_{j|n}$ is the cell polarity of the *j-th* cell for the *n-th* possible input combination. The kink energy (E_k) is the energy gap between two neighboring cells having the opposite polarity. Using the value of clock low (γ_L) and clock high (γ_H) energies, the average leakage and switching power can be estimated as:

$$P_{avg}^{leak} = \frac{1}{2^r}\sum_{i=r+1}^{N} P_{i,n\to m}^{leak} \text{ and } P_{avg}^{switch} = \frac{1}{2^r}\sum_{i=r+1}^{N} P_{i,n\to m}^{switch} \ldots. (11)$$

In this paper, we use QCAPro tool to approximate the average switching and leakage energy dissipation at different tunneling energy levels. Table 1 shows energy dissipation data for the different word length of the proposed SPM's. More precisely, the proposed 4-bit SPM dissipates 135.08, 171.37 and 217.98 meV at *0.5 E_k, 1.0 E_k,* and *1.5 E_k,* respectively. Fig. 6 illustrates the thermal hotspots of the proposed 4-bit SPM at *0.5 E_k*; where the dark cell indicates higher energy dissipated cells.

Fig. 6. Thermal hotspots of the 4-bit SPM at 0.5 E_k. All possible switching combinations were applied to approximate the energy dissipation.

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Table I: Energy Consumption Analysis of Different Multipliers at Different Tunneling Energy Level at temperature *2K*

Multiplier bit size	Leakage energy dissipation (meV)			Switching energy dissipation (meV)			Average energy dissipation (meV)		
	0.5 E_k	*1.0 E_k*	*1.5 E_k*	*0.5 E_k*	*1.0 E_k*	*1.5 E_k*	*0.5 E_k*	*1.0 E_k*	*1.5 E_k*
4-bit	25.48	77.56	138.52	109.06	93.81	79.46	107.21	138.99	177.89
8-bit	163.10	495.89	887.41	827.85	714.66	606.98	262.85	390.29	539.12
16-bit	371.19	1126.62	2009.47	1810.25	1555.83	1317.84	224.59	277.58	345.92
32-bit	858.49	2595.26	4615.09	4016.55	3441.74	2909.99	172.70	215.44	270.50
64-bit	1985.5	5978.4	10599.3	8911.85	7613.65	6425.71	281.43	462.71	674.74

IV. Simulation Results and Comparisons

All proposed circuits have been realized using QCADesigner [25] using Coherence-Vector engine, Table II illustrates a brief description of the Coherence vector simulation parameters. The simulated input-output waveform of the proposed 4-bit SPM is shown in Fig. 8. Here, the first pair of input/output is marked, and the output is in reverse order and reaches after 1.25 clock cycle.

Table II: Simulation parameters of Coherence vector engine

Parameter	**Value**
Cell Width	18 nm
Cell Hight	18 nm
Relative Permittivity	12.9
Clock High	9.8 e^{-22} J
Clock Low	3.8 e^{-23} J
Clock Amplitude Factor	2
Time Step	1.00 e^{-11} s
Relaxation Time	1.00 e^{-16} s
Simulation Time	80 e^{-12} s
Radius of Effect	80 nm

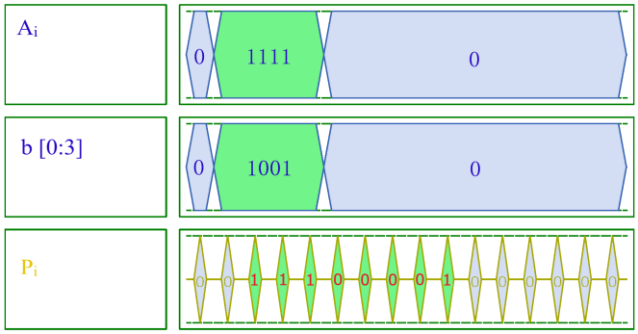

Figure 8: Simulation result of the proposed 4-bit CDM

A comparative performance analysis between the proposed design and existing designs is given in Table III. From Table III, it is observed that the proposed multiplier outperforms all previously reported designs [13] [14] [18] in terms of cell counts and covered area. The reported 4-bit SPM requires 44% fewer cells, and 51% lesser covered area compared to the design in [13]. Moreover, a reduction of 31% in cell count and 24% in the device area have been achieved over the previous design [14]. Besides, the proposed 8-, 16-, 32-, and 64-bit SPM designs have similar improvements over the previous designs [13][14]. It is worth mentioning that, compared to SPM in [18], the proposed SPM achieves only 10% and 13% reductions in the covered area and cell count, respectively; however, the extensive use of half-cell translation inverter gates makes the SPM [18] more vulnerable and computationally expensive.

TABLE III: Comparative Analysis of the Proposed SPM with others

Word	Multiplier	# Cell	Area (μm^2)	Latency (Clock cycle)	Crossover Type
4-bit	Cho et al. [13]	406	0.493	1	Multilayer
	Zhang et al. [14]	329	0.299	1	Multilayer
	Zhang et al. [14]	330	0.319	1.25	Multilayer
	Arani et al. [18]	264	0.27	0.75	Multilayer
	Proposed	229	0.243	1.25	Coplanar
8-bit	Cho et al. [13]	903	0.996	1	Multilayer
	Zhang et al. [14]	749	0.736	1	Multilayer
	Zhang et al. [14]	745	0.673	1.25	Multilayer
	Proposed	529	0.557	1.25	Coplanar
16-bit	Cho et al. [13]	1999	1.969	1	Multilayer
	Zhang et al. [14]	1689	1.693	1	Multilayer
	Zhang et al. [14]	1629	1.624	1.25	Multilayer
	Proposed	1187	1.320	1.25	Coplanar
32-bit	Cho et al. [13]	4575	5.506	1	Multilayer
	Zhang et al. [14]	3965	4.903	1	Multilayer
	Zhang et al. [14]	3589	3.790	1.25	Multilayer
	Proposed	2694	2.995	1.25	Coplanar
64-bit	Cho et al. [13]	11264	15.998	1	Multilayer
	Zhang et al. [14]	10045	14.438	1	Multilayer
	Zhang et al. [14]	8277	9.628	1.25	Multilayer
	Proposed	6384	7.743	1.25	Coplanar

To evaluate the designing efficiency, the most popular cost function known as the generalized cost function for semiconductor QCA is used, where the number of majority gates, inverter gates, circuit delay, and the number wire crossing are considered as an evaluation parameter. The generalized QCA evaluation cost function is described by equation 12 [26]:

$$Cost_{QCA} = (M^{\alpha} + I + C^{\beta}) \times T^{\delta}, \qquad \alpha, \beta, \delta \geq 1 \ldots\ldots\ldots (12)$$

where, *M*, *I*, *C* and *T* indicate the number of majority gates, inverters, wire crossing (coplanar crossing C_{cp} or multilayer crossing C_{ml}), and latency, respectively. The exponential value α, β, and δ are the weight metrics for majority gate, wire crossing, and latency, respectively. By considering the fabrication complexity, the cost of multilayer crossing C_{ml} is considered three times greater than the coplanar crossing C_{cp}. A comparative metric is depicted based on equation 12 as shown in Fig. 9. According to Fig. 9, it is noticed that the proposed SPM (bottom curve) has the least cost compared to the other multipliers. More precisely, the proposed SPM has approximately 70%, 80%, and 90% least design cost compared to previously reported design like CMD-1 [14], CMD-2 [14] and CMD [13] respectively.

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The main reason of achieving such optimization is the use of a smaller number of majority gates and co-planner wire crossing, and inverter-less logic synthesis. By using the bit-serial adder, we have extended the design to 8-, 16-, 32- and 64-bit SPM, and shown the framework to further extend it for an *N*-bit SPM. The cost function of an *N*-bit SPM can be derived from Eqn. (12) as shown below:

$$Cost_N = \left(M_N^{\alpha} + I_N + C_N^{\beta}\right) \times T_N^{\delta} \quad \text{.....(13)}$$

$$where, M_N = 3(N-1)+1, C_N = N-2, T_N = \log_2 \sqrt[4]{32} \text{ and } I_N = 0$$

The proposed SPM has *N*-parallel and one-serial input, and the resultant product is a serial bitstream. The total time requires to complete the *N*-bit multiplication is $\left(2N + \log_2 \sqrt[4]{32}\right)$ clock cycle. Moreover, the covered area of *N*-bit SPM is $\left[(220N - 202) \times \left(358 + 40 \times \text{int}\left(N/11\right)\right) \times 10^{-6}\right]$ μm².

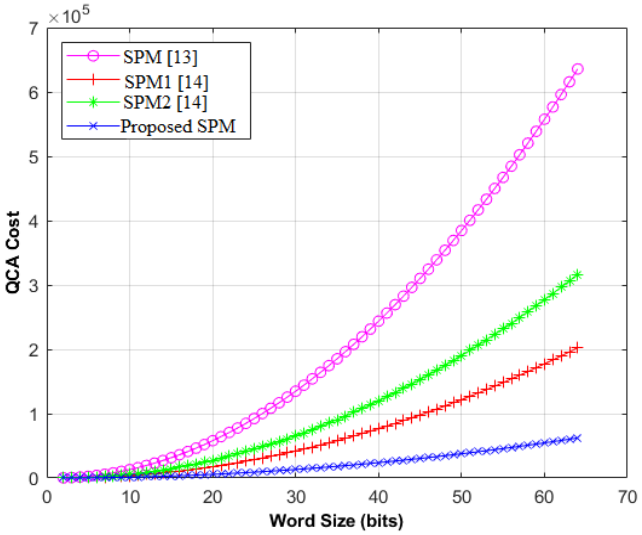

Figure 9. Comparison of QCA SPM with $Cost = (M^{\propto} + I + C^{\beta}) \times T^{\delta}$ considering $\alpha = \beta = \delta = 2$ and the cost of multilayer crossovers, $C_{ml} = 3 \times C_{cp}$.

V. Conclusion

In this brief, a new expandable bit-serial adder (BSA) is presented. To validate the efficiency of the proposed BSA module, different bit size multipliers have been presented and evaluated. The simulation results show that the reported BSA and SPM operate with higher efficiency and achieved a notable improvement in terms of cell count and occupied area. In addition, the proposed SPM has 70% lower design cost over the existing design [14], which demonstrates the advantage of the proposed design.

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