Application Report
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RLC Filter Design for ADC Interface Applications

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ABSTRACT

As high performance Analog-to-Digital Converters (ADCs) continue to improve in their performance, the last stage interface from the final amplifier into the converter inputs becomes a critical element in the system design if the full converter dynamic range is desired. This application note describes the performance and design equations for a simple passive 2nd-order filter used successfully in ADC interface applications.

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1 Introduction

Last-stage interfaces to high-speed converters typically have included a simple RC filter as both a noise bandwidth limiting stage and a way to provide a path (through the capacitor) to absorb the sampling glitch coming out of the converter. This simple interface is proving increasingly inadequate as converter SNRs and input analog bandwidths continue to increase. A simple 2nd order RLC filter can provide both lower noise power bandwidth and more aggressive attenuation of the 3rd-order harmonic distortion at the high end of the analog input range.

2 Filter Topology and Options

Figure 1 shows the basic starting point for the single-ended input to single-ended output version of the filter to be analyzed. A second resistor is included to ground (R_2) over what would normally be considered a standard filter. This resistor provides considerably more design options in the total interface design and will be included in the analysis for this added flexibility. The algebra will easily give results if $R_2 \rightarrow \infty$, so it will certainly be an option to eliminate this resistor later using the more complete development initially.

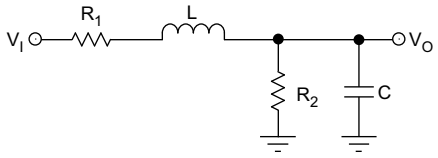

Figure 1. Proposed RLC Passive Filter

In the application where V_I is the output of an op amp and V_O is the input of an ADC, R_2 can provide DC biasing current to the output stage of the amplifier if a DC operating voltage out of the amplifier is required to match the common-mode input voltage of the ADC. This DC current can often improve harmonic distortion by turning what is normally a Class AB output stage in the amplifier to a Class A stage. If the final design requires a DC blocking cap to be inserted at R_1, then R_2 becomes the DC biasing resistor at the input of the ADC. For the circuit of Figure 1, R_2 does cost a DC and AC attenuation in the signal from V_I to V_O – it is intended that the designs using an R_2 will pick values for R_1 and R_2 where this attenuation is < 10%. For the DC level at V_I, R_2 will also drop this down slightly. This can be recovered by adjusting the V_I DC level up accordingly; or, in the case of differential input ADCs where Figure 1 will become a differential filter, R_2 can become the resistor between the legs with no ground connection. This will still give the same filter response for the differential output, but no attenuation for the common-mode DC operating voltage. These options will be explored in more detail, after the filter design discussion.

Equation 1 gives the general Laplace transfer function for the circuit of Figure 1.

$$\frac{V_O}{V_I} = \frac{\frac{1}{LC}}{S^2 + S\left[\frac{1}{R_2C} + \frac{R_1}{L}\right] + \left(1 + \frac{R_1}{R_2}\right)\frac{1}{LC}} \tag{1}$$

If the DC attenuation introduced by R_2 is defined as:

$\alpha = R_2 / (R_1 + R_2)$

and the total DC impedance seen by V_I as:

$R_T = R_1 + R_2$

then, Equation 1 becomes Equation 2.

$$\frac{V_O}{V_I} = \frac{\frac{1}{LC}}{S^2 + S\left[\frac{1}{\alpha R_T C} + \frac{R_T(1-\alpha)}{L}\right] + \left(\frac{1}{\alpha LC}\right)} \tag{2}$$

From Equation 2, the key elements for a 2nd-order filter can be written as shown in Equation 3 and Equation 4.

$$W_O = \sqrt{\frac{1}{\alpha LC}} \tag{3}$$

$$Q = \frac{\sqrt{\frac{1}{\alpha LC}}}{\frac{1}{\alpha R_T C} + \frac{R_T(1-\alpha)}{L}} \tag{4}$$

The W_O and Q completely describe the frequency response for a 2nd-order filter. The intent here is to simply pick an R_T (in order to set a DC standing current out of V_I assuming it is sitting at the required DC bias point for the converter) and α as an acceptable attenuation to take in the signal gain. With those two resistive parts of the design simply selected, Equation 3 and Equation 4 may be solved for the required L and C, given a target W_O and Q.

After some manipulation, Equation 3 and Equation 4 may be used to find the required L, as shown in Equation 5 and Equation 6, while Equation 7 gives the required C once L is determined. Both Equation 5 and Equation 6 are valid solutions for L. Using the higher value for L given by Equation 5 will lead to a lower required C value, while using Equation 6 will lead to a higher C value. Some converters have an input parasitic C that will require Equation 6 to be used to allow a physical implementation.

$$L = \frac{R_T}{2W_O Q}\left[1 + \sqrt{1-(1-\alpha)(2Q)^2}\right] \tag{5}$$

$$L = \frac{R_T}{2W_O Q}\left[1 - \sqrt{1-(1-\alpha)(2Q)^2}\right] \tag{6}$$

Solve Equation 3 for C to get Equation 7, and then substitute the results of either Equation 5 or Equation 6 to get the required C:

$$C = \frac{1}{\alpha L\left(W_O{}^2\right)} \tag{7}$$

A couple of limits to this analysis can be drawn from Equation 5. Specifically, as $\alpha \rightarrow 1$ (meaning $R_2 \rightarrow \infty$), only Equation 5 provides a solution while Equation 6 goes to zero. This shows that the lower L, higher C solution of Equation 6 is created by including R_2 as an added design option. Also, the solution for L can go imaginary for certain combinations of α and Q. It is most useful to pick an α, then solve for the maximum Q allowed, before the terms under the radical in Equation 5 and Equation 6 go negative. Equation 8 shows this constraint on the design.

$$Q < \frac{1}{2}\sqrt{\frac{1}{1-\alpha}} \tag{8}$$

With α typically > 0.9, this does not put much constraint on Q, since we are normally not looking for a peaked response at the output of the filter. For example, at α = 0.9, Q must be < 1.58 in order to get a solution for L in Equation 5 or Equation 6. A design targeting a Q of 1.58 would be getting a frequency response peaking of 4.4dB (see Equation 25). A more typical selection for Q is 0.707, where a maximally flat Butterworth filter shape results. When Q = 0.707, Equation 5 reduces to Equation 9.

$$L = \frac{R_T}{2W_O Q}\left(1 + \sqrt{2\alpha - 1}\right) \tag{9}$$

Again, when $\alpha \rightarrow 1$ (meaning $R_2 \rightarrow \infty$), the more typical design equation for L in Equation 10 is used, where R_T is now only R_1 and Q = 0.707 is assumed.

$$L = \frac{R_T}{W_O Q} \tag{10}$$

3 Design Example

Consider a typical filter design target and apply the design equations developed here to implement a 2nd-order passive RLC filter, using the circuit of Figure 1.

3.1 Conditions and Targets

Assume V_I has a 2.5 V DC component to match up to the converter midrange.

A 5 mA DC bias current out of V_I is acceptable and has been shown to improve distortion for the amplifier driving V_I. This will set R_T = 500 Ω. Allow a 0.915dB attenuation in the signal, which will require α = 0.9.

Exceptional flatness through 10 MHz is desired with a –3dB cutoff at 18 MHz. Since there are added poles in the system, a 0.5dB rolloff at 9 MHz needs to be compensated by the filter. This 0.5dB peaking can be shown (see Equation 27) to require a Q = 0.864. Then, the F_O to hit an 18 MHz F_{-3dB} can be shown (see Equation 26) to be:

$$W_O = (2\pi) * \frac{18\,MHz}{1.176} = (2\pi) * 15.31\,MHz = 2\pi F_O \tag{11}$$

Using Equation 5 (and always remembering to adjust the F_O = 15.3 MHz to radians with a 2π multiplier) gives an L shown in Equation 12.

$$L = \frac{500\ \Omega}{2(2\pi)15.31\,MHz\,(0.864)}\left[1+\sqrt{1-(1-0.9)\left(2(0.864)\right)^2}\right] = 5.5\ \mu H \tag{12}$$

With L resolved, C is provided in Equation 13.

$$C = \frac{1}{0.9(5.5\ \mu H)(2\pi 15.31\,MHz)^2} = 21.7\ pF \tag{13}$$

Looking at the alternative (low L) solution created by having an R_2 in place, and putting values into Equation 6, gives Equation 14:

$$L = \frac{500\ \Omega}{2(2\pi)15.31\,MHz\,(0.864)}\left[1-\sqrt{1-(1-0.9)\left(2(0.864)\right)^2}\right] = 0.49\ \mu H \tag{14}$$

Then, using this alternative value for L in Equation 7, provides Equation 15.

$$C = \frac{1}{0.9(0.49\ \mu H)(2\pi 15.31\,MHz)^2} = 245\ pF \tag{15}$$

Continuing with the design,

$$R_2 = 0.9 * 500\ \Omega = 450\ \Omega \text{ and } R_1 = R_T - R_2 = 500\ \Omega - 450\ \Omega = 50\ \Omega \tag{16}$$

Figure 2 shows the final design with values (Equation 12 and Equation 13 results), while Figure 3 shows the simulated frequency response that results for either combination of L and C.

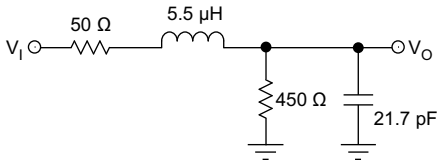

Figure 2. Design Example for 18 MHz Cutoff With 0.5dB Peaking Using Low C Design

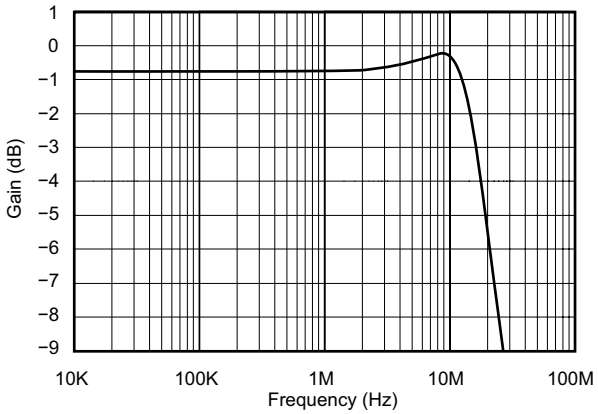

Figure 3. Simulated Filter Performance

This filter response shows the expected 0.9dB loss at low frequencies, a 0.5dB peaking at 9 MHz, and a –3dB frequency at 18 MHz. Aside from providing a noise power bandwidth limit for the noise spectrum at V_I, this filter gives some attenuation for harmonic distortion at the higher end of the desired input frequency range. For instance, if the maximum analog frequency ranges up to 10 MHz, as the input frequency extends above 6 MHz, significant attenuation of the 3rdharmonic will be provided. At 6 MHz input, the 3rd falls at 18 MHz and will see 3dB attenuation from the harmonic power present at V_I. As this input frequency moves up to 10 MHz, this 2ndorder filter provides 12.4dB attenuation for the 3rd-harmonic falling at 30 MHz. This attenuation of harmonics is less effective for 2nd-harmonic terms and of no impact for 3rd-order intermodulation terms where the two carriers are closely spaced. This 2nd-order distortion issue is most easily handled by going differential with both the amplifier and filter circuit.