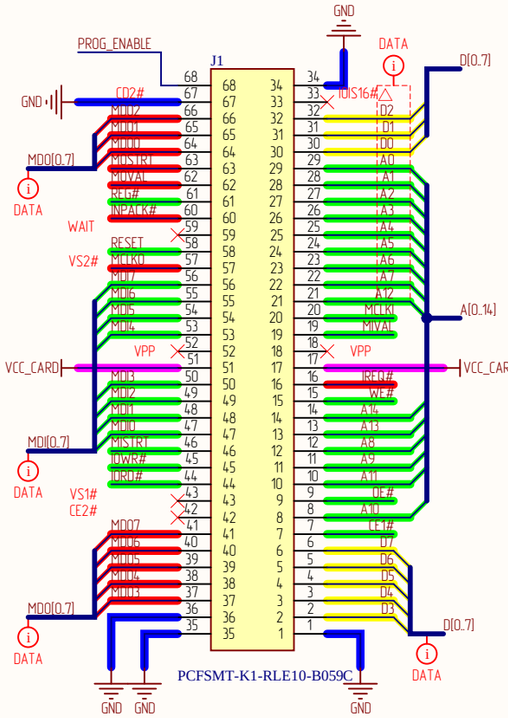
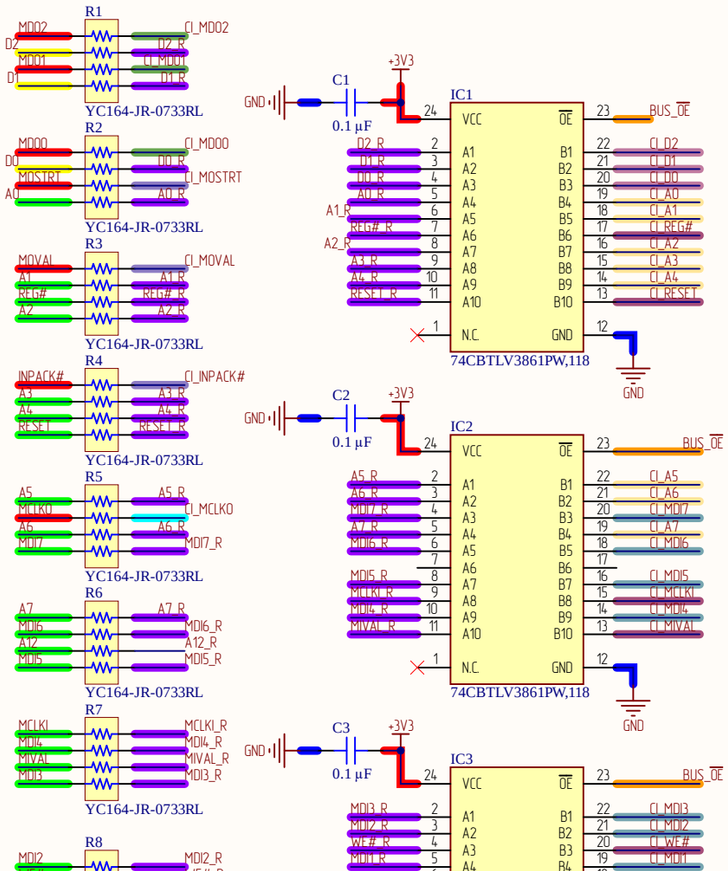
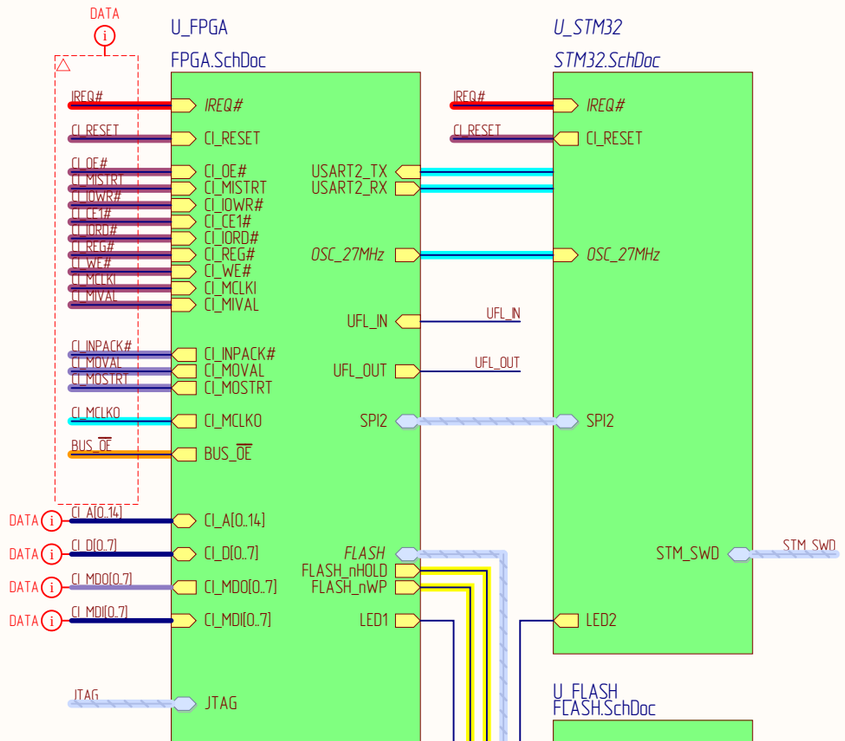
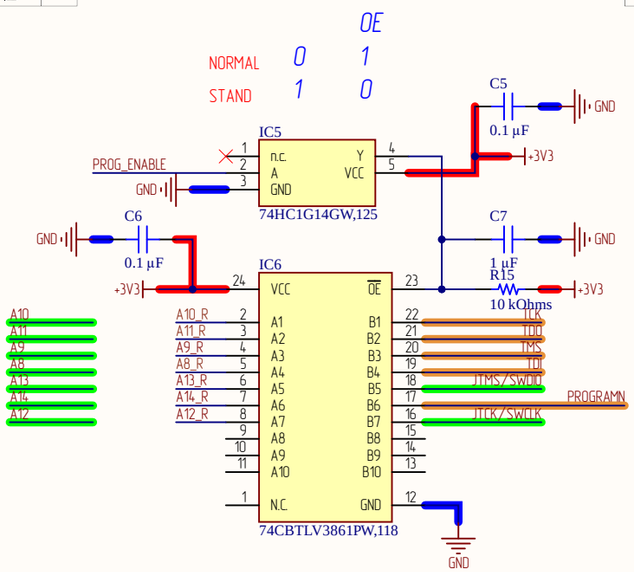
68	GND	
67	CD2#	O
66	MDO2	O
65	MDO1	O
64	MDOO	O
63	MOSTR	O
62	MOVAI	O
61	REG#	I
60	INPACI	O
59	WAIT#	O
58	RESET	I
57	MCLKO	O
56	MDI7	I
55	MDI6	I
54	MDI5	I
53	MDI4	I
52	VPP2	
51	VCC	
50	MDI3	I
49	MDI2	I
48	MDI1	I
47	MDI0	I
46	MISTR	I
45	IOWR#	I
44	IORD#	I
43	VS1#	O
42	CE2#	I
41	MDO7	O
40	MDO6	O
39	MDO5	O
38	MDO4	O
37	MDO3	O
36	CD1#	O
35	GND	

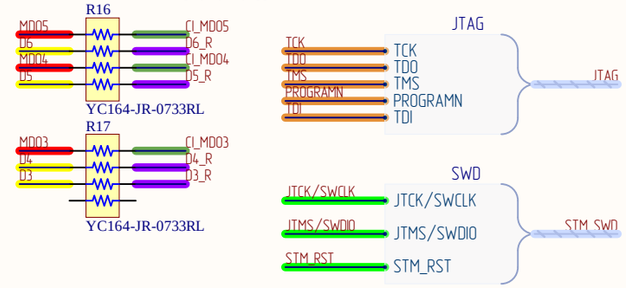


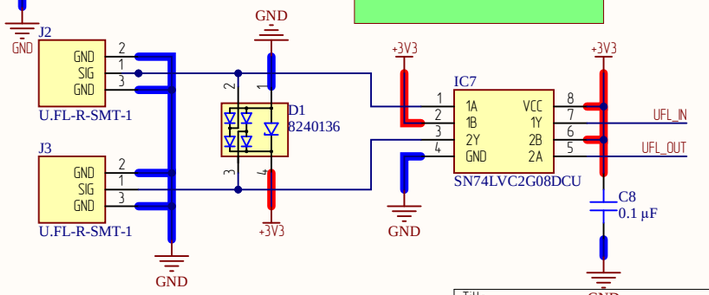
	GND	34
ways	IOIS1	33
I/O	D2	32
I/O	DI	31
I/O	DO	30
I	AO	29
I	AI	28
I	A2	27
I	A3	26
I	A4	25
I	A5	24
I	A6	23
I	A7	22
I	A12	21
I	MCLK	20
I	MIVA	19
tage	VPP1	18
	VCC	17
O	IREQ#	16
I	WE#	15
I	A14	14
I	A13	13
I	A8	12
I	A9	11
I	All	10
I	OE#	9
I	A10	8
I	CE1#	7
I/O	D7	6
I/O	D6	5
I/O	D5	4
I/O	D4	3
I/O	D3	2
	GND	1











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MAIN[6B] CI_MDO[0..7] CI_MDO[0..7]
MAIN[6B] CI_MDI[0..7] CI_MDI[0..7]
MAIN[6B] CI_A[0..14] CI_A[0..14]
MAIN[6B] CI_D[0..7] CI_D[0..7]

CI_MDO[0..7] → CI_MDO0 CI_MDO1 CI_MDO2 CI_MDO3 CI_MDO4 CI_MDO5 CI_MDO6 CI_MDO7

CI_D[0..7] → CI_D0 CI_D1 CI_D2 CI_D3 CI_D4 CI_D5 CI_D6 CI_D7

CI_MDI[0..7] → CI_MDI7 CI_MDI6 CI_MDI5 CI_MDI4 CI_MDI3 CI_MDI2 CI_MDI1 CI_MDI0

CI_A[0..14] → CI_A0 CI_A1 CI_A2 CI_A3 CI_A4 CI_A5 CI_A6 CI_A7 CI_A8 CI_A9 CI_A10 CI_A11 CI_A12 CI_A13 CI_A14

MAIN[6B] BUS_OE BUS_OE
MAIN[6B] CI_MCLKO CI_MCLKO

MAIN[6B] CI_MOVAL CI_MOVAL
MAIN[6B] CI_MOSTRT CI_MOSTRT
MAIN[6B] CI_INPACK# CI_INPACK#

MAIN[6B] CI_MCLKI CI_MCLKI
MAIN[6B] CI_MIVAL CI_MIVAL
MAIN[6A] CI_IORD# CI_IORD#
MAIN[6A] CI_MISTRT CI_MISTRT
MAIN[6A] CI_IOWR# CI_IOWR#
MAIN[6A] CI_CE1# CI_CE1#
MAIN[6A], STM32[1B] CI_RESET CI_RESET
MAIN[6A] CI_REG# CI_REG#
MAIN[6A] CI_WE# CI_WE#
MAIN[6A] CI_OE# CI_OE#

MAIN[6A], STM32[1B] IREQ# IREQ#
MAIN[7B] LED1 LED1

MAIN[7A] USART2_TX USART2_TX
MAIN[7A] USART2_RX USART2_RX

SPI
MAIN[7B], STM32[1B] SPI2 SPI2
CS SPI2.CS
SCK SPI2.SCK
MISO SPI2.MISO
MOSI SPI2.MOSI

SPI
MAIN[7B], FLASH[2B] FLASH FLASH
CS FLASH.CS
SCK FLASH.SCK
MISO FLASH.MISO
MOSI FLASH.MOSI

MAIN[7B], FLASH[2B] FLASH_nHOLD FLASH_nHOLD
MAIN[7B], FLASH[2B] FLASH_nWP FLASH_nWP

JTAG
MAIN[6B] JTAG JTAG
TCK TCK
TDO TDO
TMS TMS
PROGRAMN PROGRAMN
TDI TDI

MAIN[7B] UFL_OUT UFL_OUT
MAIN[7B] UFL_IN UFL_IN

IC9A

CI_A11 A2	PT4A	PT33A/PCLKT1_1	E8
CI_A14 B3	PT4B	PT33B/PCLKC1_1	D8
CI_A8 A3	PT6A	PT35A/PCLKT1_0	C8
CI_A9 A4	PT6B	PT35B/PCLKC1_0	B8
E4	PT9A	PT38A/GR_PCLK1_0	B9
CI_A13 D4	PT9B	PT38B/GR_PCLK1_1	C9
CI_A10 C4	PT11A	PT40A	D9
CI_A12 B4	PT11B	PT40B	E9
E5	PT13A	PT42A	A9
D5	PT13B	PT42B	A10
C5	PT15A	PT44A	B10
CI_A6 B5	PT15B	PT44B	C10
CI_A7 A5	PT18A	PT47A	D10
CI_A5 A6	PT18B	PT47B	E10
E6	PT20A	PT49A	B11
D6	PT20B	PT49B	C11
C6	PT22A	PT51A	D11
CI_A4 B6	PT22B	PT51B	E11
E7	PT24A/GR_PCLK0_1	PT53A	A11 BUS_OE
D7	PT24B/GR_PCLK0_0	PT53B	A12 CI_INPACK#
CI_A2 B7	PT27B/PCLKC0_1	PT56A	B12 CI_MOSTRT
CI_A0 C7	PT27A/PCLKT0_1	PT56B	C12
CI_A3 A7	PT29A/PCLKT0_0	PT58A	D12
CI_A1 A8	PT29B/PCLKC0_0	PT58B	E12
		PT60A	B13
		PT60B	C13
		PT62A	D13
		PT62B	E13
		PT65A	A13 CI_MOVAL
		PT65B	A14 IREQ#
		PT67A	B14 CI_REG#
		PT67B	A15

BANK 0 BANK 1

LFE5U-25F-6BG256C

FLASH_RSV.CS R26 0 Ohms FLASH.CS
FLASH_RSV.SCK R27 0 Ohms FLASH.SCK
FLASH_RSV.MISO R28 0 Ohms FLASH.MISO
FLASH_RSV.MOSI R29 0 Ohms FLASH.MOSI

FLASH_RSV.nHOLD
FLASH_RSV.nWP
FLASH_RSV.SN
R34 0 Ohms R35 0 Ohms R36 0 Ohms

+3V3 R40 4.7 kOhms R41 4.7 kOhms R42 4.7 kOhms

IC9D

T6	PB4A/D7/IO7	PROGRAMN	R9
R6	PB4B/D6/IO6	INITN	T9
R7	PB6A/D5/MISO2/IO5	DONE	P9
P7	PB6B/D4/MOSI2/IO4	CCLK	N9 FLASH.SCK
FLASH_nHOLD N7	PB9A/D3/IO3	CFG_0	N10 CFG0
FLASH_nWP M7	PB9B/D2/IO2	CFG_1	P10 CFG1
FLASH.MISO T7	PB11A/D1/MISO/IO1	CFG_2	R10 CFG2
FLASH.MOSI T8	PB11B/D0/MOSI/IO0	TDI	R11 TDI
SSPI_SN R8	PB13A/SN/CSN	TDO	M10 TDO
P8	PB13B/CS1N	TCK	T10 TCK
M9	PB18A/WRITEN	TMS	T11 TMS
FLASH.CS N8	PB15A/HOLDN/DI/BUSY/CSSPIN/CEN		
M8	PB15B/DOUT/CSON		

LFE5U-25F-6BG256C

+3V3 R30 4.7 kOhms R31 4.7 kOhms R32 4.7 kOhms TP17
PROGRAMN R33 0 Ohms PROGRAMN_RSV

+3V3 R37 4.7 kOhms R38 4.7 kOhms R39 4.7 kOhms
TP18 TP19 TP20 TP21
R43 4.7 kOhms
GND

Table 6.3. Configuration Pins Needed per Programming Mode[1]

Configuration Mode	Bus Size	Dedicated CFG[2:0]	Clock Pin	Clock I/O	Shared Pins	Dedicated Pins
SSPI	1 Bit	001	CCLK	Input	MISO, MOSI, SI, DOUT,	PROGRAMN, INITN, DONE
MSPI[2]	1 Bit	010	MCLK	Output	MISO, MOSI, CSSPIN, DOUT	PROGRAMN, INITN, DONE
	2 Bits				D[1:0], CSSPIN, DOUT	
	4 Bits				D[3:0], CSSPIN, DOUT	
SCM	1 Bit	101	CCLK	Input	DI, DOUT	PROGRAMN, INITN, DONE
SPCM (Parallel)	8 Bits	111	CCLK	Input	D[7:0], DOUT, CSON, BUSY, WRITEN, CSN, CS1N	PROGRAMN, INITN, DONE
JTAG	1 Bit	xxx	TCK	Input	—	TCK, TMS, TDI, TDO

Notes:
1. SN should have 4.7 kΩ pull-up resistor on-board for SSPI.
2. CSSPIN should have 4.7 kΩ pull-up on-board resistor for MSPI.
3. D[7:0] should have 10 kΩ pull-up resistor on-board for SPCM.
4. MOSI and MISO should have 10 kΩ pull-up resistor on-board for MSPI.
5. IO[3:2] should have 10 kΩ pull-up resistor on-board for QUAD MSPI.
6. MCLK should have a 1 kΩ pull-up. See Figure 6.1.

+3V3 +3V3 +3V3
DNC R44 R45 4.7 kOhms DNC R46
CFG0 CFG1 CFG2
R47 0 Ohms DNC R48 R49 0 Ohms
GND GND GND

IC9C

B16	PR2A		
B15	PR2B		
C14	PR2C		
D14	PR2D		
C16	PR5A	PR26A/PCLKT3_1	L16 27MHz
C15	PR5B	PR26B/PCLKC3_1	L15
E14	PR5C	PR26C/PCLKT3_0	M16
F14	PR5D	PR26D/PCLKC3_0	M15
	PR8A	PR29A/GR_PCLK3_0	K13
LED1 D16	PR8B	PR29B	K12
E15	PR8C	PR29C/GR_PCLK3_1	L13
F13	PR8D	PR29D	L12
F12	PR11A	PR32A	N16 FLASH_RSV.nWP
G12	PR11B	PR32B	P15
G13	PR11C	PR32C	L14
SPI2.SCK F15	PR11D	PR32D	M14
SPI2.CS E16	PR14A	PR35A	P16 FLASH_RSV.SN
SPI2.MISO F16	PR14B	PR35B	R16 FLASH_RSV.nHOLD
SPI2.MOSI G15	PR14C	PR35D	N14
G14	PR14D	PR35C	M13
H14	PR17A	PR38A	N13
H12	PR17B	PR38B	P14
H13	PR17C	PR38C	R15 FLASH_RSV.MOSI
J13	PR17D	PR38D	T15 PROGRAMN_RSV
J12	PR20A/GR_PCLK2_1	PR41A	P13
G16	PR20B	PR41B	R14
H15	PR20C/GR_PCLK2_1	PR41C	R13 FLASH_RSV.CS
J14	PR20D	PR41D	T14 FLASH_RSV.SCK
K14	PR23A/PCLKT2_1	PR44A	R12
UFL_OUT J16	PR23B/PCLKC2_1	PR44B	T13 FLASH_RSV.MISO
J15	PR23C/PCLKT2_0	PR44C	M12
UFL_IN K16	PR23D/PCLKC2_0	PR44D	N12
K15		PR47A	M11
		PR47B	N11
		PR47C/LRC_GPLLOT_IN	P11
		PR47D/LRC_GPLLOC_IN	P12 PLL_27MHz

BANK 2 BANK 3

LFE5U-25F-6BG256C

IC9B

CI_RESET B1	PL2A		
B2	PL2B		
C3	PL2C		
D3	PL2D	PL26A/PCLKT6_1	L1 CI_MCLKO
		PL26B/PCLKC6_1	L2 CI_MISTRT
CI_MDI7 C1	PL5A	PL26C/PCLKT6_0	M1 CI_MCLKI
CI_MDI6 C2	PL5B	PL26D/PCLKC6_0	M2 CI_IOWR#
E3	PL5C		
F3	PL5D	PL29A/GR_PCLK6_0	K4
		PL29B	K5
CI_MDI5 D1	PL8A	PL29C/GR_PCLK6_1	L4
E2	PL8B	PL29D	L5
F4	PL8C		
F5	PL8D	PL32A	N1 CI_MDO2
		PL32B	P2 CI_MDO0
G5	PL11A	PL32C	L3
G4	PL11B	PL32D	M3
CI_MIVAL F2	PL11C		
CI_MDI4 E1	PL11D	PL35A	P1 CI_MDO1
		PL35B	R1 CI_MDO7
CI_MDI3 F1	PL14A	PL35C	M4
CI_MDI2 G2	PL14B	PL35D	N3 CI_D2
G3	PL14C		
H3	PL14D	PL38A	N4 CI_D1
		PL38B	P3 CI_MDO4
H5	PL17A	PL38C	R2 CI_MDO6
H4	PL17B	PL38D	T2 CI_MDO5
J4	PL17C		
J5	PL17D	PL41A	P4 CI_D3
		PL41B	R3 CI_D7
CI_WE# G1	PL20A/GR_PCLK_7_1	PL41C	R4 CI_D5
CI_MDI1 H2	PL20B	PL41D	T3 CI_MDO3
J3	PL20C/GR_PCLK7_0		
K3	PL20D	PL44A	R5 CI_D4
		PL44B	T4 CI_D6
CI_IORD# J1	PL23A/PCLKT7_1	PL44C	M5
CI_MDI0 J2	PL23B/PCLKC7_1	PL44D	N5 CI_D0
CI_CE1# K1	PL23C/PCLKT7_0		
CI_OE# K2	PL23D/PCLKC7_0	PL47A	M6
		PL47B	N6
		PL47C/LLC_GPLLOT_IN	P6
		PL47D/LLC_GPLLOC_IN	P5

BANK 7 BANK 6

LFE5U-25F-6BG256C

+3V3
R50 4.7 kOhms R51 1.1 kOhms R52 10 kOhms R53 10 kOhms R54 10 kOhms R55 10 kOhms
FLASH.CS
FLASH.SCK
FLASH.MISO
FLASH.MOSI
FLASH_nHOLD
FLASH_nWP

R56 33 Ohms PLL_27MHz
R57 33 Ohms STM_27MHz OSC_27MHz
R58 33 Ohms 27MHz
+3V3
Y1 VDD OUT GND TRI 27 MHz
C37 0.1 µ
GND GND

ЗАМЕНИТЬ НА 8 пиновый

JTAG MODE
J6
TCK TDO TMS PROGRAMN TDI
+3V3 +5V
PBD2-10
GND

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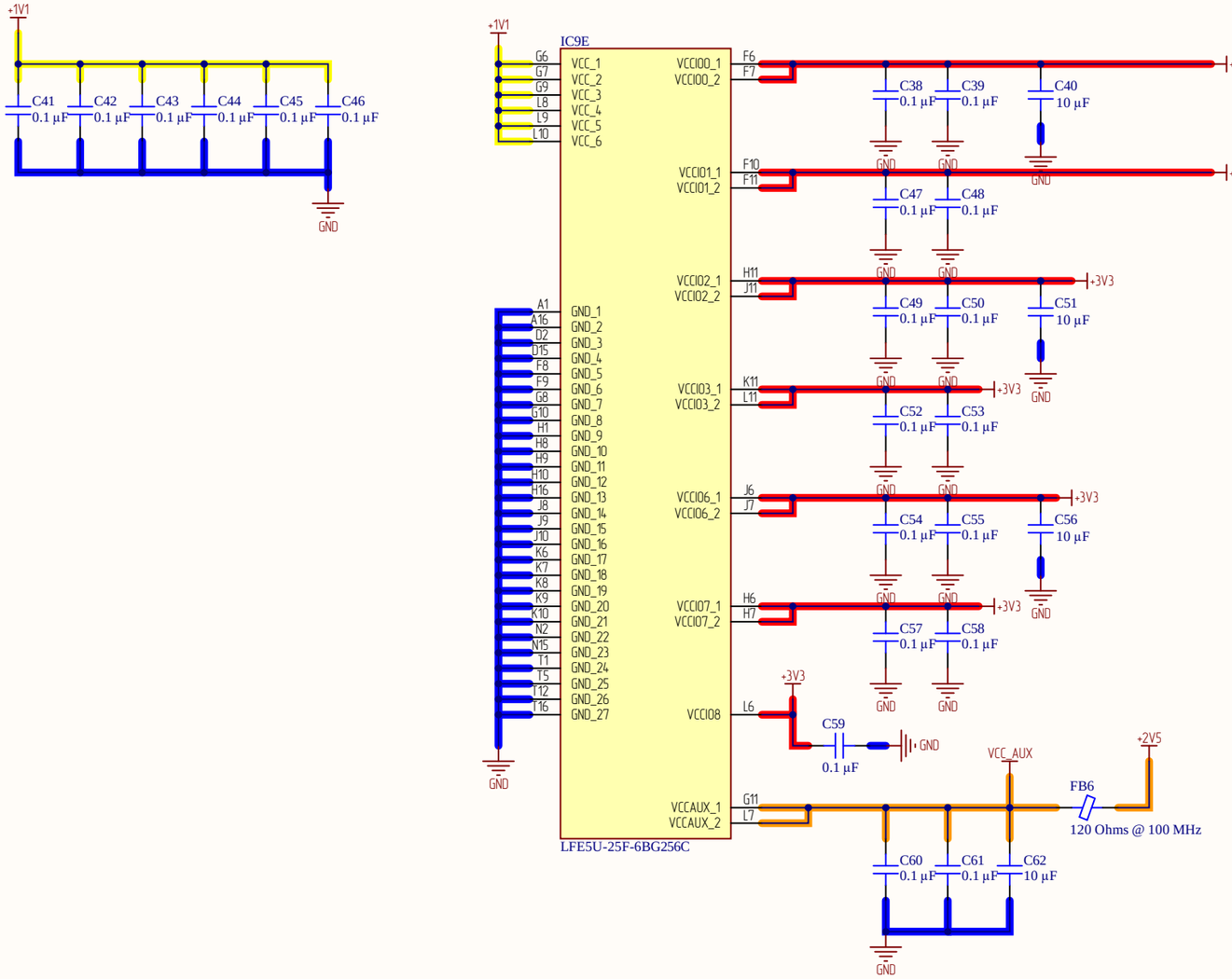

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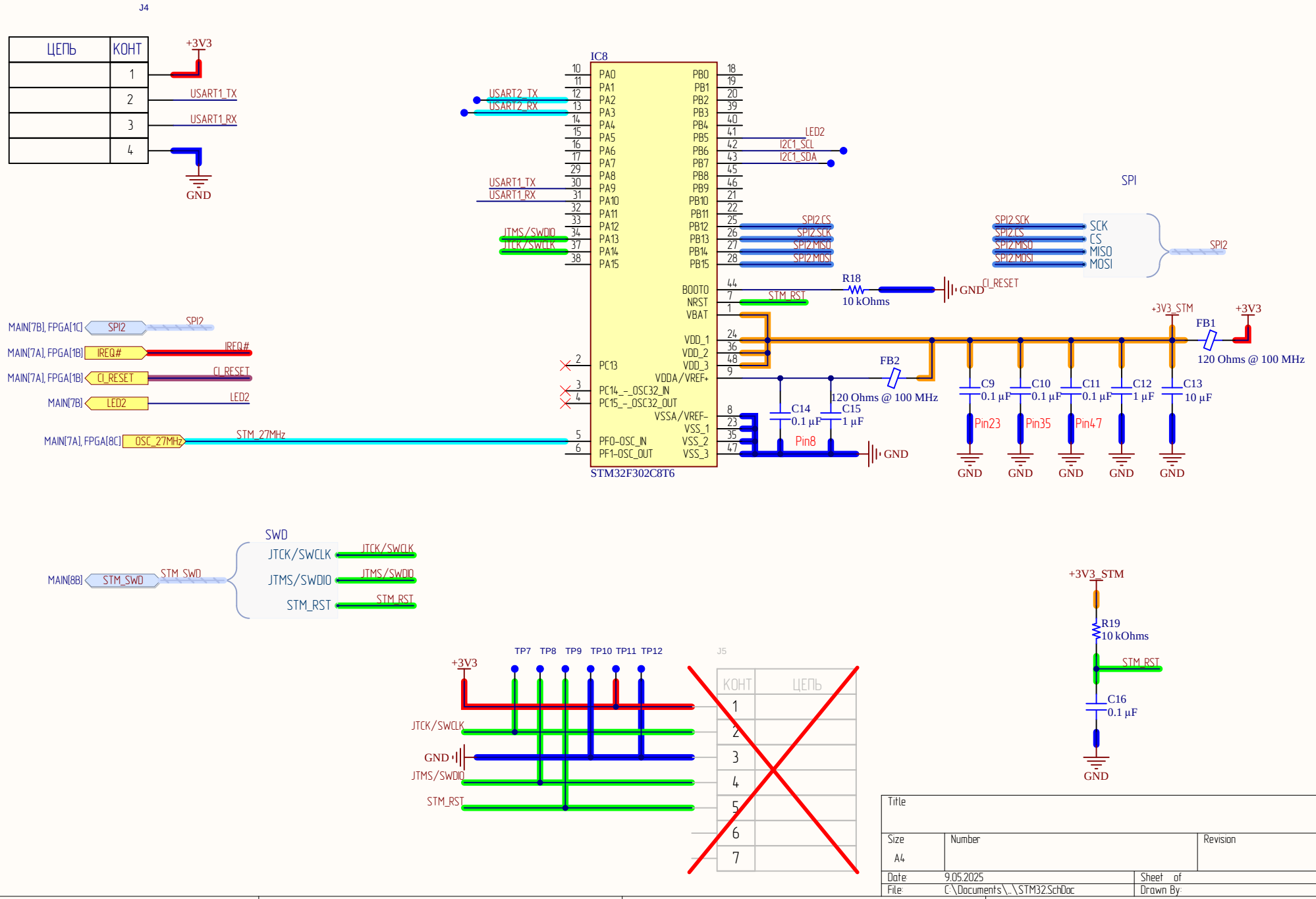
J4
ЦЕПЬ
КОНТ
1
2
3
4
+3V3
USART1_TX
USART1_RX
GND
IC8
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13
PA14
PA15
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
BOOT0
NRST
VBAT
PC13
PC14_-_OSC32_IN
PC15_-_OSC32_OUT
PF0-OSC_IN
PF1-OSC_OUT
VDD_1
VDD_2
VDD_3
VDDA/VREF+
VSSA/VREF-
VSS_1
VSS_2
VSS_3
USART2_TX
USART2_RX
LED2
I2C1_SCL
I2C1_SDA
JTMS/SWDIO
JTCK/SWCLK
SPI2.CS
SPI2.SCK
SPI2.MISO
SPI2.MOSI
STM_RST
R18
10 kOhms
CI_RESET
SPI
SCK
CS
MISO
MOSI
SPI2
MAIN[7B], FPGA[1C]
MAIN[7A], FPGA[1B]
IREQ#
MAIN[7B]
LED2
MAIN[7A], FPGA[8C]
OSC_27MHz
STM_27MHz
STM32F302C8T6
+3V3_STM
+3V3
FB1
120 Ohms @ 100 MHz
FB2
C9
0.1 µF
C10
0.1 µF
C11
0.1 µF
C12
1 µF
C13
10 µF
C14
0.1 µF
C15
1 µF
Pin8
Pin23
Pin35
Pin47
GND
SWD
MAIN[8B]
STM_SWD
JTCK/SWCLK
JTMS/SWDIO
STM_RST
TP7
TP8
TP9
TP10
TP11
TP12
J5
КОНТ
ЦЕПЬ
R19
10 kOhms
C16
0.1 µF
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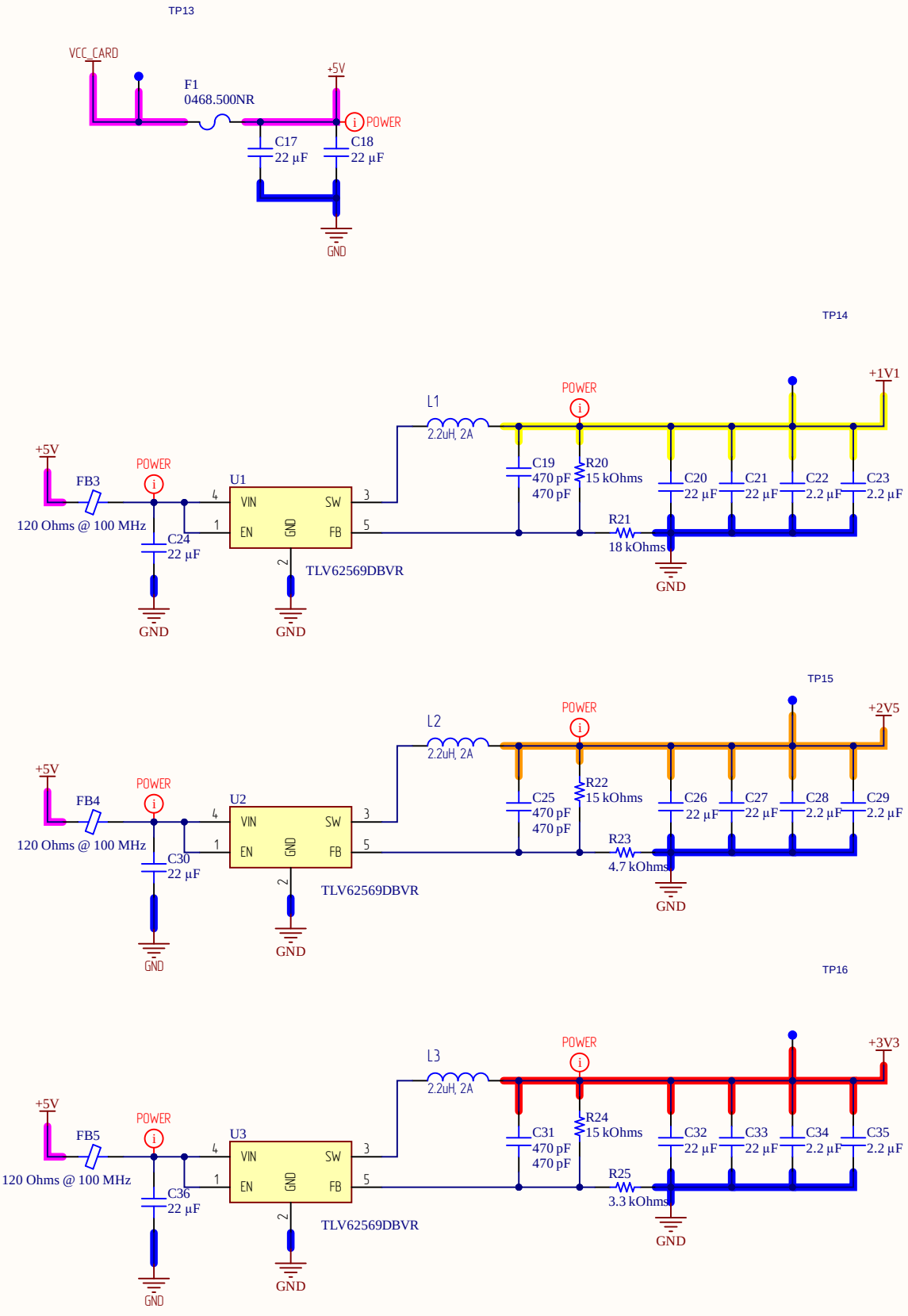

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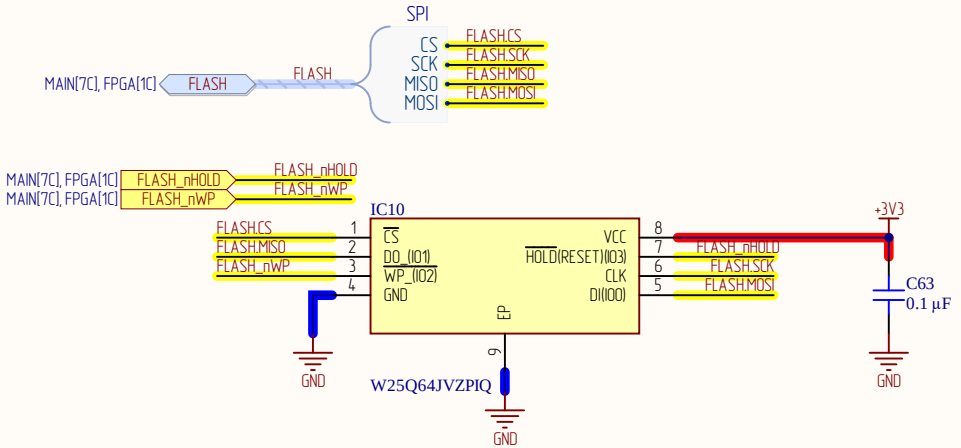

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rev.1 first release

rev.1.1 SCHEMATIC

signal BUS_OE to U1 pin 83 (R30, R31, R33, R34, R35 убраны)

пины ПЛИС 94, 96, 97 убраны DNP резисторы, 0 Ohm подключены к GND напрямую

убраны разъемы J2 (программирования флэш), J4 (AS mode ПЛИС)

R8 корректно подключен с пина 4 IC2 на GND (был на VCC)

RN1 – RN12 заменены с 330 Ом на 33 Ома

R6, R7 убраны (поддержка STM32F1 отсутствует)

LED1 переключен на ПЛИС

X1 -> заменен на J2 -> заменен на PBS2-6

VPP и VCC разделены. Пины 18 и 52 (VPP) отключены от шины питания VCC.

PCB

PCB сжать до 50*75

корректное подключение полигона 3V3 рядом с DCDC

STACKUP Total 0.86mm

Copper 1oz

IMPEDANCE Width 0.15mm – S75 – Imp 68.2(-9%) Standart = 60-90 Ohm

ADD "POWER" class with VIA 0.6/0.3

rev.1.11 STM_RCC_OUT убран с ПЛИС и СТМ, на 5 OSC_IN заеден сигал с генератора у3

TODO разобраться с питанием ПЛИС, лишние домены с DCDC убрать

rev.2.0 Lattice FP caBGA256

recommend	0.45	0.53		
example	0.35	0.5	0.100/0.100	0.4/0.15
current	0.42	0.54	0.125/0.125	0.4/0.2

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