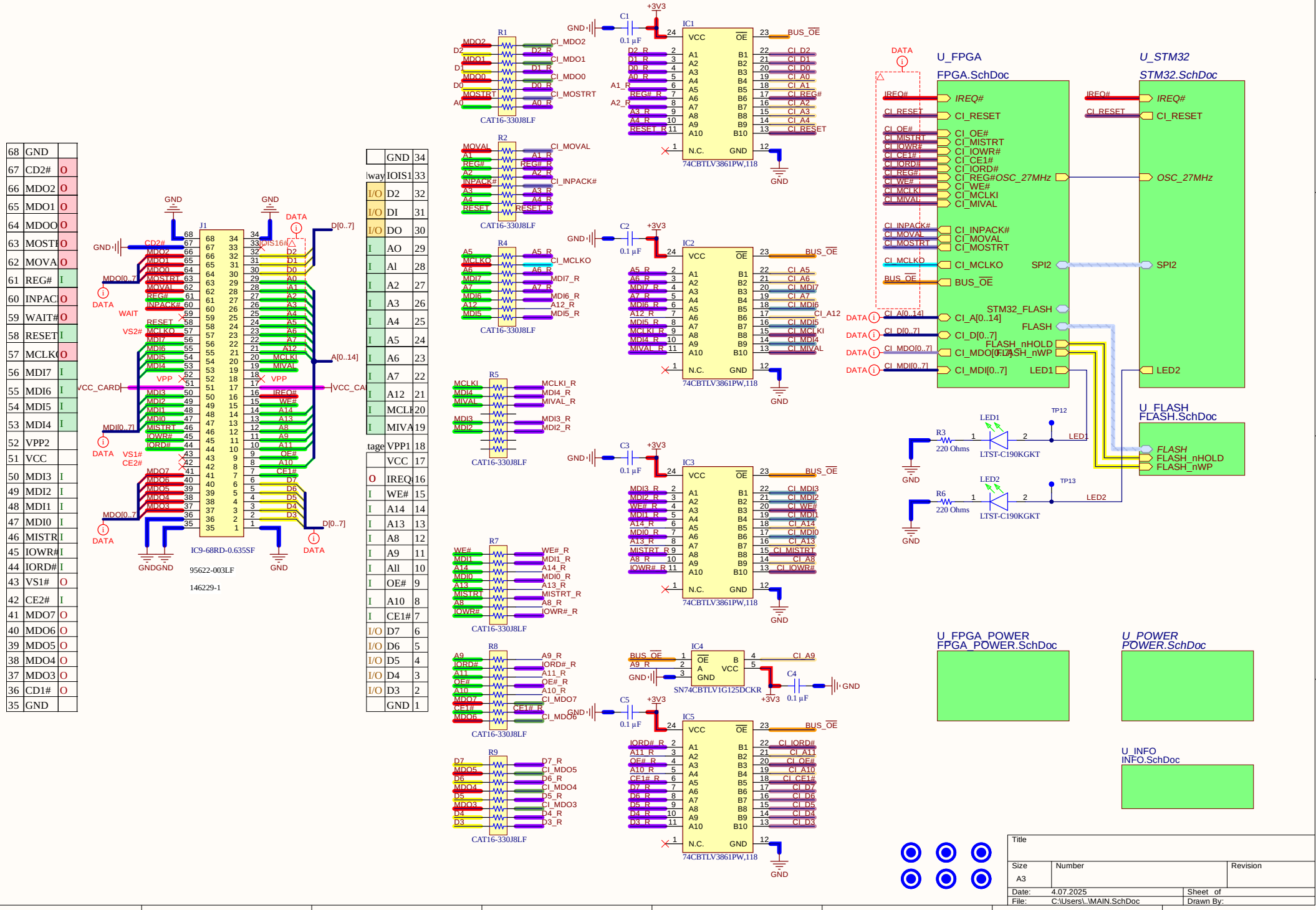
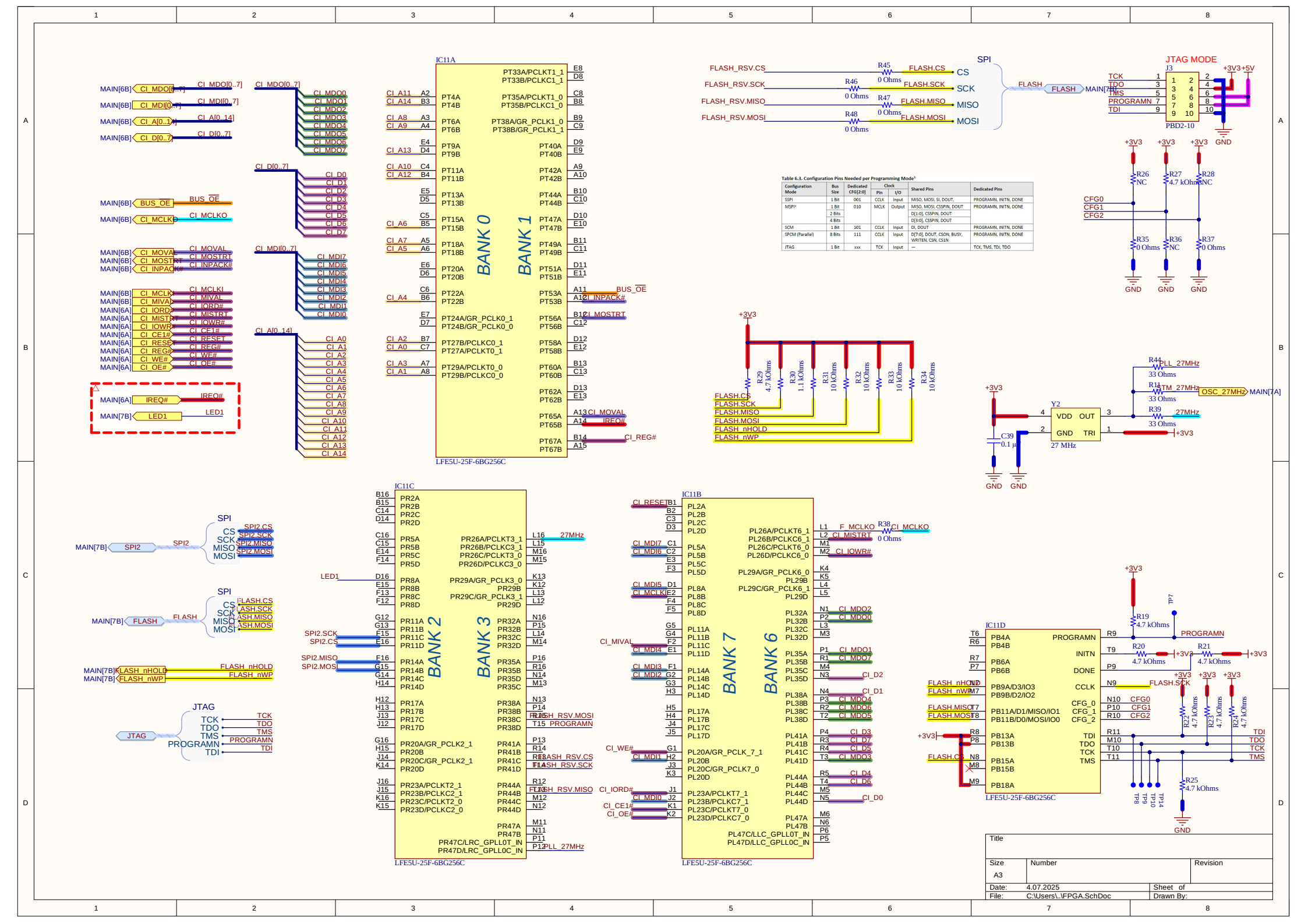
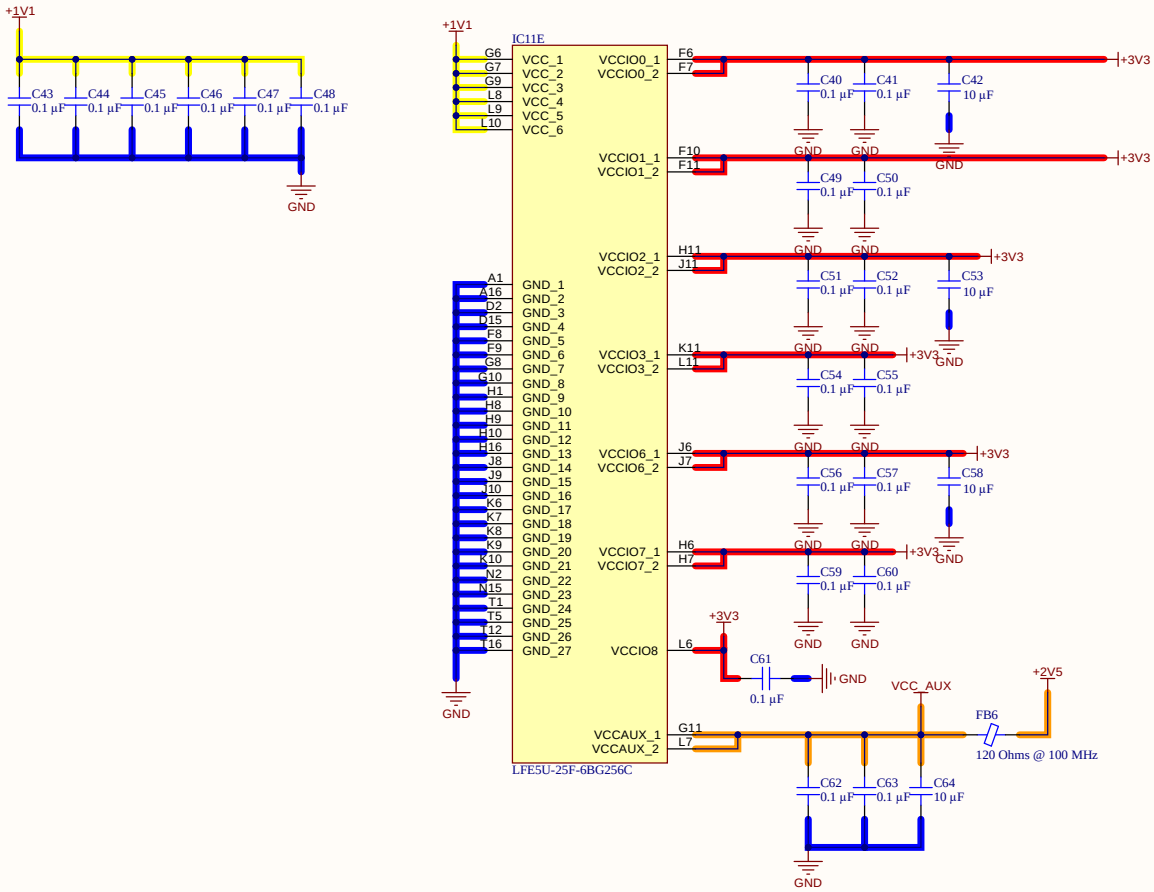

U_FPGA
FPGA.SchDoc
U_STM32
STM32.SchDoc
U_FLASH
FLASH.SchDoc
U_FPGA_POWER
FPGA_POWER.SchDoc
U_POWER
POWER.SchDoc
U_INFO
INFO.SchDoc
IC1
IC2
IC3
IC4
IC5
74CBTLV3861PW,118
SN74CBTLV1G125DCKR
CAT16-330J8LF
IC9-68RD-0.635SF
95622-003LF
146229-1
LTST-C190KGKT
220 Ohms
+3V3
GND
DATA
Title
Size
A3
Number
Revision
Date: 4.07.2025
File: C:\Users\..\MAIN.SchDoc
Sheet of
Drawn By:


IC11A
LFE5U-25F-6BG256C
BANK 0
BANK 1
IC11C
BANK 2
BANK 3
IC11B
BANK 7
BANK 6
IC11D
SPI
JTAG MODE
PBD2-10
FLASH
Table 6.3. Configuration Pins Needed per Programming Mode¹
Configuration Mode
Bus Size
Dedicated CFG[2:0]
Clock
Pin
I/O
Shared Pins
Dedicated Pins
SSPI
MSPI¹
SCM
SPCM (Parallel)
JTAG
CI_MDO[0..7]
CI_MDI[0..7]
CI_A[0..14]
CI_D[0..7]
BUS_OE
CI_MCLKO
CI_MOVAL
CI_MOSTRT
CI_INPACK#
CI_MCLKI
CI_MIVAL
CI_IORD#
CI_MISTRT
CI_IOWR#
CI_CE1#
CI_RESET
CI_REG#
CI_WE#
CI_OE#
IREQ#
LED1
FLASH_RSV.CS
FLASH_RSV.SCK
FLASH_RSV.MISO
FLASH_RSV.MOSI
FLASH.CS
FLASH.SCK
FLASH.MISO
FLASH.MOSI
FLASH_nHOLD
FLASH_nWP
F_MCLKO
CI_MISTRT
CI_IOWR#
CI_MDO2
CI_MDO0
CI_MDO1
CI_MDO7
CI_MDO6
CI_MDO5
CI_MDO4
CI_MDO3
CI_D2
CI_D1
CI_D3
CI_D7
CI_D5
CI_D6
CI_D4
CI_D0
CI_MDI7
CI_MDI6
CI_MDI5
CI_MDI4
CI_MDI3
CI_MDI2
CI_MDI1
CI_MDI0
CI_WE#
CI_IORD#
CI_CE1#
CI_OE#
SPI2.CS
SPI2.SCK
SPI2.MISO
SPI2.MOSI
TCK
TDO
TMS
PROGRAMN
TDI
PLL_27MHz
TM_27MHz
OSC_27MHz
27MHz
MAIN[7A]
MAIN[7B]
MAIN[6A]
MAIN[6B]
Title
Size
A3
Number
Revision
Date:
4.07.2025
Sheet of
File:
C:\Users\..\FPGA.SchDoc
Drawn By:

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| Title | | |
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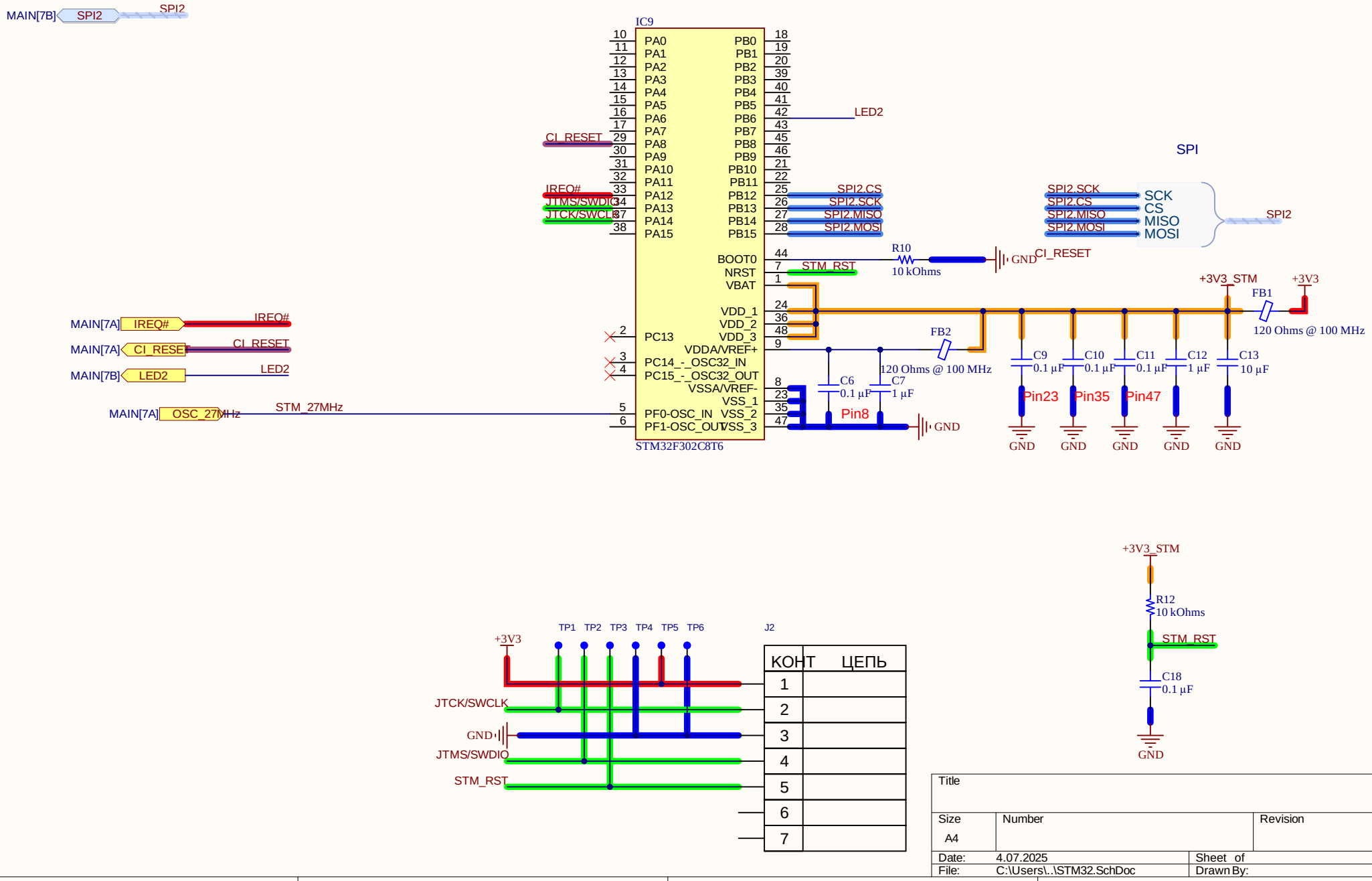
| File: C:\Users\..\FPGA_POWER.SchDoc | | Drawn By: |


MAIN[7B]
SPI2
IC9
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13
PA14
PA15
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
BOOT0
NRST
VBAT
VDD_1
VDD_2
VDD_3
VDDA/VREF+
PC13
PC14_-_OSC32_IN
PC15_-_OSC32_OUT
VSSA/VREF-
VSS_1
PF0-OSC_IN
PF1-OSC_OUT
VSS_2
VSS_3
STM32F302C8T6
LED2
CI_RESET
IREQ#
JTMS/SWDIO
JTCK/SWCLK
SPI2.CS
SPI2.SCK
SPI2.MISO
SPI2.MOSI
STM_RST
R10
10 kOhms
GND
SPI
SCK
CS
MISO
MOSI
+3V3_STM
+3V3
FB1
120 Ohms @ 100 MHz
FB2
C6
C7
C9
C10
C11
C12
C13
0.1 µF
1 µF
10 µF
Pin8
Pin23
Pin35
Pin47
MAIN[7A]
OSC_27MHz
STM_27MHz
TP1
TP2
TP3
TP4
TP5
TP6
J2
КОНТ
ЦЕПЬ
R12
C18
Title
Size
A4
Number
Revision
Date:
4.07.2025
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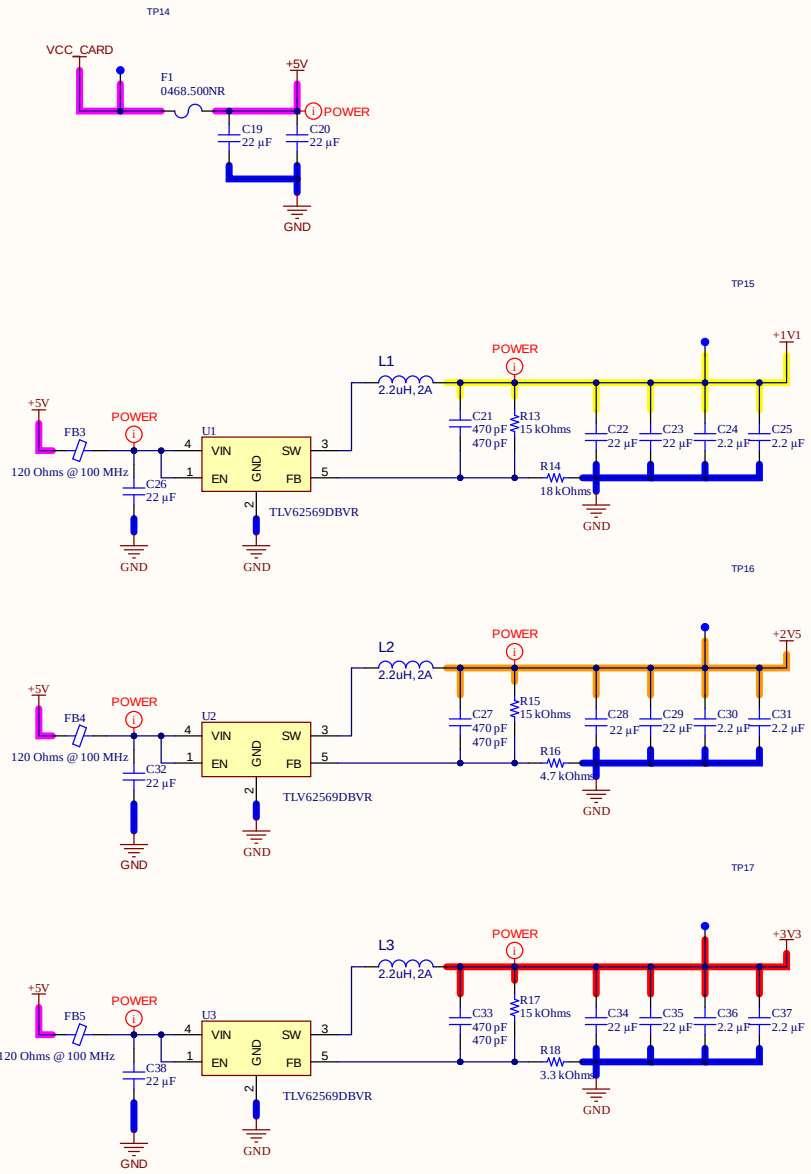
File:
C:\Users\..\STM32.SchDoc
Drawn By:

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|---|---|---|
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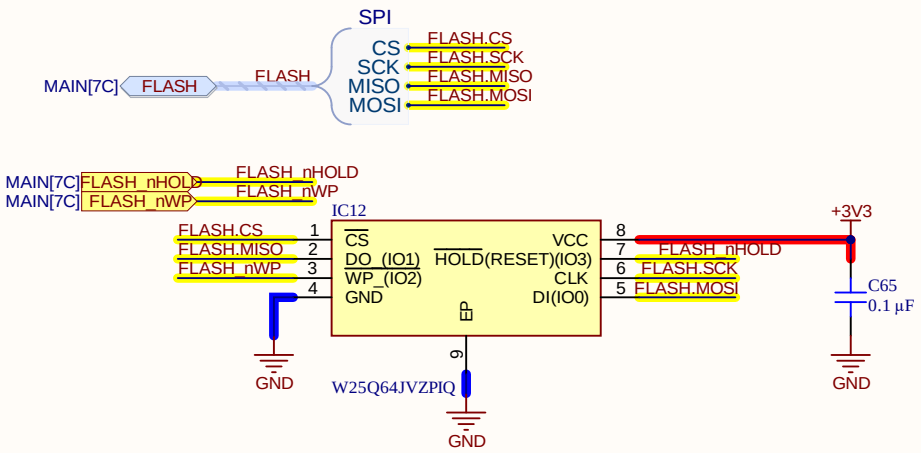
| Size A4 | Number | Revision |
| Date: 4.07.2025 | | Sheet of |
| File: C:\Users\..\POWER.SchDoc | | Drawn By: |

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| Title | | |
| Size: A4 | Number | Revision |
| Date: 4.07.2025 | | Sheet of |
| File: C:\Users\..\FLASH.SchDoc | | Drawn By: |

rev.1 first release

rev.1.1 SCHEMATIC

signal BUS_OE to U1 pin 83 (R30, R31, R33, R34, R35 убраны)

пины ПЛИС 94, 96, 97 убраны DNP резисторы, 0 Ohm подключены к GND напрямую

убраны разъемы J2 (программирования флэш), J4 (AS mode ПЛИС) update BOM SN74CBTLV1G125DCKR

R8 корректно подключен с пина 4 IC2 на GND (был на VCC)

RN1 - RN12 заменены с 330 Ом на 33 Ома

R6, R7 убраны (поддержка STM32F1 отсутствует)

LED1 переключен на ПЛИС

X1 -> заменен на J2 -> заменен на PBS2-6

VPP и VCC разделены. Пины 18 и 52 (VPP) отключены от шины питания VCC.

PCB

PCB сжать до 50*75

корректное подключение полигона 3V3 рядом с DCDC

STACKUPTotal 0.86mm

Copper 1oz

IMPEDANCE Width 0.15mm - S75 - Imp 68.2(-9%) Standart = 60-90 Ohm

ADD "POWER" class with VIA 0.6/0.3

rev.1.11 STM_RCC_OUT убран с ПЛИС и СТМ, на 5 OSC_IN заеден сигал с генератора у3

TODO разобраться с питанием ПЛИС, лишние домены с DCDC убрать

rev.2.0 Lattice FP caBGA256 recommend 0.45 0.53

example 0.35 0.5 0.100/0.100 0.4/0.15

current 0.42 0.54 0.125/0.125 0.4/0.2

| | | | | |
|---|---|---|---|---|
| Title | | | | |
| Size A4 | Number | | | Revision |
| Date: 4.07.2025 | | | Sheet of | |
| File: C:\Users\..\INFO.SchDoc | | | Drawn By: | |

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|---|---|---|---|---|---|
| | Top Overlay | | | | |
| | Top Solder | SM-001 | 0,025mm | 3.5 | |
| | Top Copper Plating | PbSn | 0,027mm | | |
| 1 | Top Layer | CF-003 | 0,035mm | | |
| | Dielectric 1 | FR4 PR | 0,190mm | 4.6 | |
| 2 | Int1 | CF-003 | 0,035mm | | |
| | Dielectric 2 | FR4 Tg150 | 0,236mm | 4.1 | |
| 3 | Int2 | CF-003 | 0,035mm | | |
| | Dielectric 3 | FR4 PR | 0,190mm | 4.6 | |
| 4 | Bottom Layer | CF-003 | 0,035mm | | |
| | Bottom Copper Plating | PbSn | 0,027mm | | |
| | Bottom Solder | SM-001 | 0,025mm | 3.5 | |
| | Bottom Overlay | | | | |
| Total board thickness: | | | 0,861mm | | |