| | | |
|---|---|---|
| 68 | GND | |
| 67 | CD2# | O |
| 66 | MDO2 | O |
| 65 | MDO1 | O |
| 64 | MDO0 | O |
| 63 | MOSTR | O |
| 62 | MOVAI | O |
| 61 | REG# | I |
| 60 | INPACI | O |
| 59 | WAIT# | O |
| 58 | RESET | I |
| 57 | MCLKO | O |
| 56 | MDI7 | I |
| 55 | MDI6 | I |
| 54 | MDI5 | I |
| 53 | MDI4 | I |
| 52 | VPP2 | |
| 51 | VCC | |
| 50 | MDI3 | I |
| 49 | MDI2 | I |
| 48 | MDI1 | I |
| 47 | MDI0 | I |
| 46 | MISTR | I |
| 45 | IOWR# | I |
| 44 | IORD# | I |
| 43 | VS1# | O |
| 42 | CE2# | I |
| 41 | MDO7 | O |
| 40 | MDO6 | O |
| 39 | MDO5 | O |
| 38 | MDO4 | O |
| 37 | MDO3 | O |
| 36 | CD1# | O |
| 35 | GND | |

| | | |
|---|---|---|
| | GND | 34 |
| ways | IOIS1 | 33 |
| I/O | D2 | 32 |
| I/O | DI | 31 |
| I/O | DO | 30 |
| I | AO | 29 |
| I | Al | 28 |
| I | A2 | 27 |
| I | A3 | 26 |
| I | A4 | 25 |
| I | A5 | 24 |
| I | A6 | 23 |
| I | A7 | 22 |
| I | A12 | 21 |
| I | MCLK | 20 |
| I | MIVA | 19 |
| tage | VPP1 | 18 |
| | VCC | 17 |
| O | IREQ# | 16 |
| I | WE# | 15 |
| I | A14 | 14 |
| I | A13 | 13 |
| I | A8 | 12 |
| I | A9 | 11 |
| I | All | 10 |
| I | OE# | 9 |
| I | A10 | 8 |
| I | CE1# | 7 |
| I/O | D7 | 6 |
| I/O | D6 | 5 |
| I/O | D5 | 4 |
| I/O | D4 | 3 |
| I/O | D3 | 2 |
| | GND | 1 |

J1

IC9-68RD-0.635SF

95622-003LF

146229-1

R1 R2 R4 R5 R7 R8 R9

CAT16-330J8LF

IC1 IC2 IC3 IC4 IC5

74CBTLV3861PW,118

SN74CBTLV1G125DCKR

C1 C2 C3 C4 0.1 µF

R3 R6 220 Ohms

LED1 LED2 LTST-C190KGKT

TP12 TP13

U_FPGA
FPGA.SchDoc

U_STM32
STM32.SchDoc

U_FLASH
FLASH.SchDoc

U_FPGA_POWER
FPGA_POWER.SchDoc

U_POWER
POWER.SchDoc

U_INFO
INFO.SchDoc

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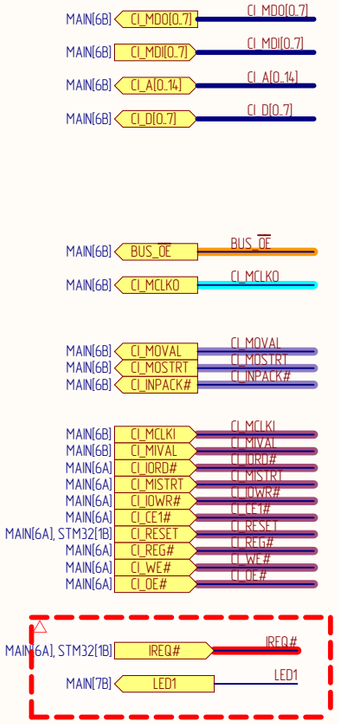
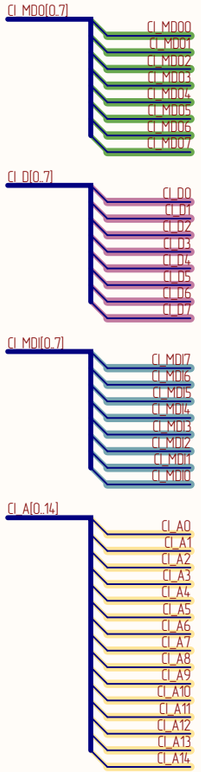
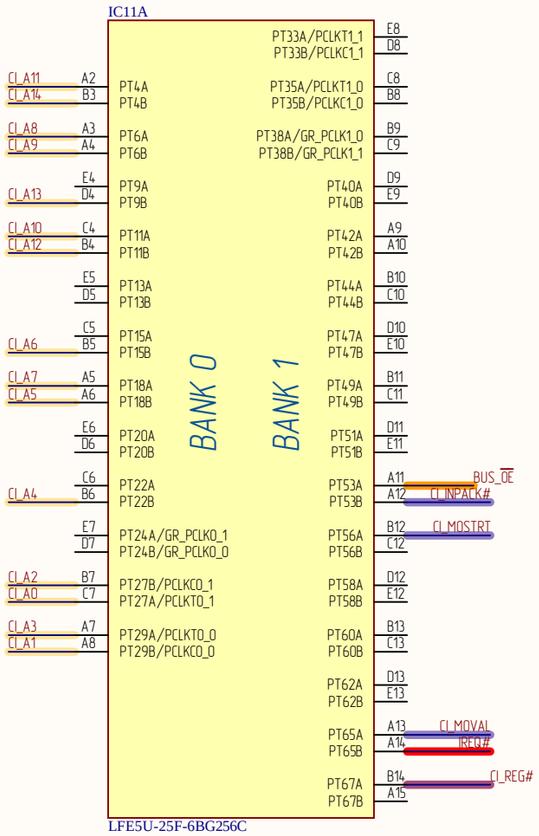
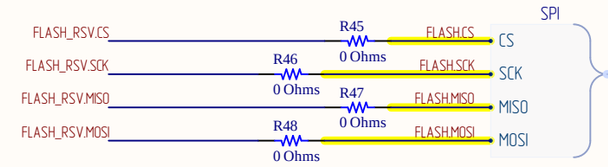


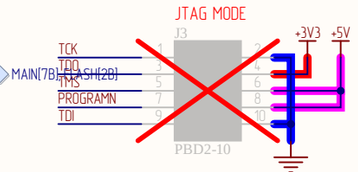
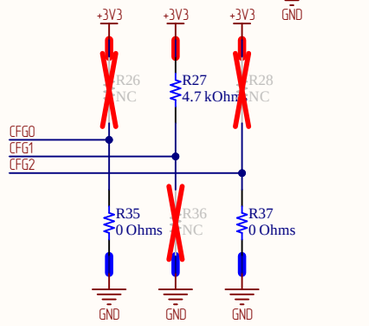
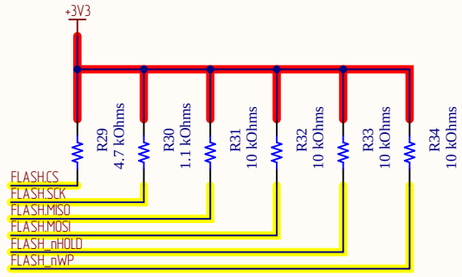
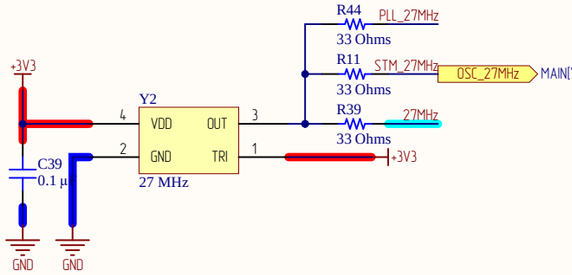



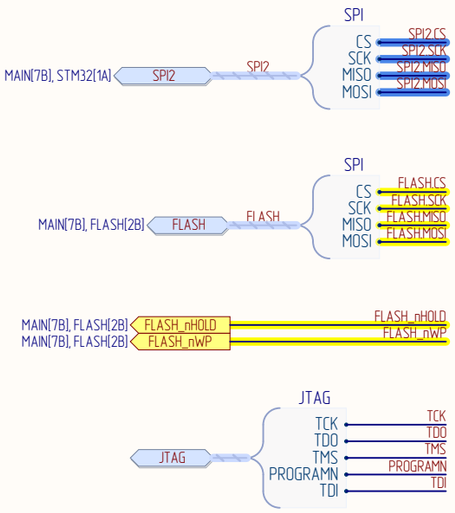

**Table 6.3. Configuration Pins Needed per Programming Mode[1]**

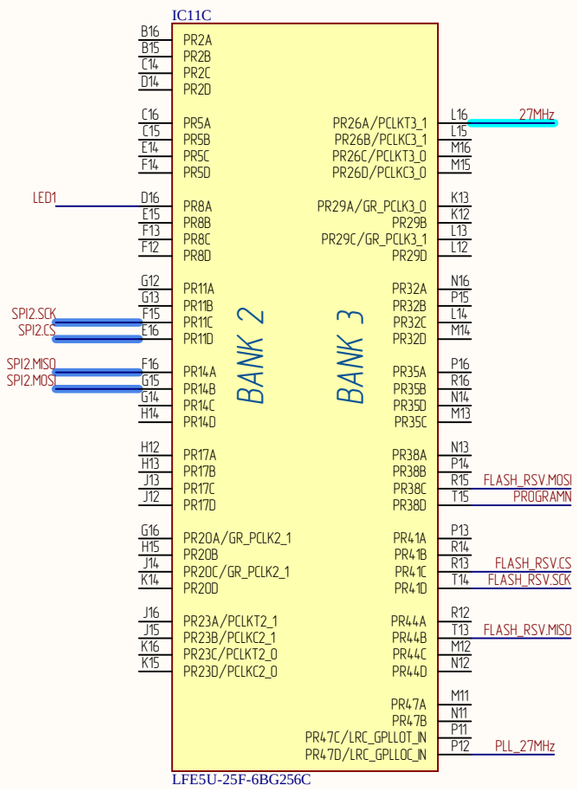
| Configuration Mode | Bus Size | Dedicated CFG[2:0] | Clock | | Shared Pins | Dedicated Pins |
|---|---|---|---|---|---|---|
| | | | Pin | I/O | | |
| SSPI | 1 Bit | 001 | CCLK | Input | MISO, MOSI, SI, DOUT, | PROGRAMN, INITN, DONE |
| MSPI[2] | 1 Bit | 010 | MCLK | Output | MISO, MOSI, CSSPIN, DOUT | PROGRAMN, INITN, DONE |
| | 2 Bits | | | | D[1:0], CSSPIN, DOUT | |
| | 4 Bits | | | | D[3:0], CSSPIN, DOUT | |
| SCM | 1 Bit | 101 | CCLK | Input | DI, DOUT | PROGRAMN, INITN, DONE |
| SPCM (Parallel) | 8 Bits | 111 | CCLK | Input | D[7:0], DOUT, CSON, BUSY, WRITEN, CSN, CS1N | PROGRAMN, INITN, DONE |
| JTAG | 1 Bit | xxx | TCK | Input | — | TCK, TMS, TDI, TDO |

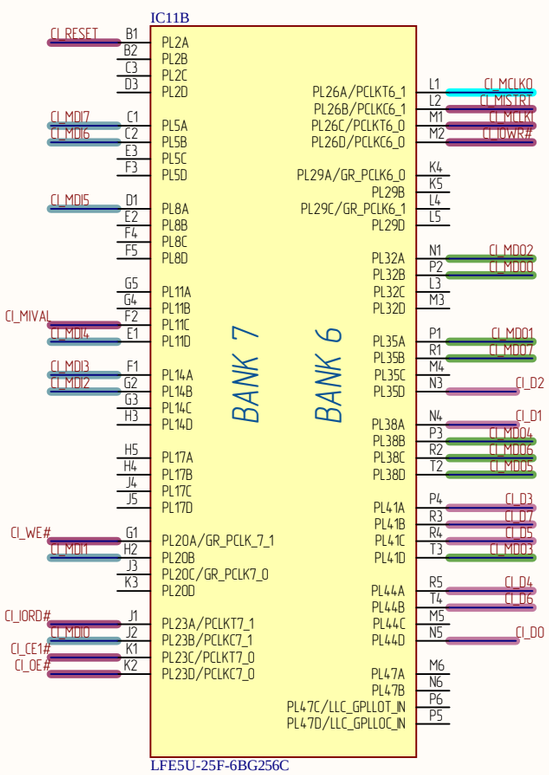


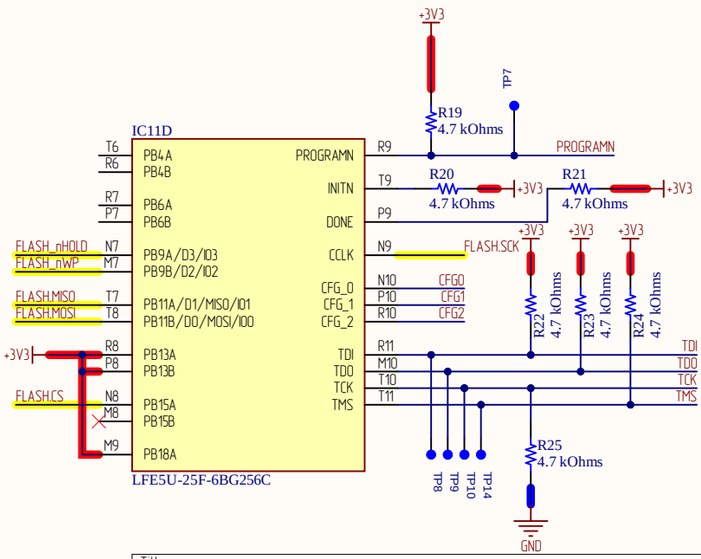

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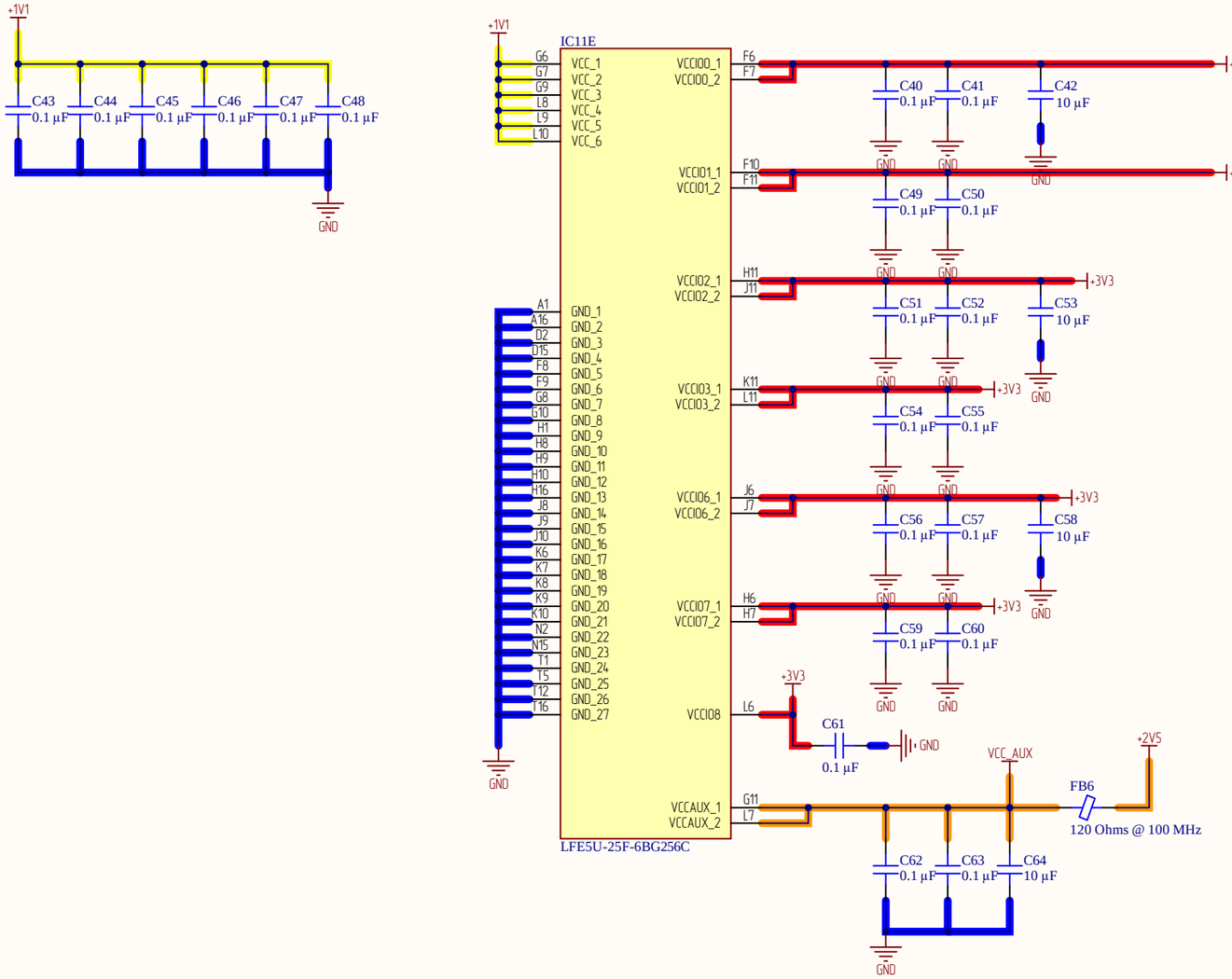


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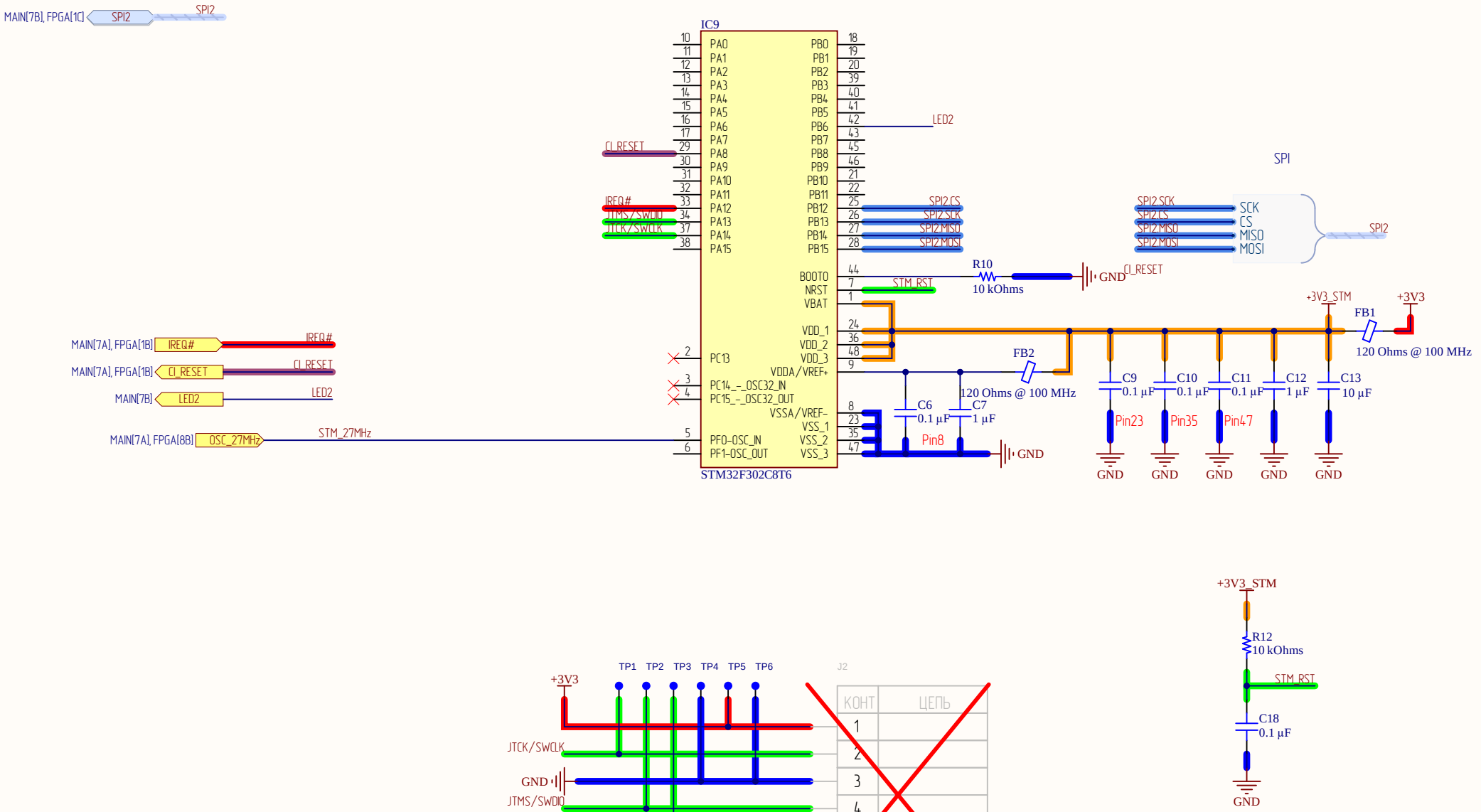
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SPI2
IC9
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13
PA14
PA15
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PB8
PB9
PB10
PB11
PB12
PB13
PB14
PB15
LED2
CI_RESET
IREQ#
JTMS/SWDIO
JTCK/SWCLK
SPI2.CS
SPI2.SCK
SPI2.MISO
SPI2.MOSI
SPI
SCK
CS
MISO
MOSI
BOOT0
NRST
VBAT
STM_RST
R10
10 kOhms
GND
+3V3_STM
+3V3
FB1
120 Ohms @ 100 MHz
VDD_1
VDD_2
VDD_3
VDDA/VREF+
FB2
PC13
PC14_-_OSC32_IN
PC15_-_OSC32_OUT
VSSA/VREF-
VSS_1
VSS_2
VSS_3
PF0-OSC_IN
PF1-OSC_OUT
C6
0.1 µF
C7
1 µF
Pin8
C9
C10
C11
C12
C13
Pin23
Pin35
Pin47
MAIN[7A], FPGA[1B]
MAIN[7B]
MAIN[7A], FPGA[8B]
OSC_27MHz
STM_27MHz
STM32F302C8T6
TP1
TP2
TP3
TP4
TP5
TP6
J2
КОНТ
ЦЕПЬ
R12
C18
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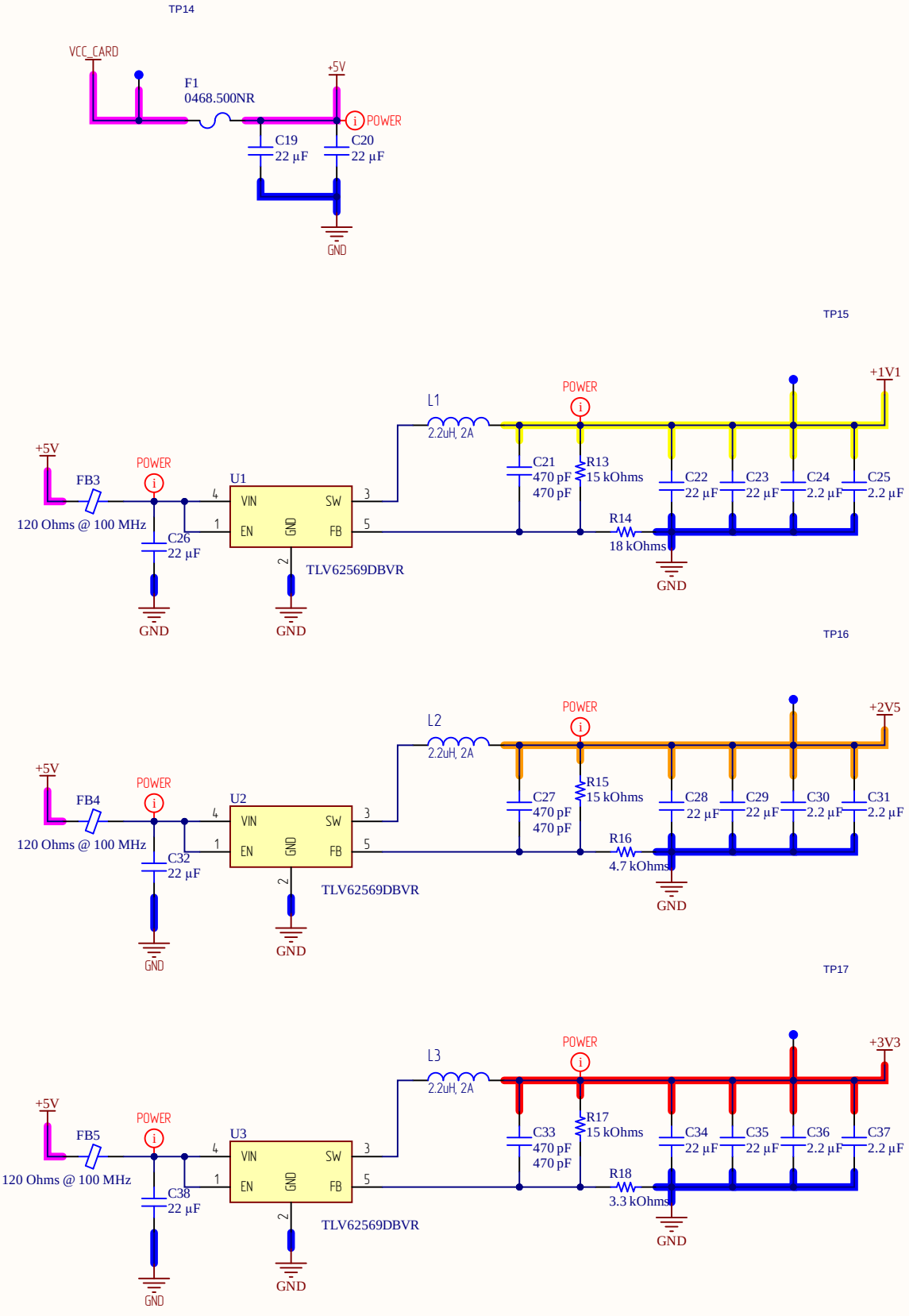


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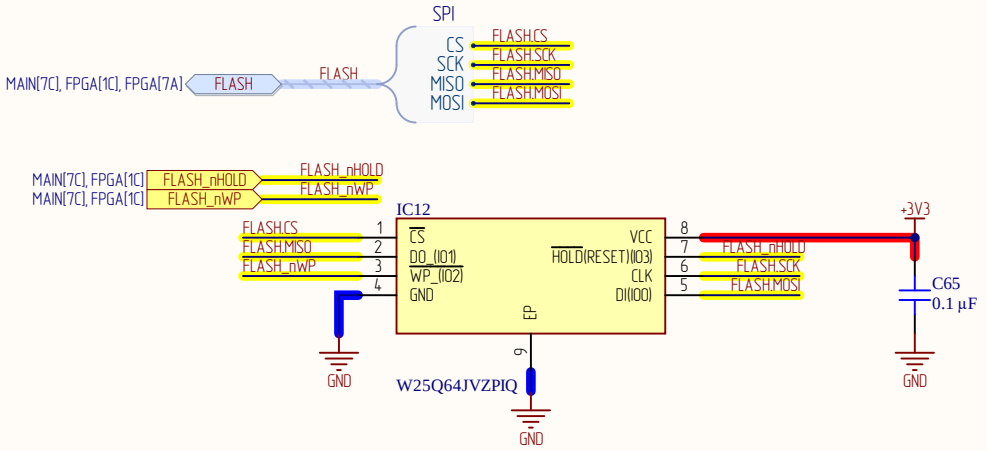


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rev.1 first release

rev.1.1 SCHEMATIC

signal BUS_OE to U1 pin 83 (R30, R31, R33, R34, R35 убраны)

пины ПЛИС 94, 96, 97 убраны DNP резисторы, 0 Ohm подключены к GND напрямую

убраны разъемы J2 (программирования флэш), J4 (AS mode ПЛИС)

R8 корректно подключен с пина 4 IC2 на GND (был на VCC)

RN1 – RN12 заменены с 330 Ом на 33 Ома

R6, R7 убраны (поддержка STM32F1 отсутствует)

LED1 переключен на ПЛИС

X1 -> заменен на J2 -> заменен на PBS2-6

VPP и VCC разделены. Пины 18 и 52 (VPP) отключены от шины питания VCC.

PCB

PCB сжать до 50*75

корректное подключение полигона 3V3 рядом с DCDC

STACKUP Total 0.86mm

Copper 1oz

IMPEDANCE Width 0.15mm – S75 – Imp 68.2(-9%) Standart = 60-90 Ohm

ADD "POWER" class with VIA 0.6/0.3

rev.1.11 STM_RCC_OUT убран с ПЛИС и СТМ, на 5 OSC_IN заеден сигал с генератора у3

TODO разобраться с питанием ПЛИС, лишние домены с DCDC убрать

rev.2.0 Lattice FP caBGA256

| | | | | |
|---|---|---|---|---|
| recommend | 0.45 | 0.53 | | |
| example | 0.35 | 0.5 | 0.100/0.100 | 0.4/0.15 |
| current | 0.42 | 0.54 | 0.125/0.125 | 0.4/0.2 |

update BOM SN74CBTLV1G125DCKR

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