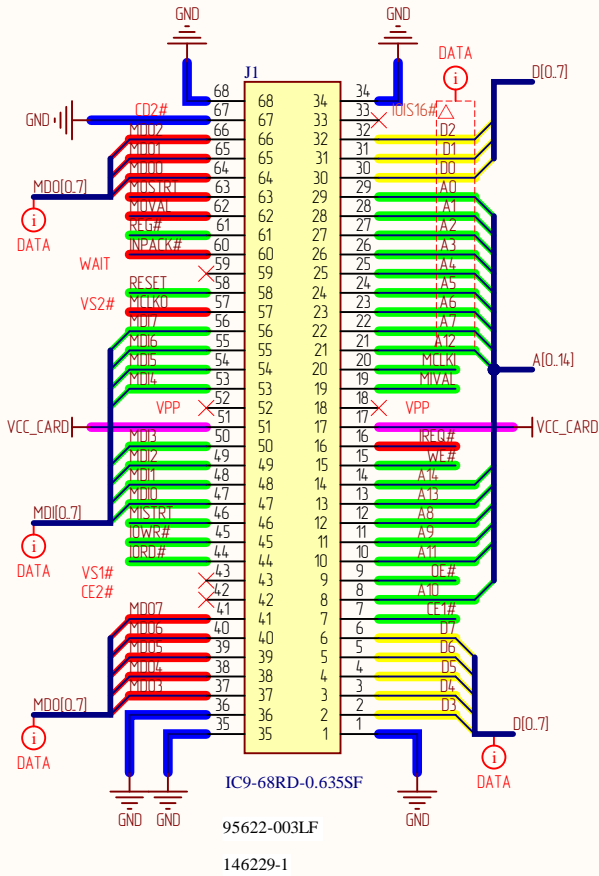
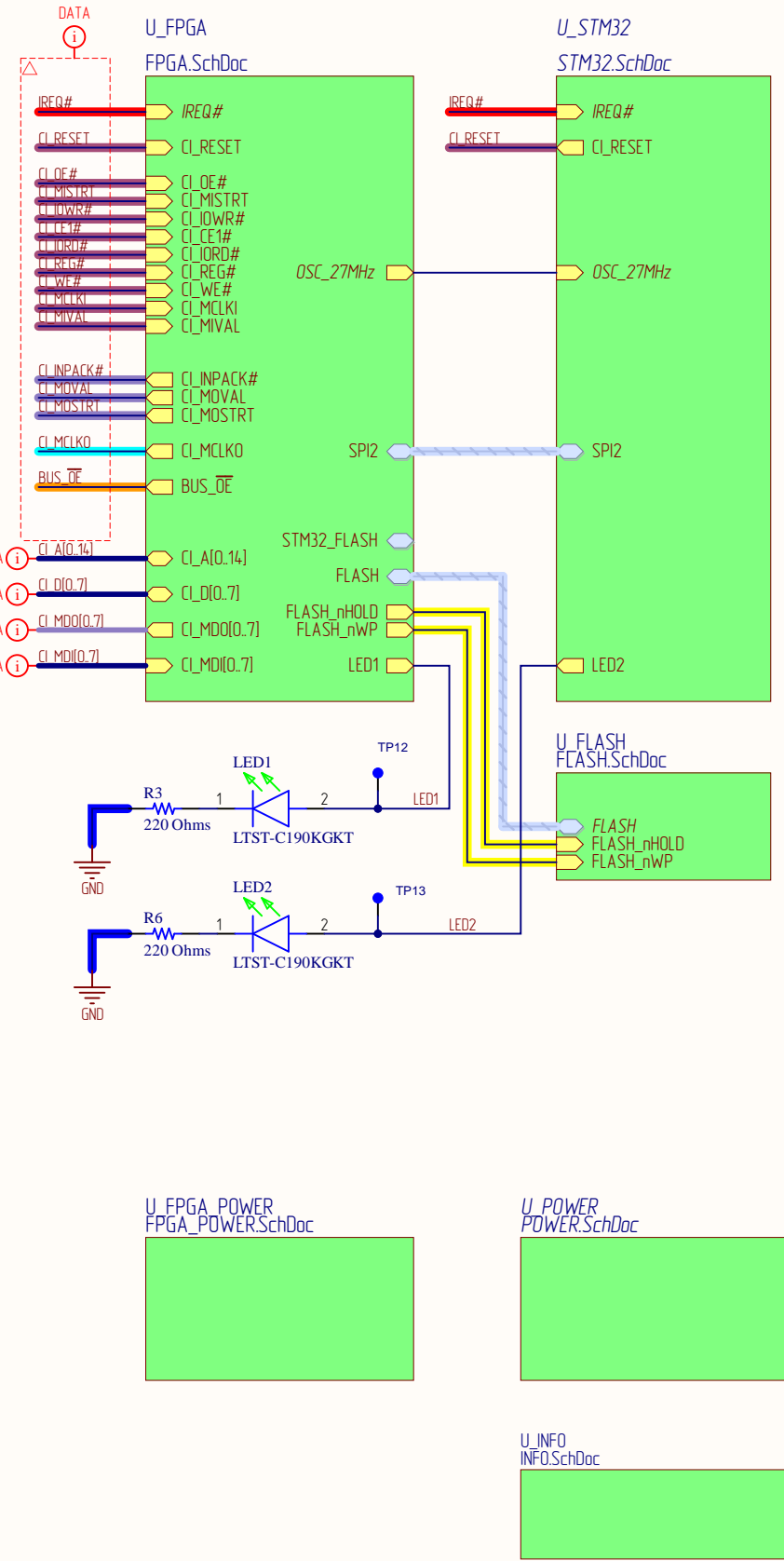
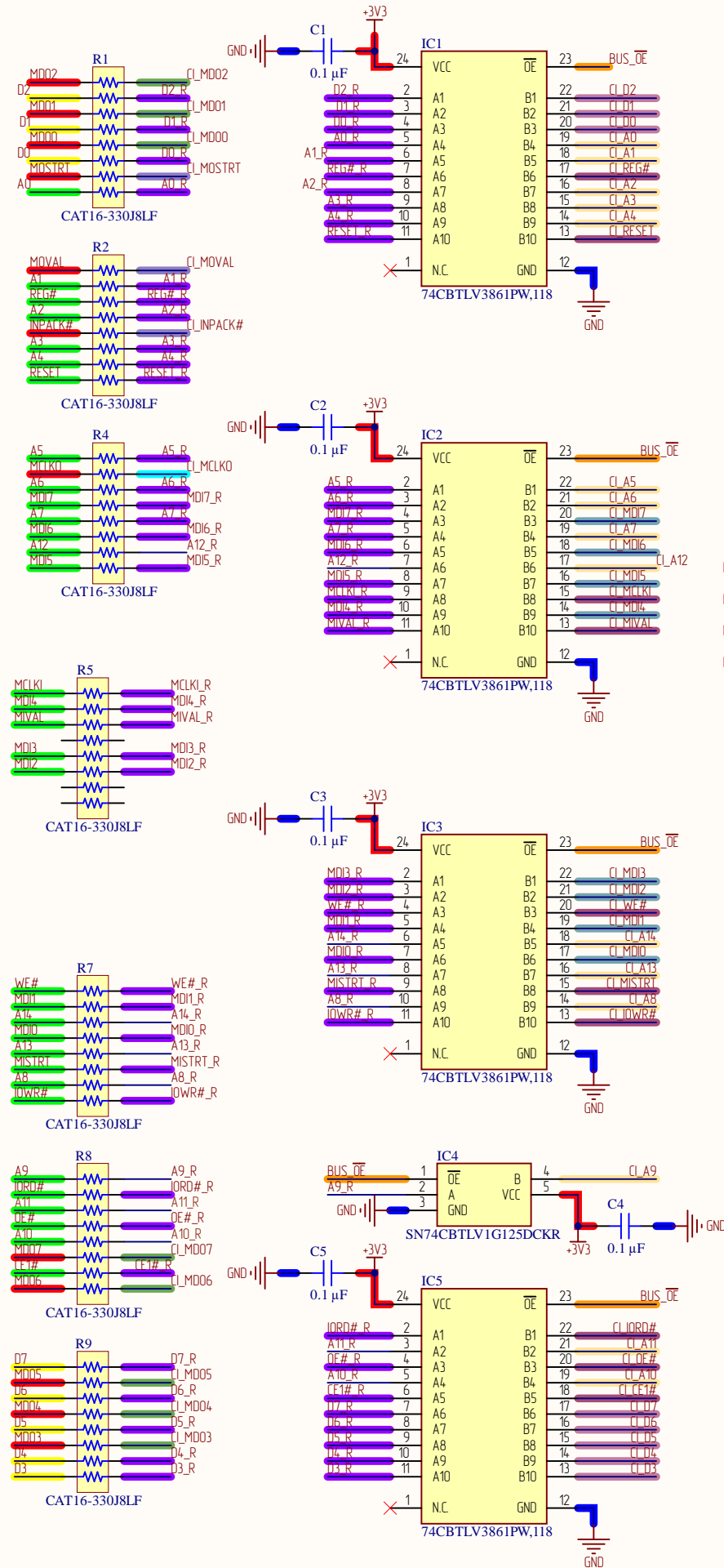


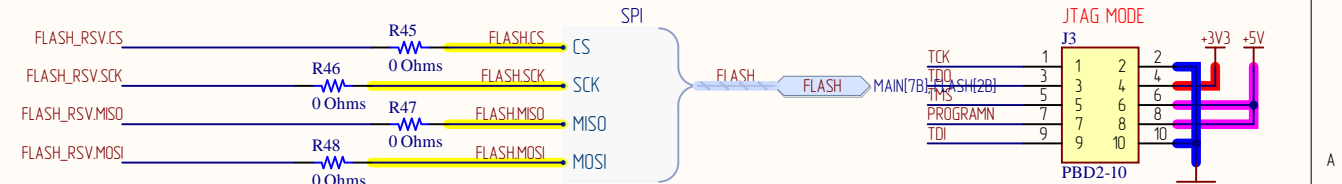
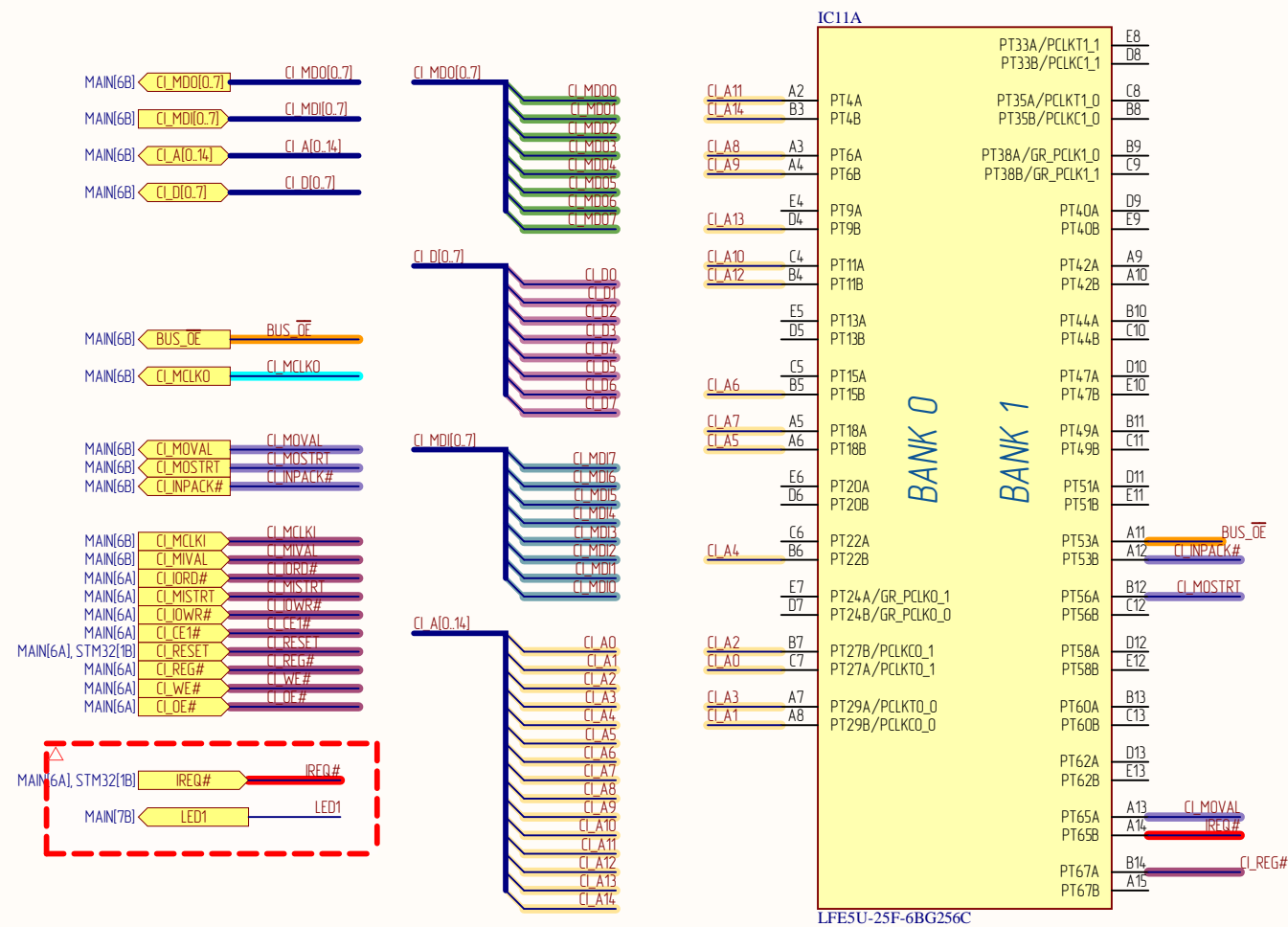
|    |         |   |
|----|---------|---|
| 68 | GND     |   |
| 67 | CD2#    | O |
| 66 | MDO2    | O |
| 65 | MDO1    | O |
| 64 | MDO0    | O |
| 63 | MOSTRT  | O |
| 62 | MOVAL   | O |
| 61 | REG#    | I |
| 60 | INPACK# | O |
| 59 | WAIT#   | O |
| 58 | RESET   | I |
| 57 | MCLK#   | O |
| 56 | MDI7    | I |
| 55 | MDI6    | I |
| 54 | MDI5    | I |
| 53 | MDI4    | I |
| 52 | VPP2    |   |
| 51 | VCC     |   |
| 50 | MDI3    | I |
| 49 | MDI2    | I |
| 48 | MDI1    | I |
| 47 | MDI0    | I |
| 46 | MISTR#  | I |
| 45 | IOWR#   | I |
| 44 | IORD#   | I |
| 43 | VS1#    | O |
| 42 | CE2#    | I |
| 41 | MDO7    | O |
| 40 | MDO6    | O |
| 39 | MDO5    | O |
| 38 | MDO4    | O |
| 37 | MDO3    | O |
| 36 | CD1#    | O |
| 35 | GND     |   |



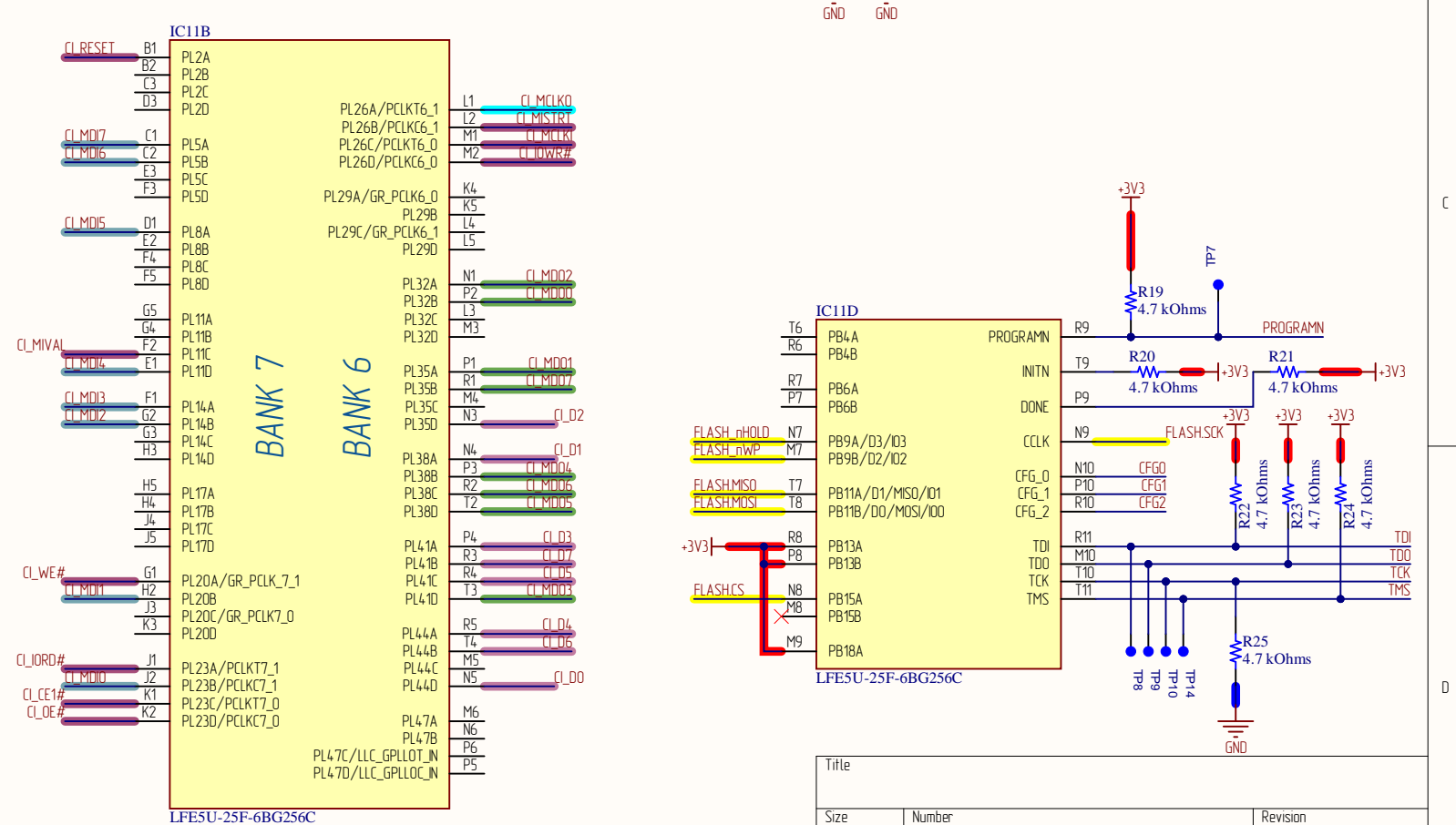
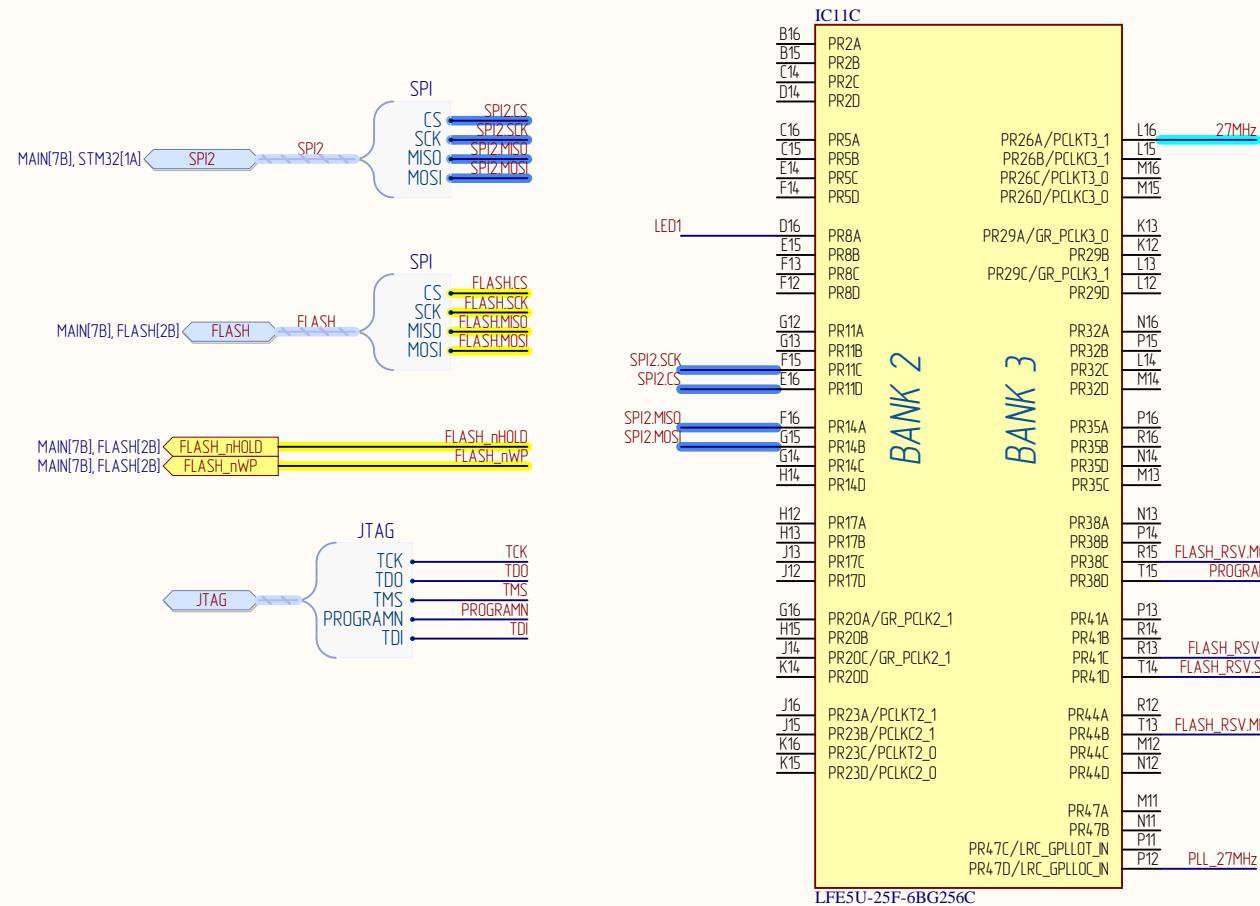
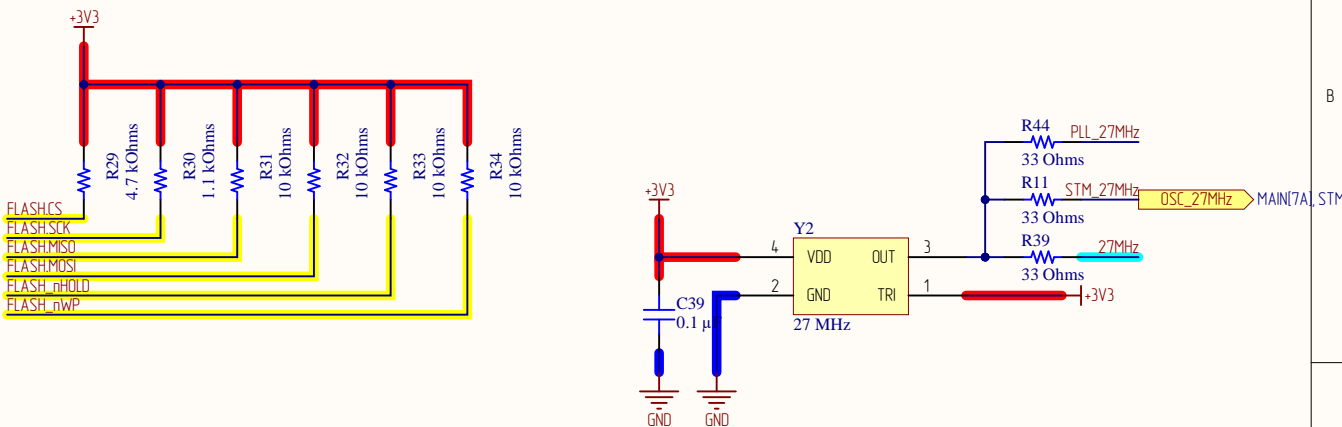
|            |    |
|------------|----|
| GND        | 34 |
| ways:IOIS1 | 33 |
| I/O D2     | 32 |
| I/O DI     | 31 |
| I/O DO     | 30 |
| I AO       | 29 |
| I AI       | 28 |
| I A2       | 27 |
| I A3       | 26 |
| I A4       | 25 |
| I A5       | 24 |
| I A6       | 23 |
| I A7       | 22 |
| I A12      | 21 |
| I MCLK#    | 20 |
| I MIVA     | 19 |
| tagc VPP1  | 18 |
| VCC        | 17 |
| O IREQ#    | 16 |
| I WE#      | 15 |
| I A14      | 14 |
| I A13      | 13 |
| I A8       | 12 |
| I A9       | 11 |
| I AI1      | 10 |
| I OE#      | 9  |
| I A10      | 8  |
| I CE1#     | 7  |
| I/O D7     | 6  |
| I/O D6     | 5  |
| I/O D5     | 4  |
| I/O D4     | 3  |
| I/O D3     | 2  |
| GND        | 1  |



|       |                          |           |
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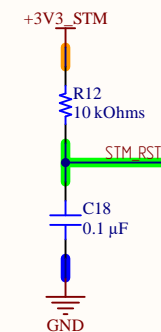
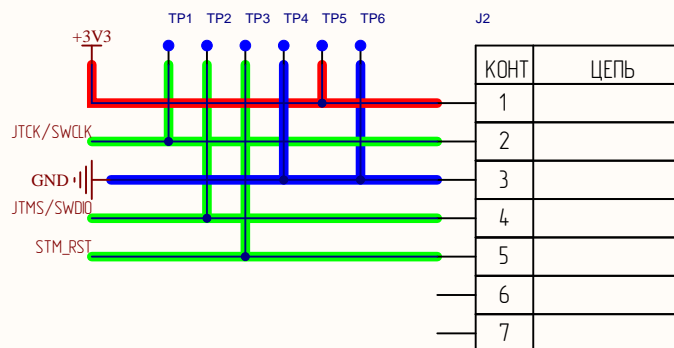
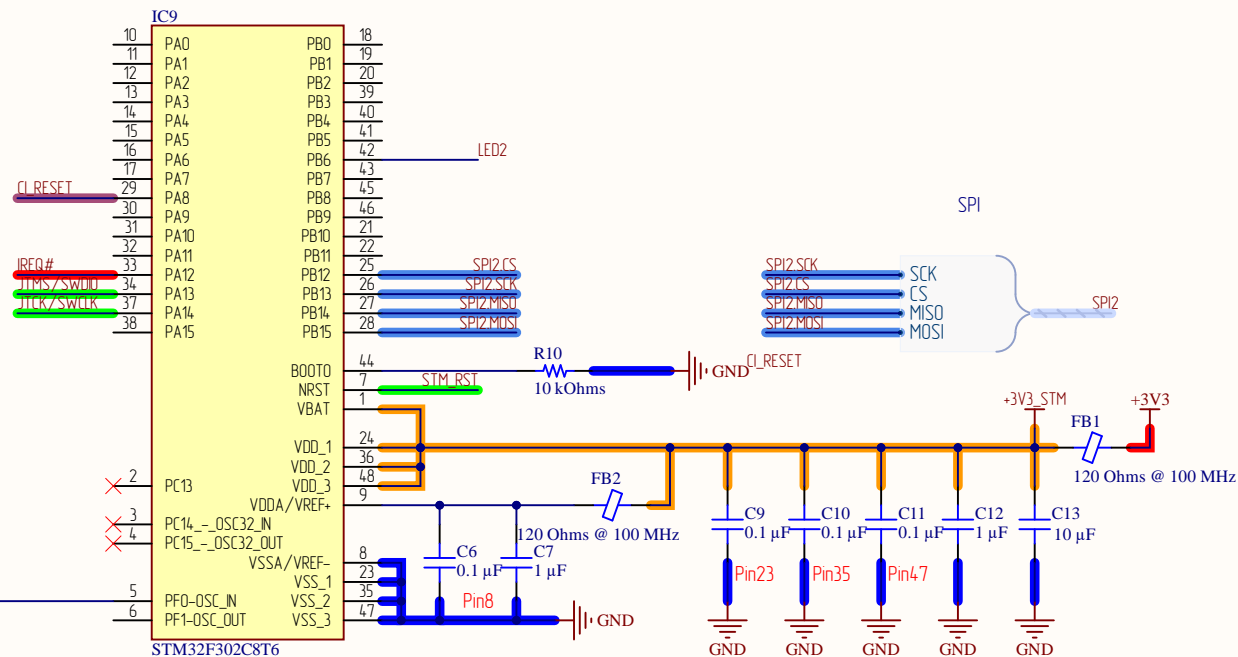
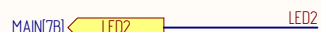
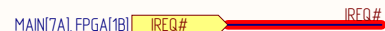
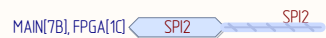


| Configuration Mode | Bus Size | Dedicated CFG[2:0] | Clock       | Shared Pins                                 | Dedicated Pins        |
|--------------------|----------|--------------------|-------------|---------------------------------------------|-----------------------|
|                    |          |                    | CLK<br>I/O  |                                             |                       |
| SPSI <sup>2</sup>  | 1 Bit    | 001                | PCLK Input  | MISO, MOSI, SS, DOUT,                       | PROGRAMM, INITN, DONE |
| MSP1 <sup>2</sup>  | 2 Bits   | 010                | MCLK Output | MISO, MOSI, CSPPIN, DOUT                    | PROGRAMM, INITN, DONE |
|                    | 2 Bits   |                    |             | DI[0], CSSIPIN, DOUT                        |                       |
|                    | 4 Bits   |                    |             | D[0:3], CSSIPIN, DOUT                       |                       |
| SPCM               | 1 Bit    | 101                | CCLK Input  | DI, DOUT                                    | PROGRAMM, INITN, DONE |
| SCM (Parallel)     | 8 Bits   | 111                | CCLK Input  | D[7:0], DOUT, CS0N, BUSY, WRITEN, CSN, CS1N | PROGRAMM, INITN, DONE |
| JTAG               | 1 Bit    | xxx                | TCLK Input  | —                                           | TCK, TMS, TDI, TDO    |

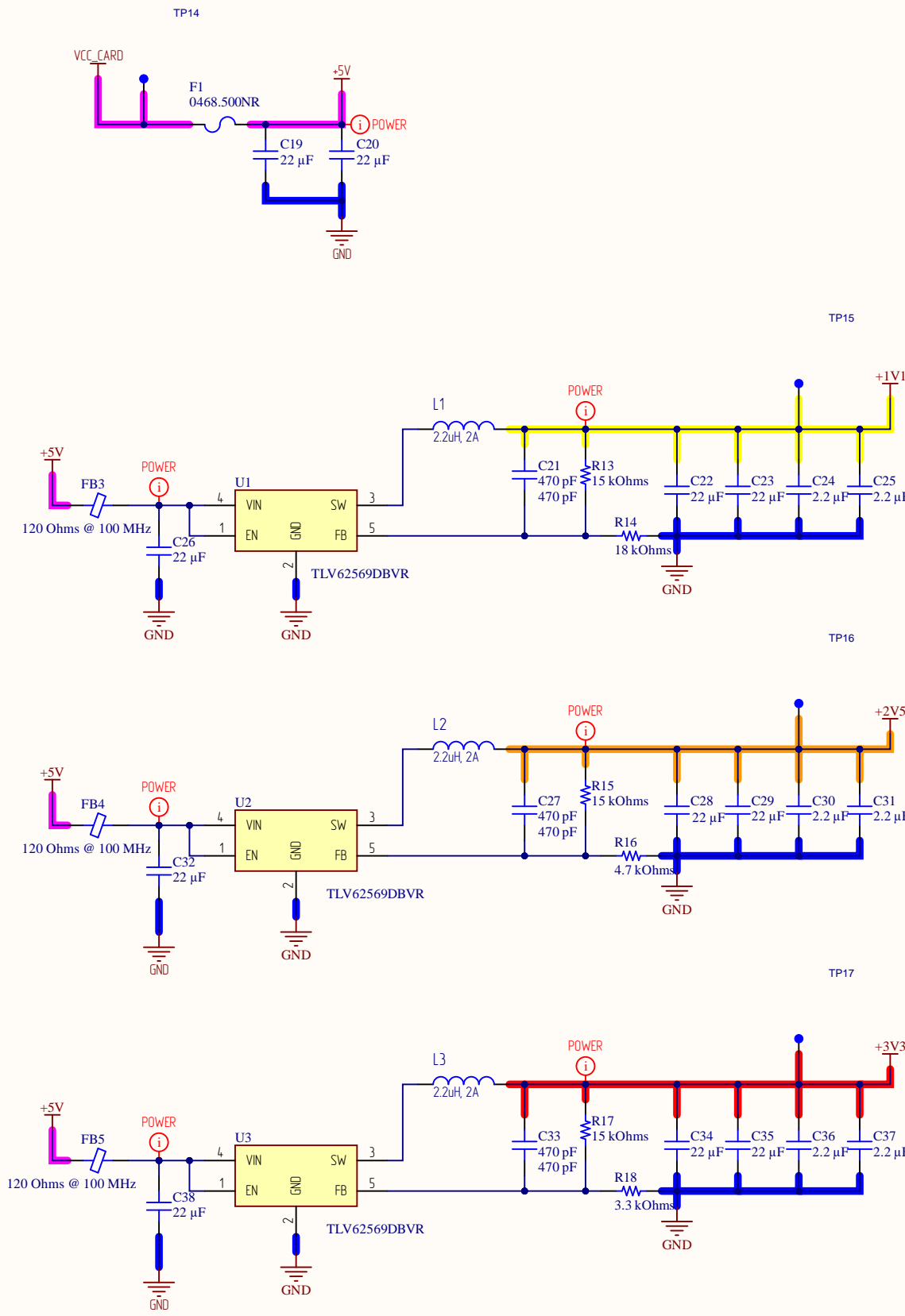


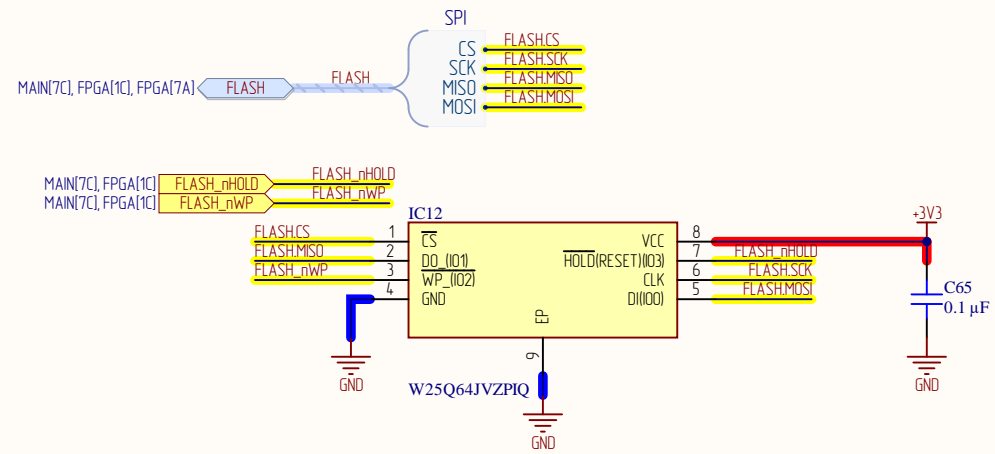
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| Date       | 4.23.2025                | Sheet of  |
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| Date<br>4/23/2025                     | Sheet of  |          |
| File<br>C:\Documents\...\FLASH.SchDoc | Drawn By: |          |

| 1       |                                                                            | 2                                                                         |  | 3                             |           | 4                   |                          |
|---------|----------------------------------------------------------------------------|---------------------------------------------------------------------------|--|-------------------------------|-----------|---------------------|--------------------------|
| A       | rev.1                                                                      | first release                                                             |  |                               | rev.2.0   | Lattice FP caBGA256 |                          |
|         | rev.1.1                                                                    | SCHEMATIC                                                                 |  |                               | recommend | 0.45                | 0.53                     |
|         | signal BUS_OE to U1 pin 83 (R30, R31, R33, R34, R35 убраны)                |                                                                           |  | example                       | 0.35      | 0.5                 | 0.100/0.100 0.4/0.15     |
| B       | пины ПЛИС 94, 96, 97 убраны DNP резисторы, 0 Ohm подключены к GND напрямую |                                                                           |  | update BOM                    | current   | 0.42                | 0.54 0.125/0.125 0.4/0.2 |
|         | убраны разъемы J2 (программирования флэш), J4 (AS mode ПЛИС)               |                                                                           |  |                               |           |                     |                          |
|         | R8 корректно подключен с пина 4 IC2 на GND (был на VCC)                    |                                                                           |  |                               |           |                     |                          |
|         | RN1 – RN12 заменены с 330 Ом на 33 Ома                                     |                                                                           |  |                               |           |                     |                          |
|         | R6, R7 убраны (поддержка STM32F1 отсутствует)                              |                                                                           |  |                               |           |                     |                          |
|         | LED1 переключен на ПЛИС                                                    |                                                                           |  |                               |           |                     |                          |
|         | X1 -> заменен на J2 -> заменен на PBS2-6                                   |                                                                           |  |                               |           |                     |                          |
|         | VPP и VCC разделены. Пины 18 и 52 (VPP) отключены от шины питания VCC.     |                                                                           |  |                               |           |                     |                          |
|         | PCB                                                                        |                                                                           |  |                               |           |                     |                          |
|         | PCB сжать до 50*75                                                         |                                                                           |  |                               |           |                     |                          |
| C       | корректное подключение полигона 3V3 рядом с DCDC                           |                                                                           |  | <div>SN74CBTLV1G125DCKR</div> |           |                     |                          |
|         | STACKUP Total 0.86mm                                                       |                                                                           |  |                               |           |                     |                          |
|         | Copper 1oz                                                                 |                                                                           |  |                               |           |                     |                          |
|         | IMPEDANCE Width 0.15mm – S75 – Imp 68.2(-9%) Standart = 60-90 Ohm          |                                                                           |  |                               |           |                     |                          |
|         | ADD "POWER" class with VIA 0.6/0.3                                         |                                                                           |  |                               |           |                     |                          |
|         | rev.1.1                                                                    | STM_RCC_OUT убран с ПЛИС и CTM, на 5 OSC_IN заеден сигнал с генератора у3 |  |                               |           |                     |                          |
|         | TODO                                                                       | разобраться с питанием ПЛИС, лишние домены с DCDC убрать                  |  |                               |           |                     |                          |
|         |                                                                            |                                                                           |  |                               |           |                     |                          |
|         |                                                                            |                                                                           |  |                               |           |                     |                          |
|         |                                                                            |                                                                           |  |                               |           |                     |                          |
| D       |                                                                            |                                                                           |  |                               |           |                     |                          |
|         |                                                                            |                                                                           |  |                               |           |                     |                          |
|         |                                                                            |                                                                           |  |                               |           |                     |                          |
|         |                                                                            |                                                                           |  |                               |           |                     |                          |
|         |                                                                            |                                                                           |  |                               |           |                     |                          |
| 1       |                                                                            | 2                                                                         |  | 3                             |           | 4                   |                          |
| Title   |                                                                            |                                                                           |  | Title                         |           |                     |                          |
| Size A4 |                                                                            | Number                                                                    |  | Revision                      |           | Revision            |                          |
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