White Rabbit: an accurate time and frequency transfer over Ethernet networks

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Electronics Design & Low-Level Software section

Open Compute Forum
5 May 2021

Outline

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- CERN and GSI initiative for control & timing

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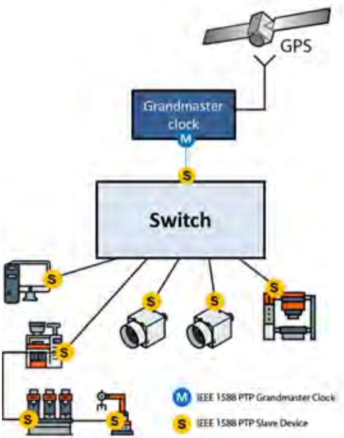

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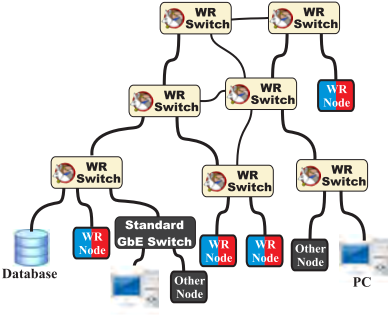

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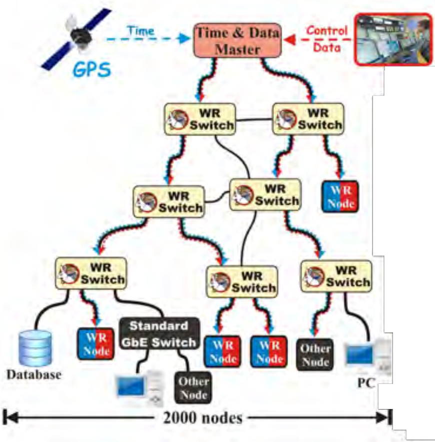
  - Sub-ns synchronisation
  - Deterministic data transfer



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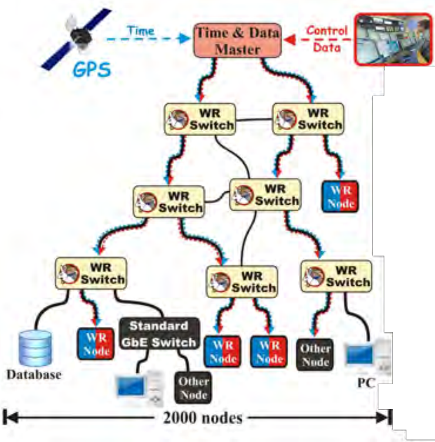

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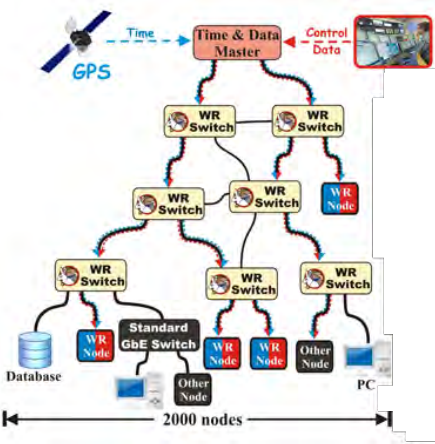
- **Open Source and commercially available**



Many users worldwide, including metrology labs...

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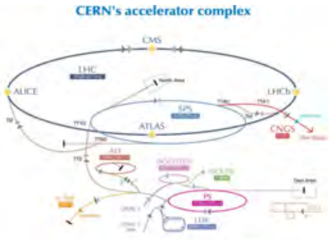

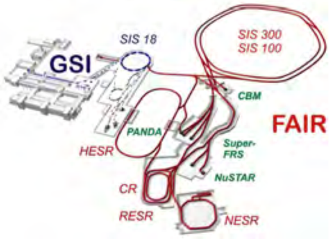

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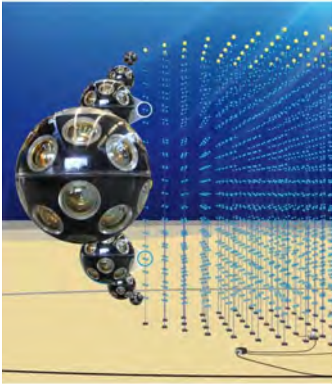

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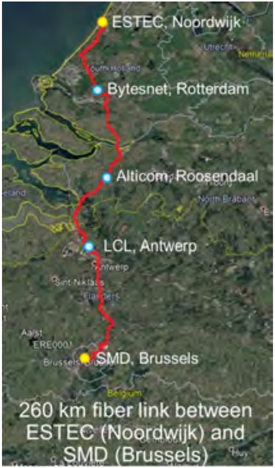

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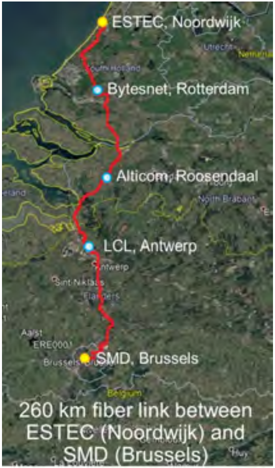

See user page: `http://www.ohwr.org/projects/white-rabbit/wiki/WRUsers`

Outline

White Rabbit technology - sub-ns synchronisation

Based on

- Gigabit Ethernet over fibre
- IEEE 1588 Precision Time Protocol

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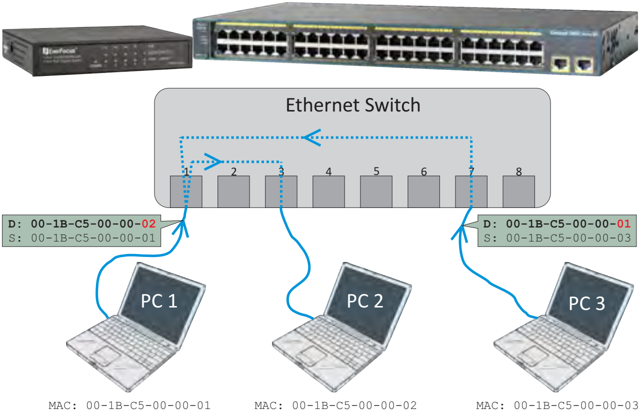
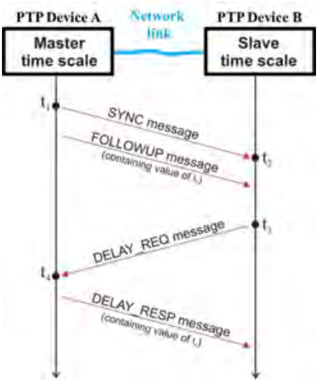
Enhanced with

- Layer 1 syntonisation
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model

Gigabit Ethernet Local Area Network over fibre



Precision Time Protocol (IEEE 1588)



- Frame-based synchronisation protocol
- Simple calculations:
  - link delay: $\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$
  - offset from master: $OFM = t_2 - (t_1 + \delta_{ms})$

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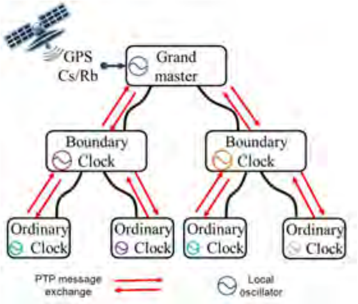

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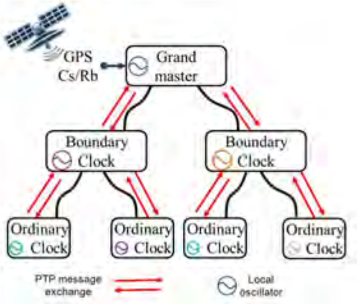

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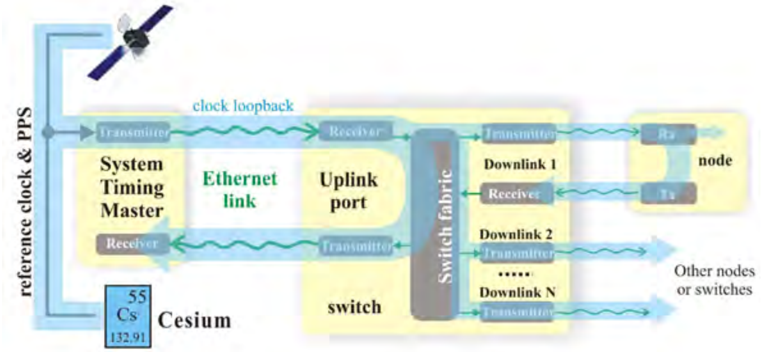
- Hierarchical network
- Shortcomings:
  - devices have free-running oscillators
  - frequency drift compensation vs. message exchange traffic
  - assumes symmetry of medium
  - timestamps resolution

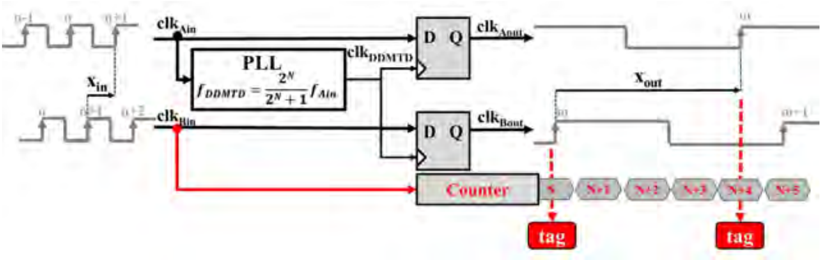
Layer 1 Syntonisation

- Clock is encoded in the Ethernet carrier and recovered by the receiver chip
- All network devices use the same physical layer clock
- Clock loopback allows phase detection to enhance precision of timestamps



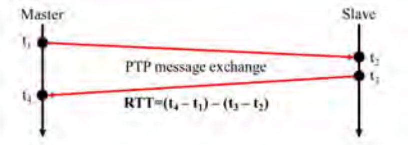
Digital Dual Mixer Time Difference (DDMTD)

- Precise phase measurements in FPGA
- WR parameters:
  - $clk_{in} \quad = 62.5$ MHz
  - $clk_{DDMTD} = 62.496185$ MHz (N=14)
  - $clk_{out} \quad = \ 3.814$ kHz
- Theoretical resolution of 0.977 ps



Link delay model

- Correction of RTT for asymmetries



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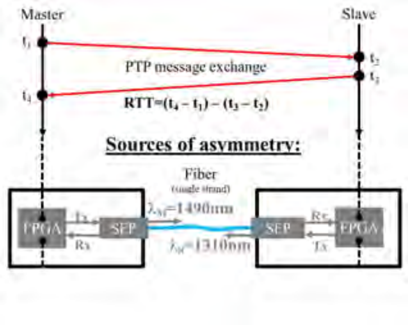

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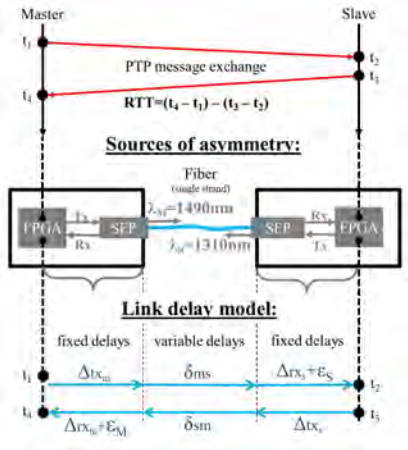
  - **Fixed delays** – FPGA, PCB, SFP
  - **Variable delays** – fiber:

    $$\alpha = \frac{\nu_g(\lambda_s)}{\nu_g(\lambda_m)} - 1 = \frac{\delta_{ms} - \delta_{sm}}{\delta_{sm}}$$
  - Calibration procedure to find fixed delays and α



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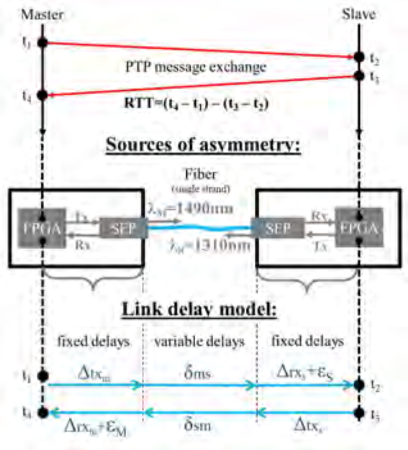
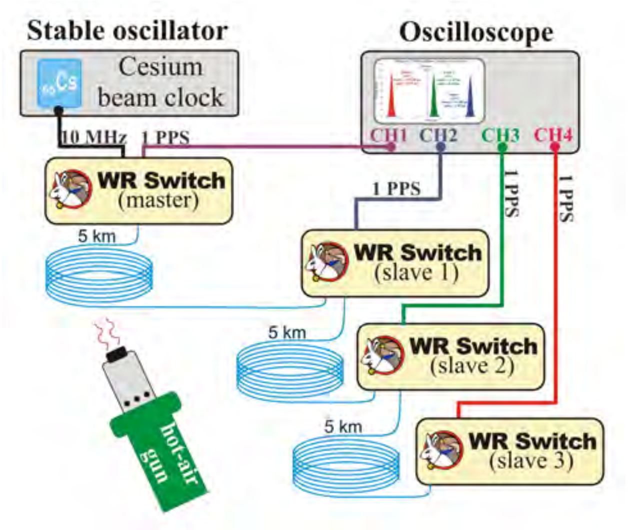
  - Calibration procedure to find fixed delays and α
- Accurate offset from master (OFM):

$$\delta_{ms} = \frac{1+\alpha}{2+\alpha} \left(RTT - \sum \Delta - \sum \epsilon\right)$$

$$OFM = t_2 - (t_1 + \delta_{ms} + \Delta_{txm} + \Delta_{rxs} + \epsilon_S)$$



Out-of-the-box performance



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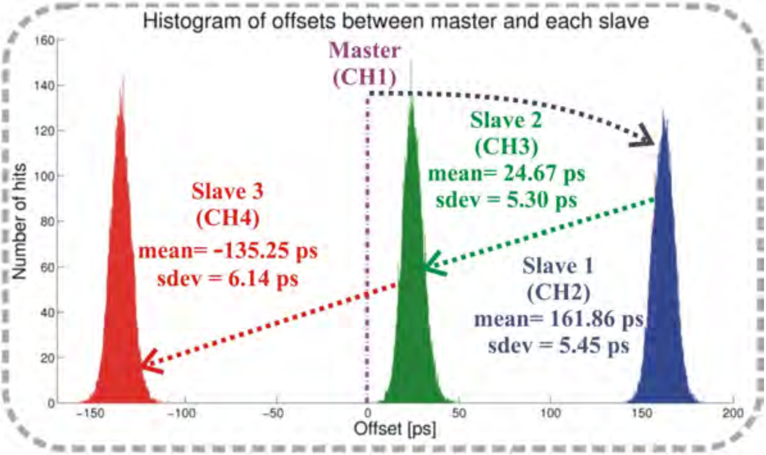
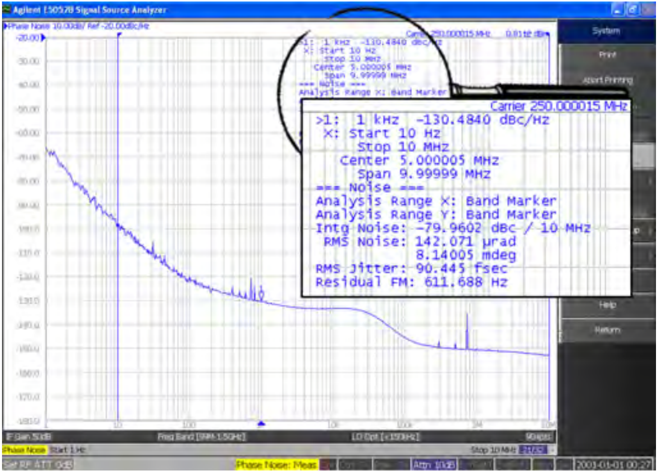


"White Rabbit: a PTP Application for Robust Sub-nanosecond Synchronization", M.Lipinski et al, ISPCS 2011

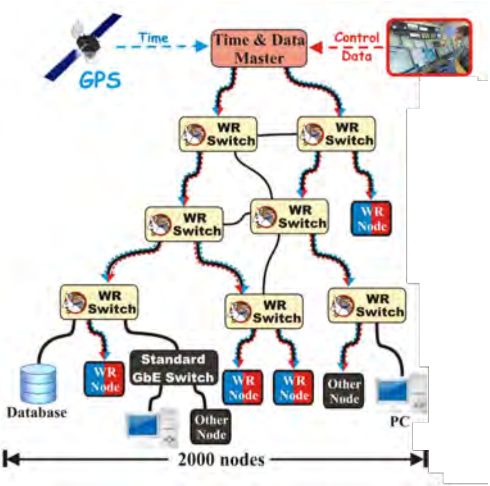
State of the art performance



- **Accuracy:** <**10 ps**
- **Jitter:** <**100 fs** RMS 10 Hz–10 MHz

Outline

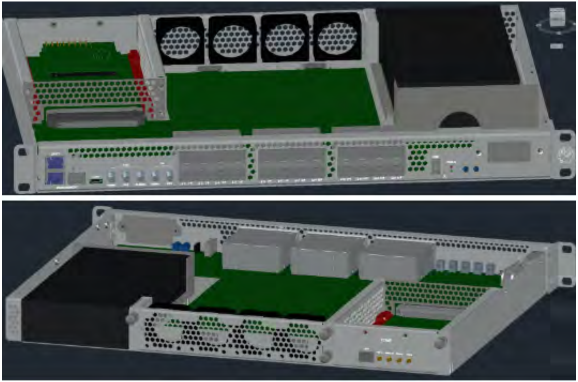
Typical WR network



WR Switch v3 - current

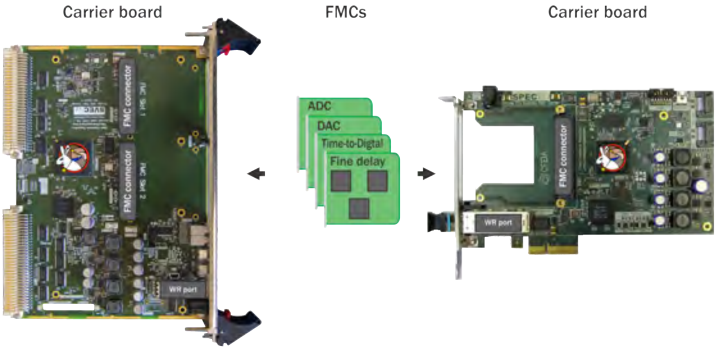
- Central element of WR network
- 18 port gigabit Ethernet switch with WR features
- Default optical transceivers: up to 10km, single-mode fiber
- Fully open, commercially available from 4 companies

WR Switch v4 - under development



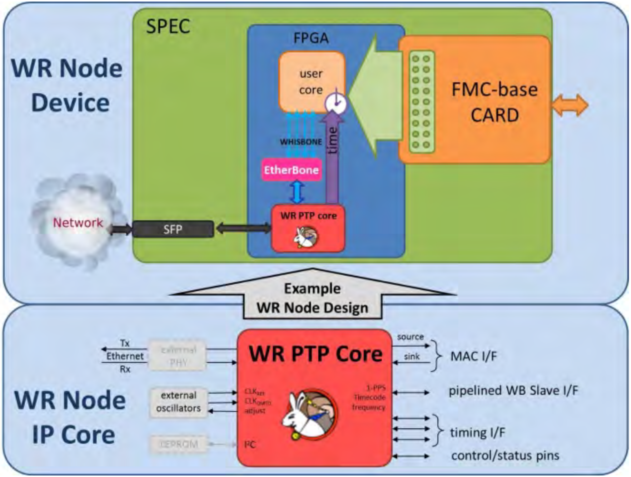
- Up to 24 port, 1 and 10 Gbps, with WR features
- Redundant & hot-swappable power supply and fans
- Expansion board
- Fully open design

WR Node: carriers + mezzanines



- All carrier cards are equipped with a White Rabbit port
- All carrier cards instantiate WR PTP Core
- Mezzanines can use the accurate clock signal and timecode (synchronous sampling clock, trigger time tag, ...)

WR PTP Core


WR Node
Device
SPEC
FPGA
user
core
WHISBONE
time
EtherBone
WR PTP core
FMC-base
CARD
Network
SFP
Example
WR Node Design
WR Node
IP Core
Tx
Ethernet
Rx
external
oscillators
WR PTP Core
source
sink
MAC I/F
pipelined WB Slave I/F
timing I/F
control/status pins

Open **and** commercially available off-the-shelf

Companies selling White Rabbit:

www.ohwr.org/projects/white-rabbit/wiki/wrcompanies

Outline

WR applications in science and beyond

- Time & frequency transfer
- Time-based control
- Precise timestamping
- Trigger distribution
- Fixed-latency data transfer
- Radio-frequency transfer

Time & frequency transfer

- Widely used/evaluated by National Time Labs (5 countries)

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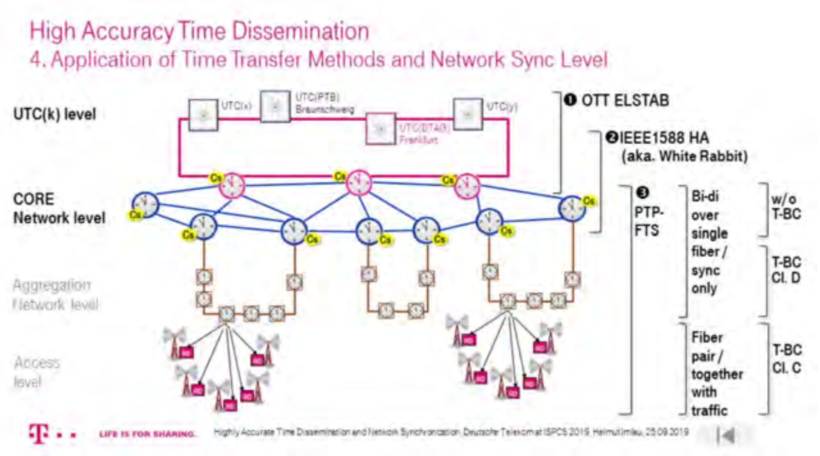
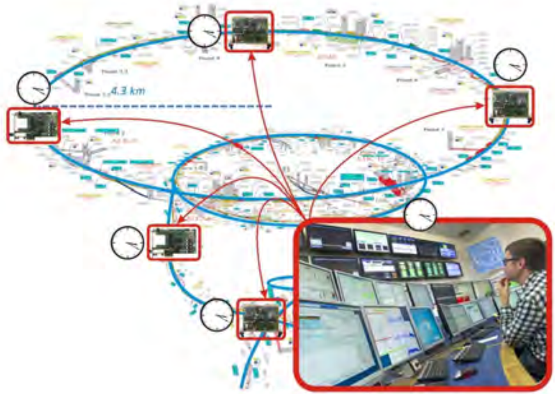


ISPCS keynote *Highly Accurate Time Dissemination & Network Synchronisation*, Helmut Imlau, Deutsche Telekom

Time-based control



Time-based control

Event ID	Hh:mm:ss:nanoseconds
ID = 1	00:00:10:000000000
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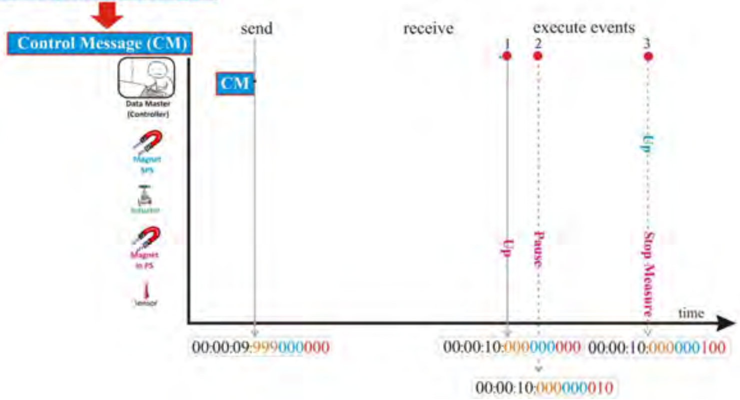

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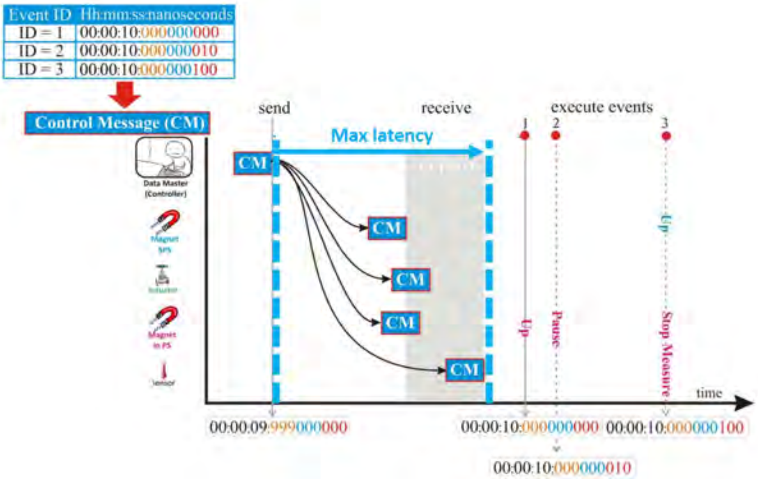
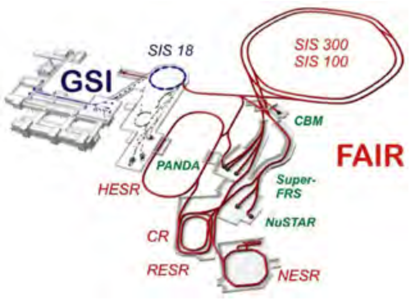


Time-based control - example application

- GSI Helmholtz Centre for Heavy Ion Research in Germany



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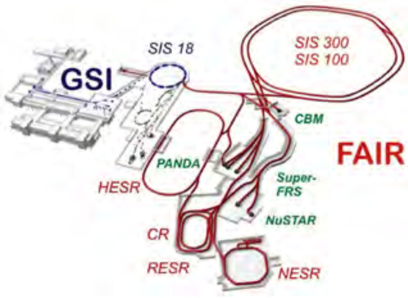
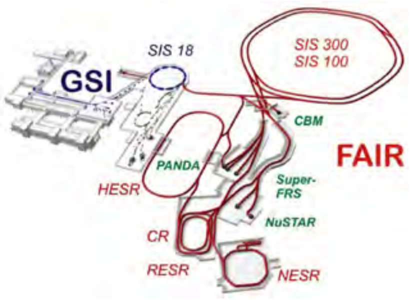


Time-based control - example application

- GSI Helmholtz Centre for Heavy Ion Research in Germany
- 1-5 ns accuracy and 10 ps precision
- WR network at GSI:
  - Operational since June 2018: 134 nodes & 32 switches
  - Final: 2000 WR nodes & 300 switches in 5 layers



Precise timestamping

- Association of time with
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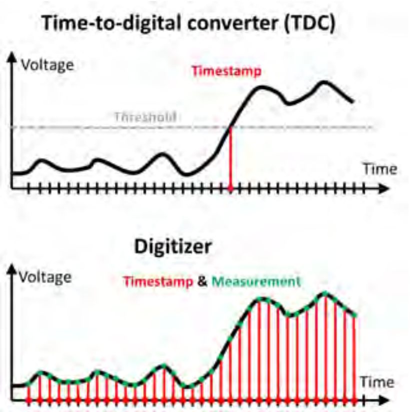

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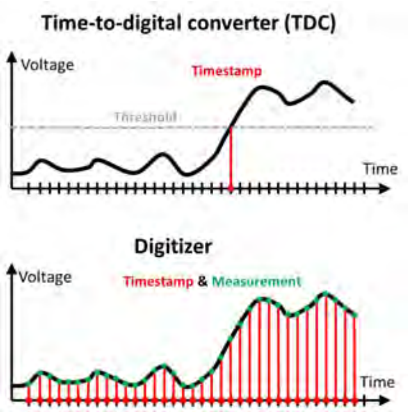

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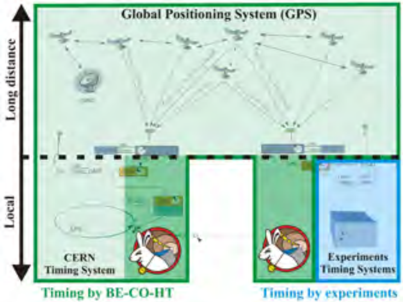

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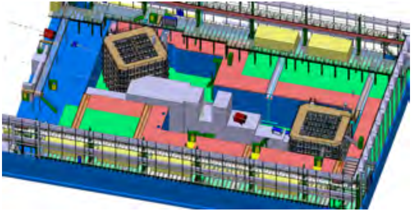

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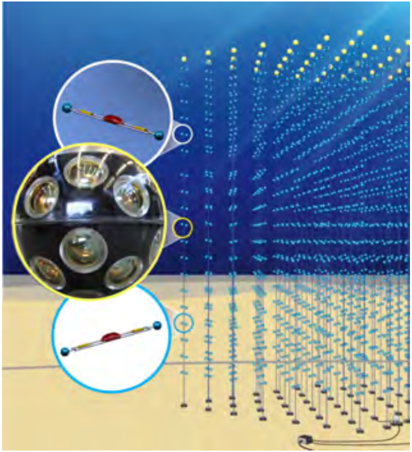

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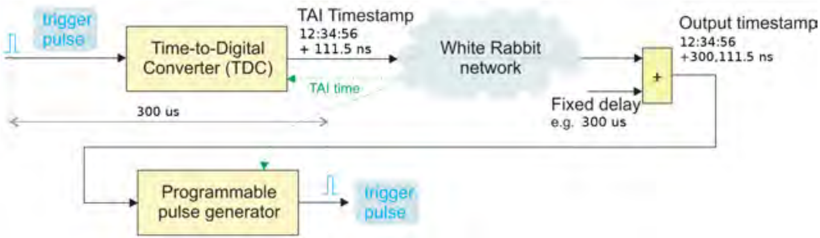
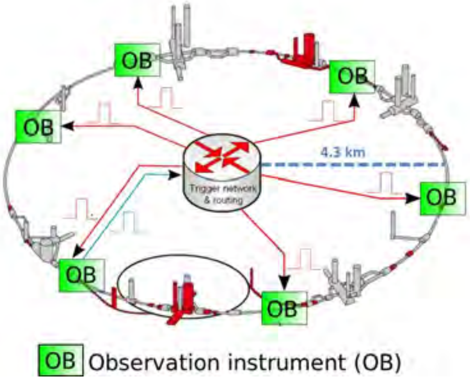
Trigger distribution



Trigger distribution - example applications

LHC trigger distribution to measure beam instabilities - since 2016



Trigger distribution - example applications

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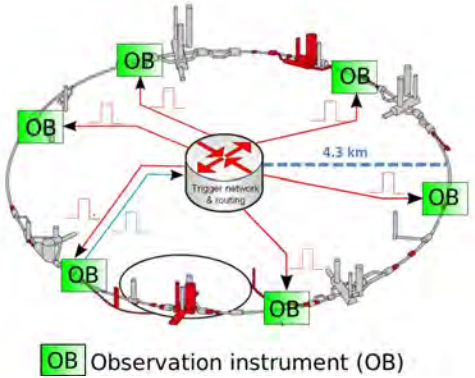
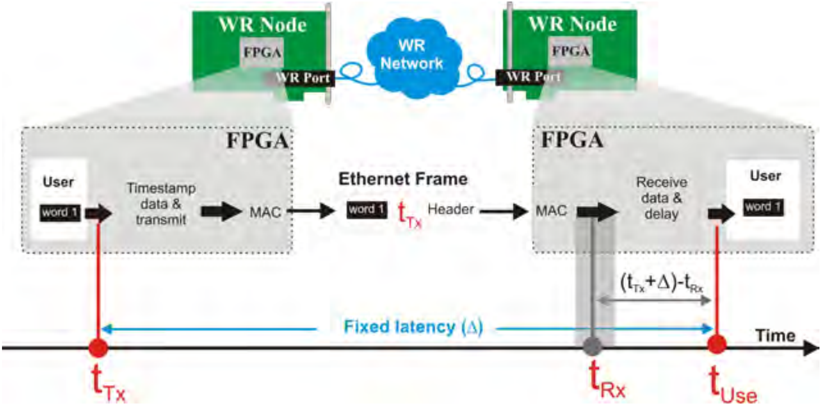


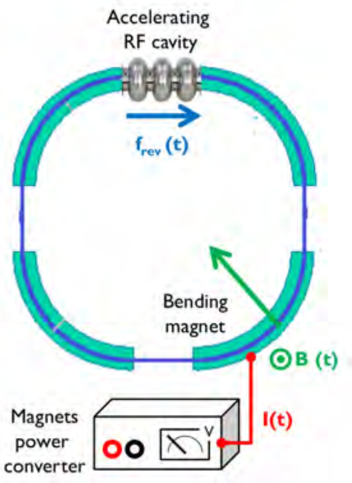
WRTD - White Rabbit Trigger Distribution- to be used for CERN's Open Analog Signals Information System (OASIS)

Fixed-latency data transfer

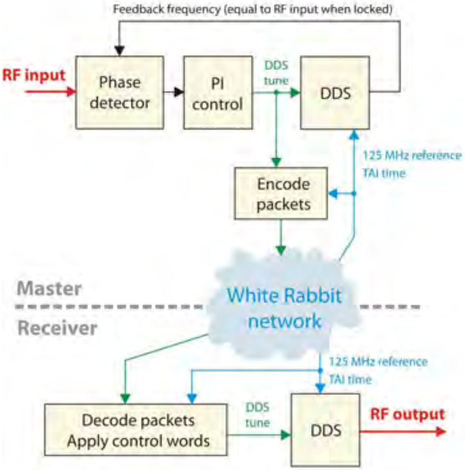


Fixed-latency data transfer- example application

Distribution of magnetic field in CERN accelerators



Radio-frequency transfer



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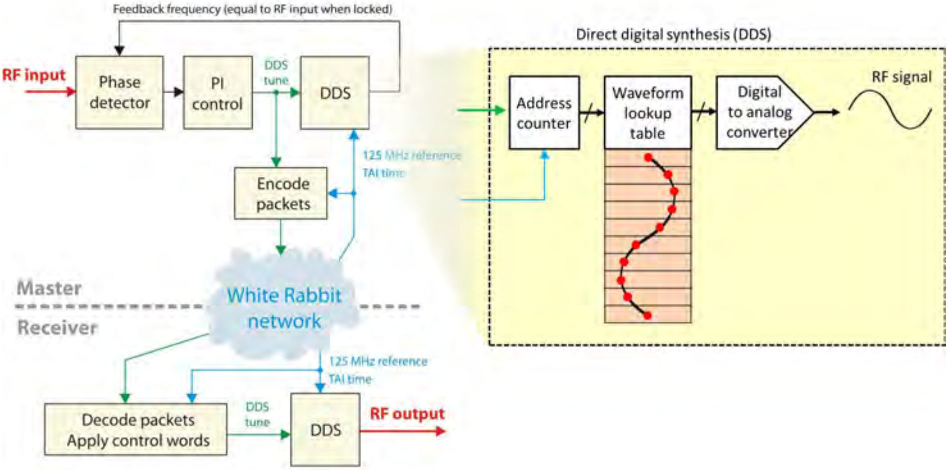
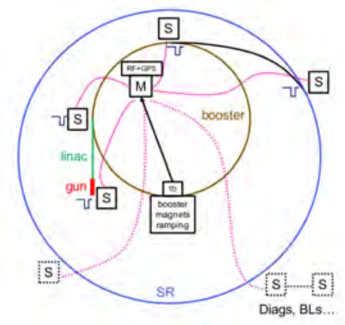


Radio-frequency transfer - example application



- RF over WR at European Synchrotron Radiation Facility (ESRF)
  - A prototype tested in operation: $<$10 ps jitter
- RF over WR at CERN
  - A prototype: $<$100 fs jitter and $<$10 ps reproducibility over reboots

Outline

WR standardisation in IEEE 1588 (1)

- IEEE standards are revised periodically

IEEE 1588

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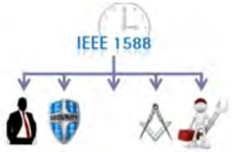

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White Rabbit integration into IEEE 1588 as High Accuracy:
`https://www.ohwr.org/projects/wr-std/wiki/wrin1588`

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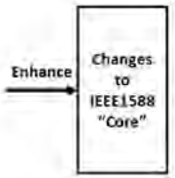

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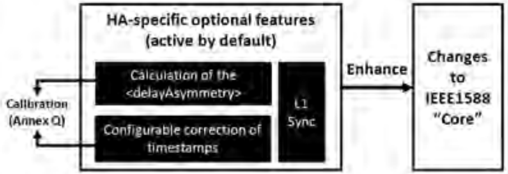

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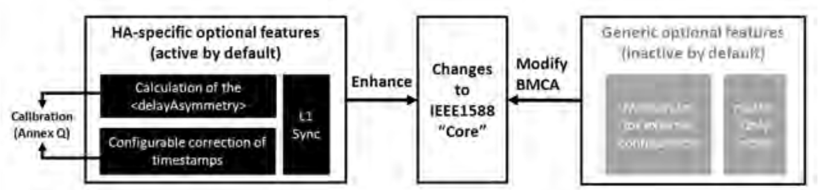

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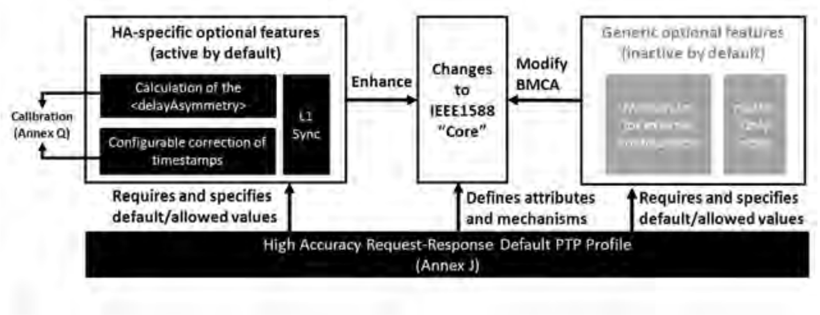

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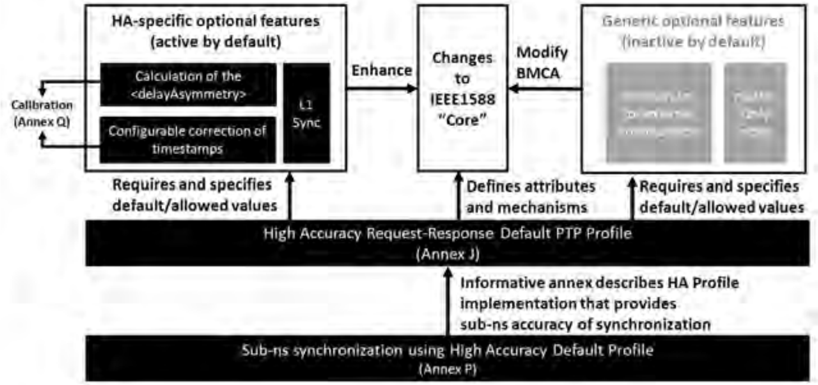

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- A versatile solution for general control and data acquisition
- Showcase of technology transfer

Q&A

Questions?

WR Project page: http://www.ohwr.org/projects/white-rabbit/wiki

Backup slides

Backup slides

Outline

Management of WR networks: monitoring & config

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  - Simple Network Management Protocol (SNMP)
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Management of WR networks: monitoring & config

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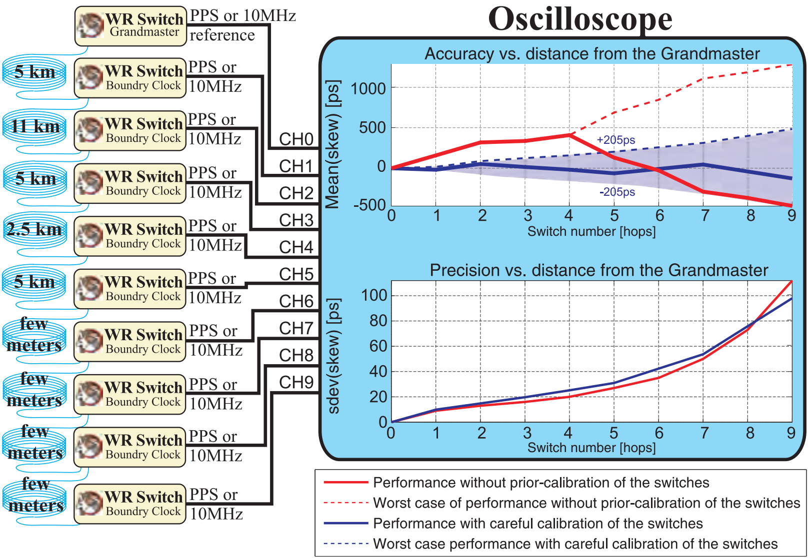
- It can be managed using standard protocols and tools:
  - Simple Network Management Protocol (SNMP)
  - Syslog
  - Link Layer Discovery Protocol (LLDP)
  - Kerberos-based authentication
- It can be debugged using standard tools:
  - Wireshark
  - Tcpdump
  - Professional Ethernet testers

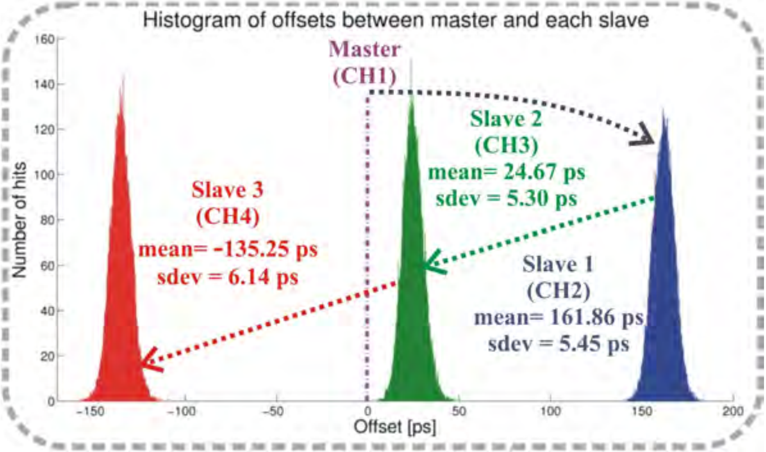
Outline

WR performance in a long chain



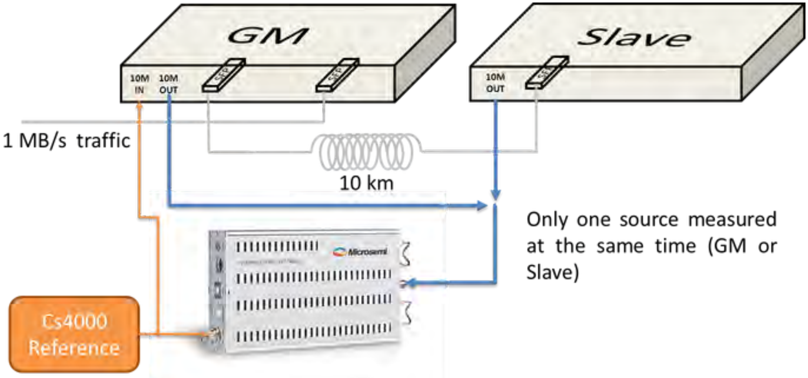
Outline

Time transfer: out-of-the-box



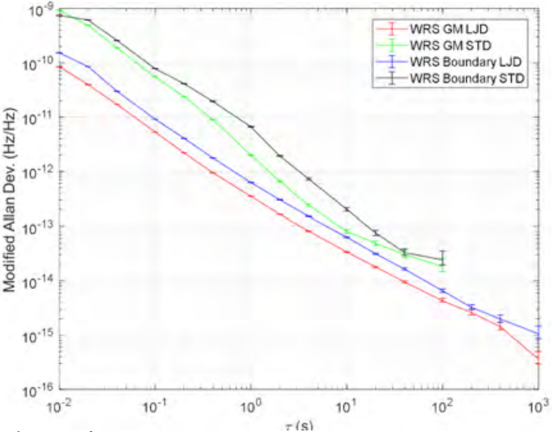
Reported in 2011

Frequency transfer: out-of-the-box and improved



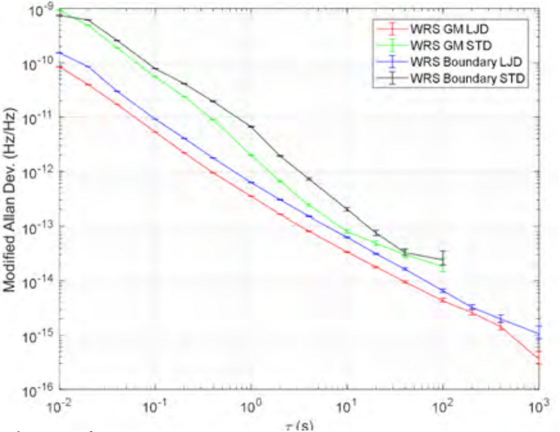
Measurement device: Microsemi/Microchip 3120A Phase Noise Test Probe

Frequency transfer: out-of-the-box and improved



- Out-of-the-box performance:
  - **GM-in to GM-out**: jitter of **9 ps** RMS 1 Hz–100 kHz and MDEV of **2E-12** τ=1 s ENBW 50 Hz
  - **GM-in to Slave-out**: jitter of **11 ps** RMS 1 Hz–100 kHz and MDEV of **4E-12** τ=1 s ENBW 50 Hz

Frequency transfer: out-of-the-box and improved



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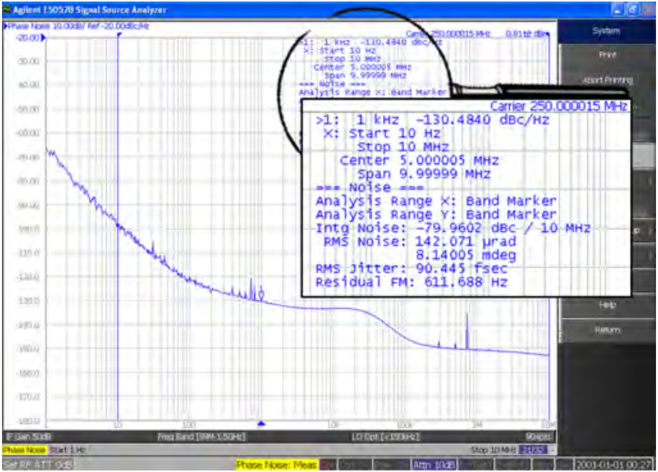
  - **GM-in to Slave-out**: jitter of **11 ps** RMS 1 Hz–100 kHz and MDEV of **4E-12** τ=1 s ENBW 50 Hz
- WR Switches improved with Low Jitter Daughterboard (LJD):
  - **GM-in to GM-out**: jitter of **1 ps** RMS 1 Hz–100 kHz and MDEV of $<$**5E-13** τ=1 s ENBW 50 Hz
  - **GM-in to Slave-out**: jitter of $<$**2 ps** RMS 1 Hz–100 kHz and MDEV of $<$**7E-13** τ=1 s ENBW 50 Hz

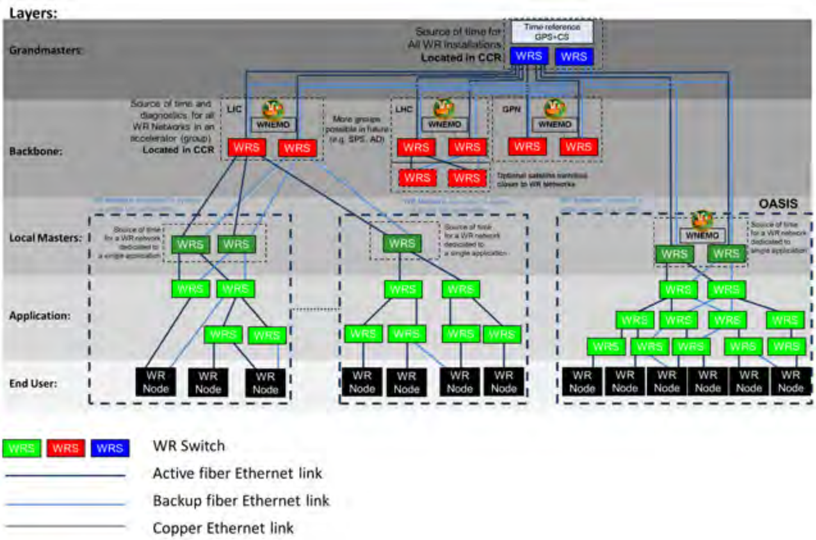
WR time & frequency tranfser: state of the art



- **GM-out to end-node-out**: accuracy of <**10 ps**
- **GM-out to end-node-out**: jitter of <**100 fs** RMS 10 Hz–10 MHz

Outline

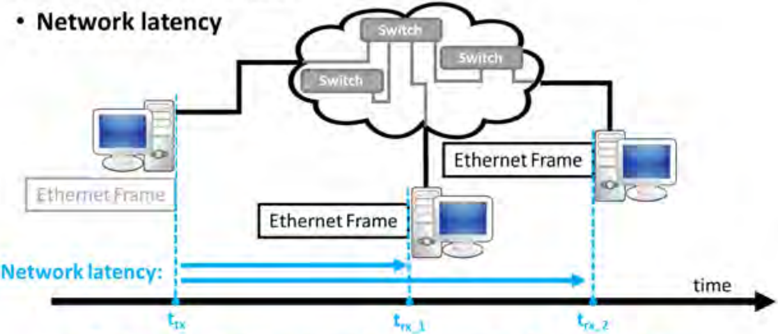
Global WR network at CERN



Outline

Determinism and Network Latency

- **Determinism**
  A deterministic system is predictable: it provides calculable and consistent characteristics of operation that are required by the application, e.g. **network latency** of data transmission.
- **Network latency**

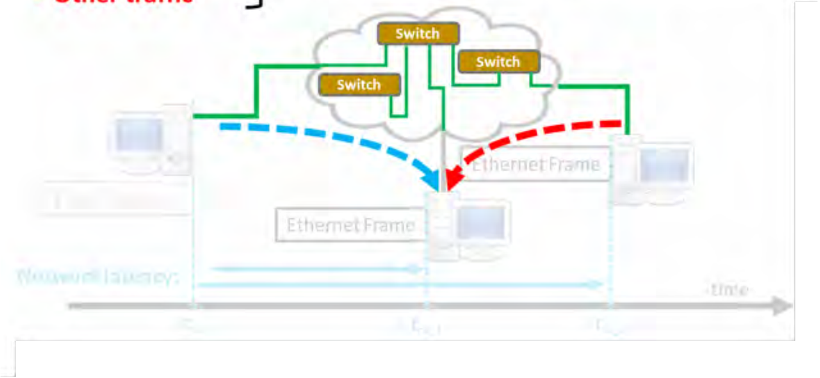


Deterministic network is a network in which we can calculate the maximum latency

Network Latency Contributors

- Cables: 5us/km – we cannot do much about this
- Switch operation
- Other traffic

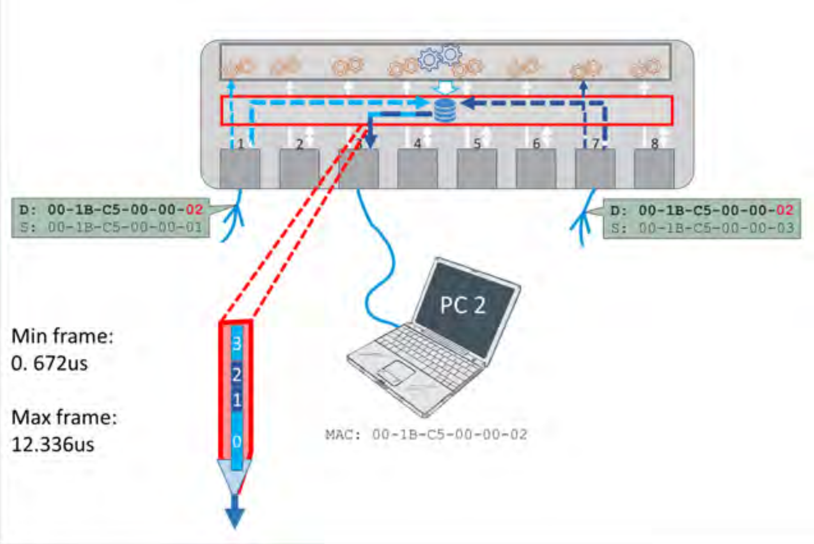
We can do something about this



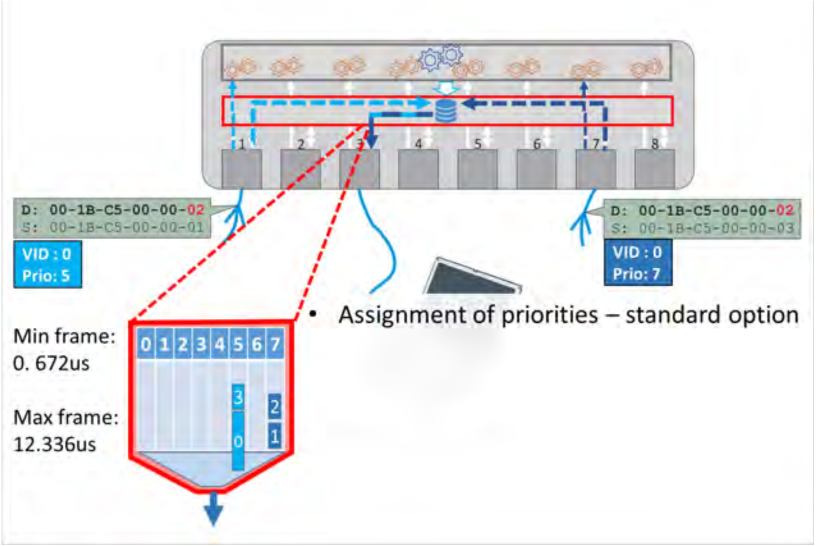
Determinism in WR

- ”White Box” design of WR switch - allows thorough analysis
- Backward-compatible extension of the IEEE 802.1Q std

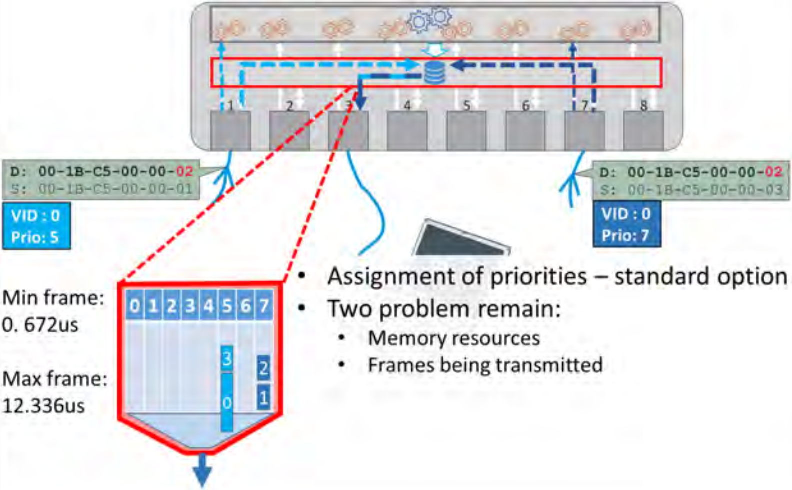
Priorities


1
2
3
4
5
6
7
8
D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-01
D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-03
Min frame:
0. 672us
Max frame:
12.336us
3
2
1
0
PC 2
MAC: 00-1B-C5-00-00-02

Priorities

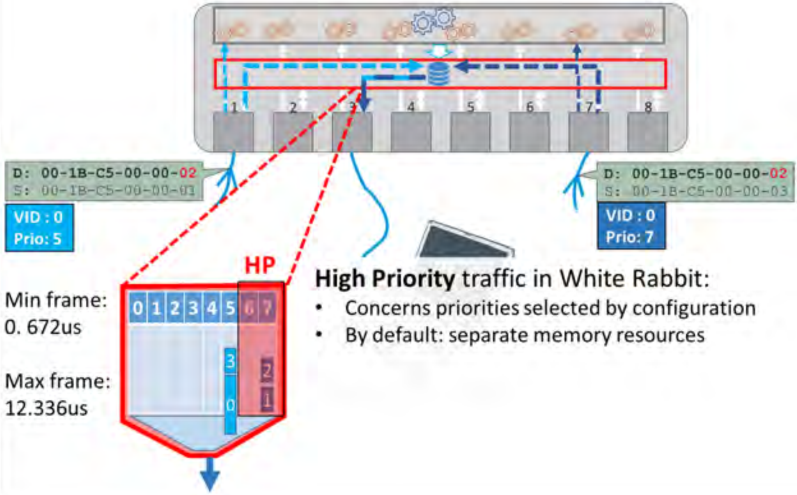

1
2
3
4
5
6
7
8
D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-01
VID : 0
Prio: 5
D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-03
VID : 0
Prio: 7
• Assignment of priorities – standard option
Min frame:
0. 672us
Max frame:
12.336us
0 1 2 3 4 5 6 7
3
0
2
1

Priorities



- Assignment of priorities – standard option
- Two problem remain:
  - Memory resources
  - Frames being transmitted

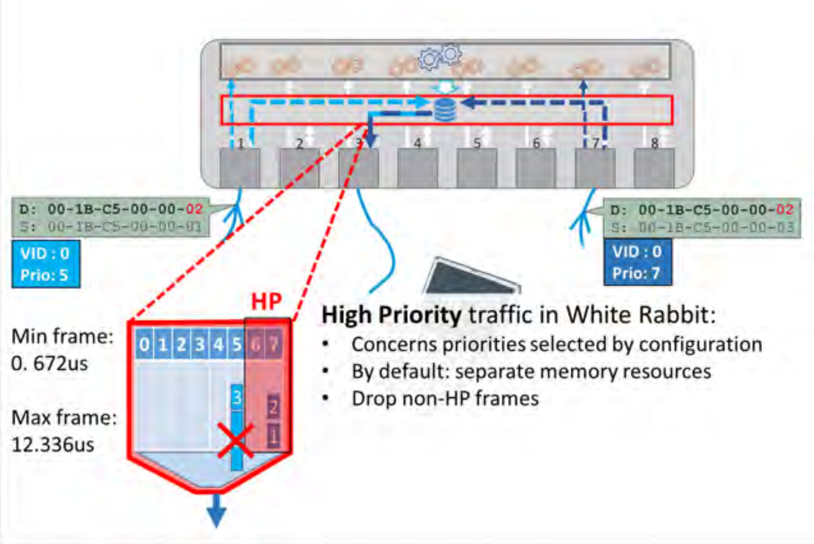
High Priority



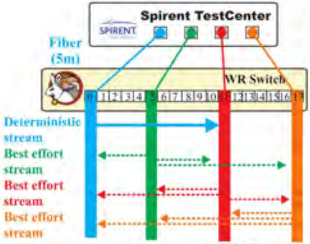
High Priority traffic in White Rabbit:

- Concerns priorities selected by configuration
- By default: separate memory resources

High Priority



WR Switch Latency



Intervening traffic	Latency [us]			
	One switch		Two switches	
	Max	Pk-pk	Max	Pk-pk
No	3.1	0.3	5.8	0.5
WR-PTP	5.6	2.8	8.7	3.9
Non-HP traffic	3.1	0.2	N/A	N/A