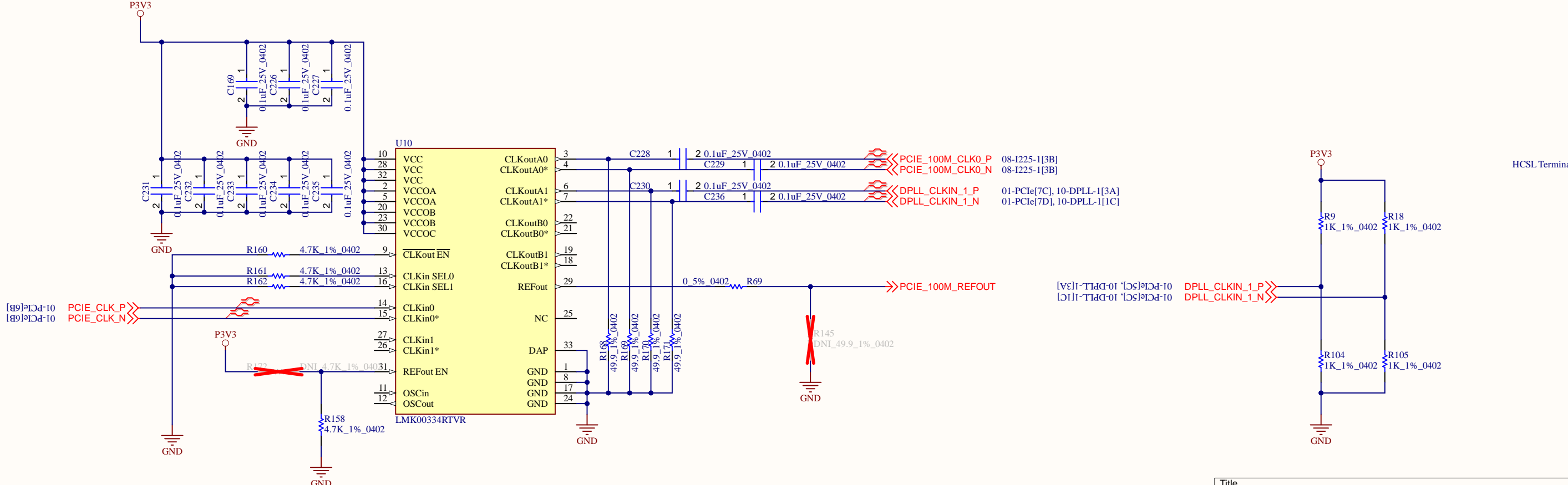
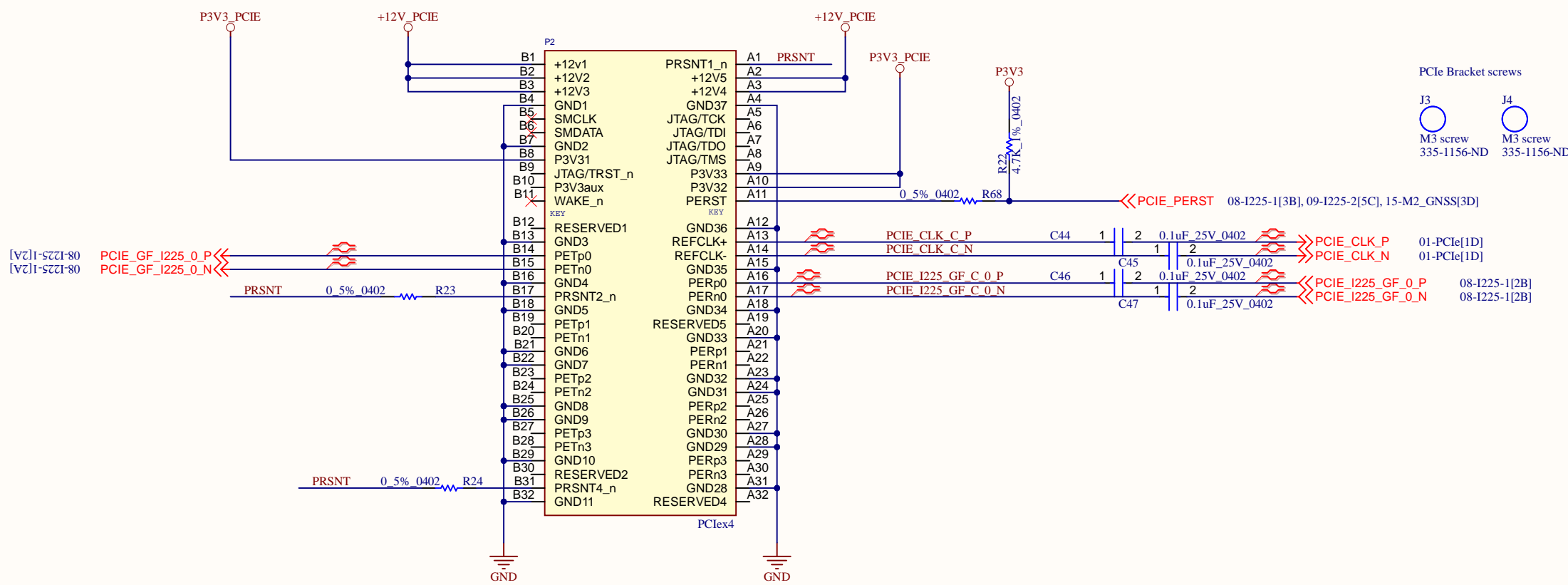


PCIe Connector

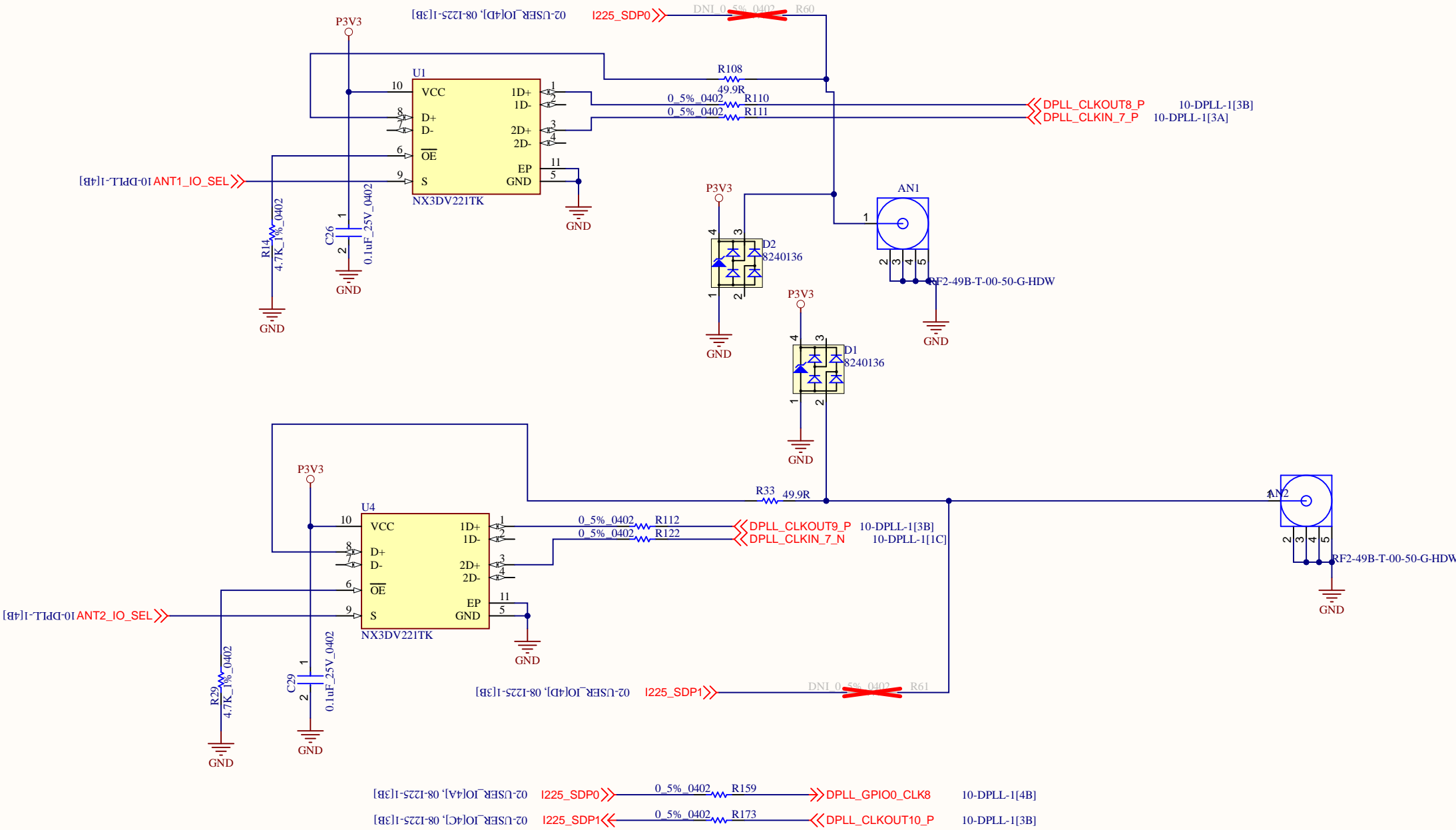


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INPUT/OUTPUT SMA

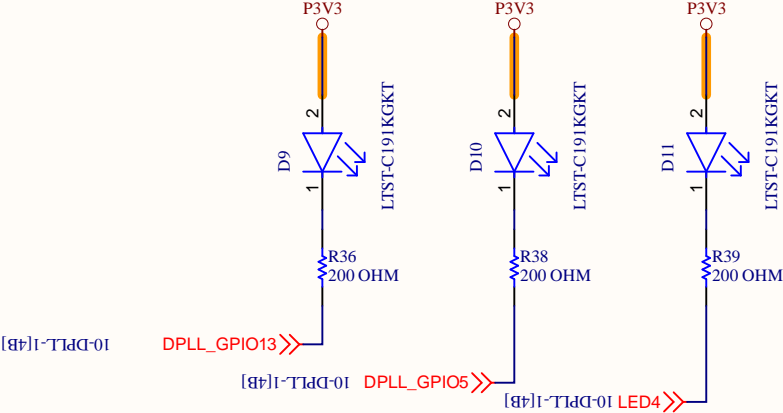
Using USB MUX To select Input vs Output, cheap, lots of options, low prop delay

BOM Option to connect I225 directly
Also BOM options for how DPLL connects to I225 SDP0 and SDP1

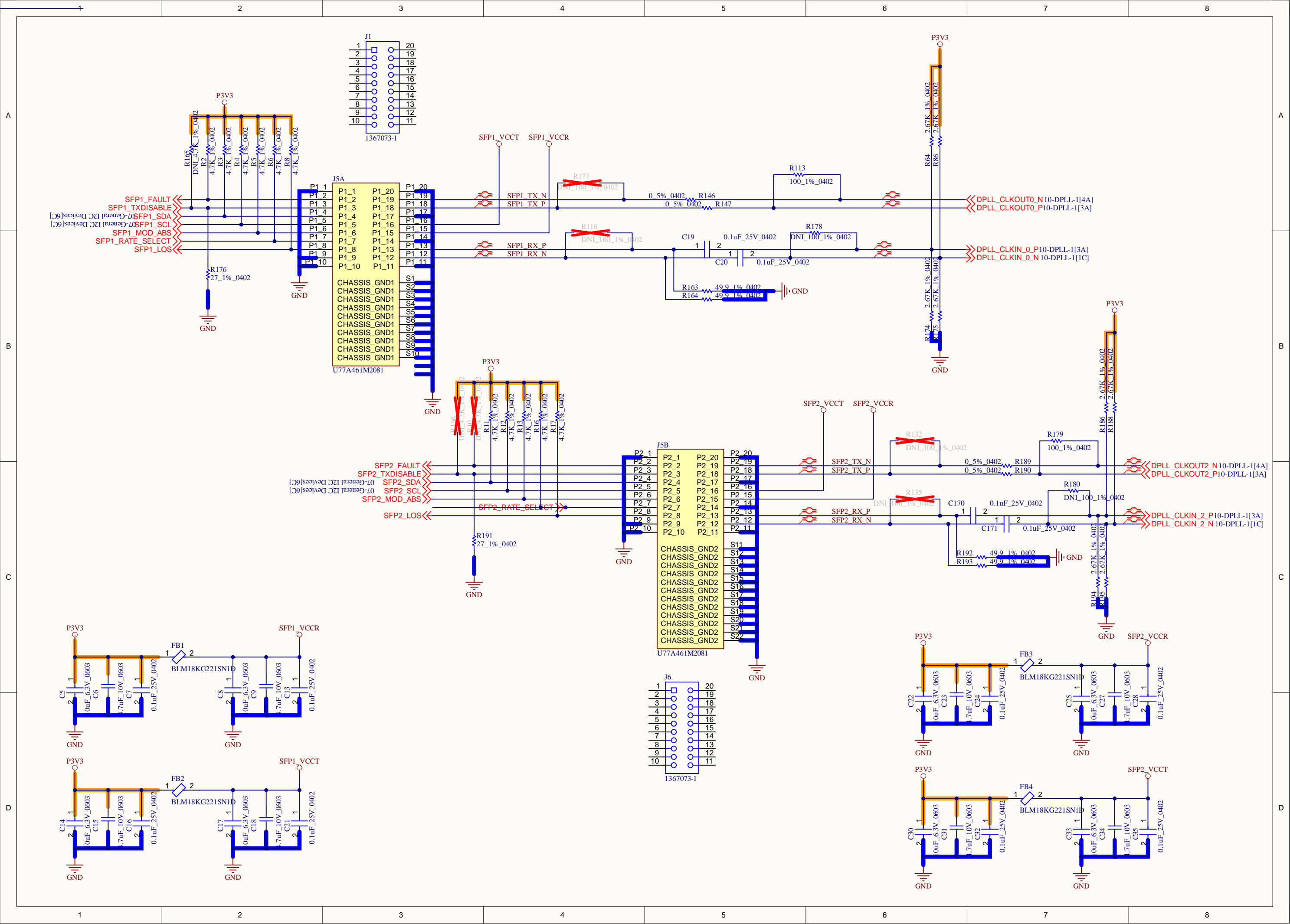


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File:	C:\Documents\102-USER_IO.SchDoc	Drawn By:

SYSTEM STATUS LEDS



Title		
Size A4	Number	Revision
Date:	7.28.2025	Sheet of
File:	C:\Documents\..03-USER_IO_STATU	Drawn By:



A

B

C

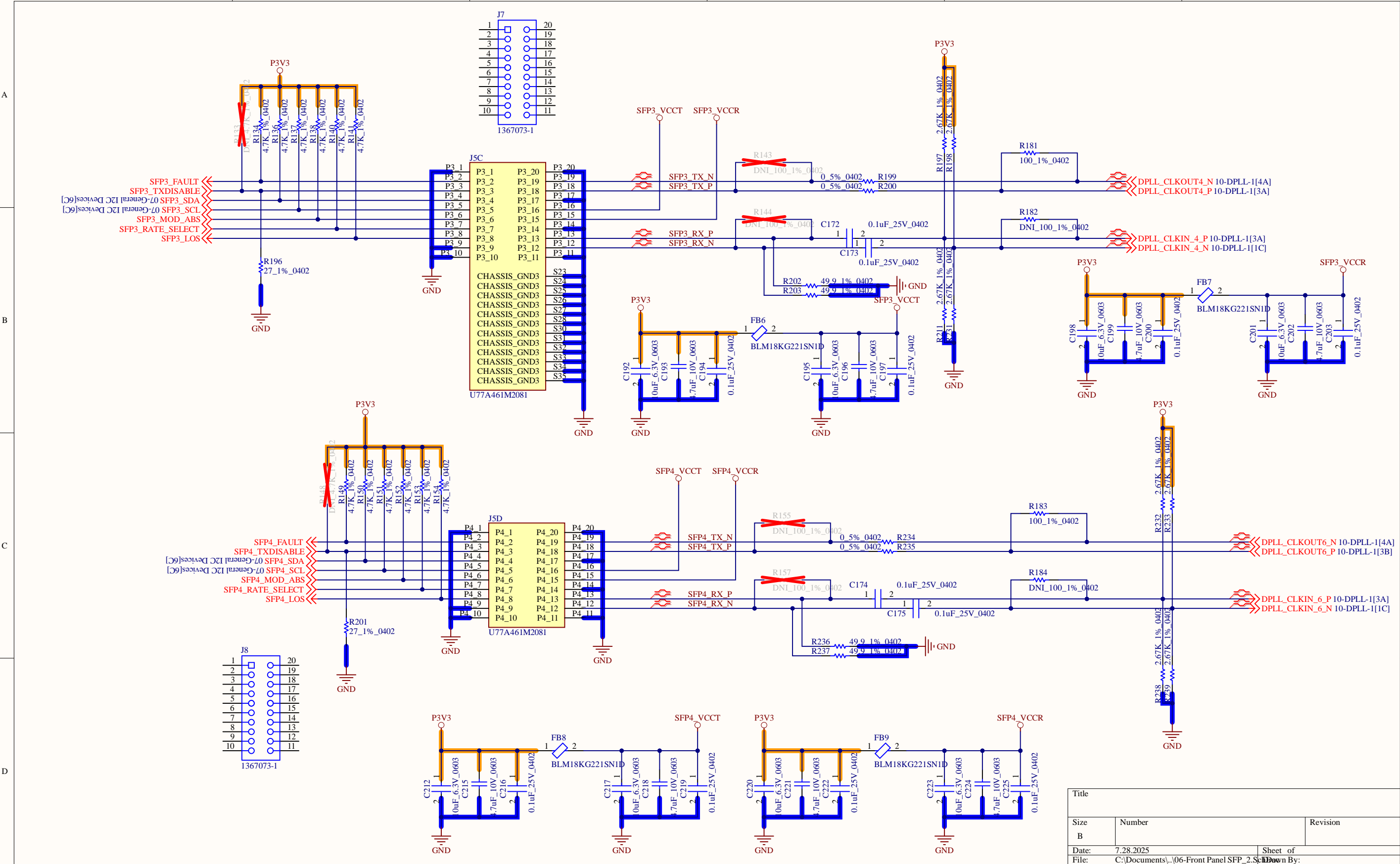
D

A

B

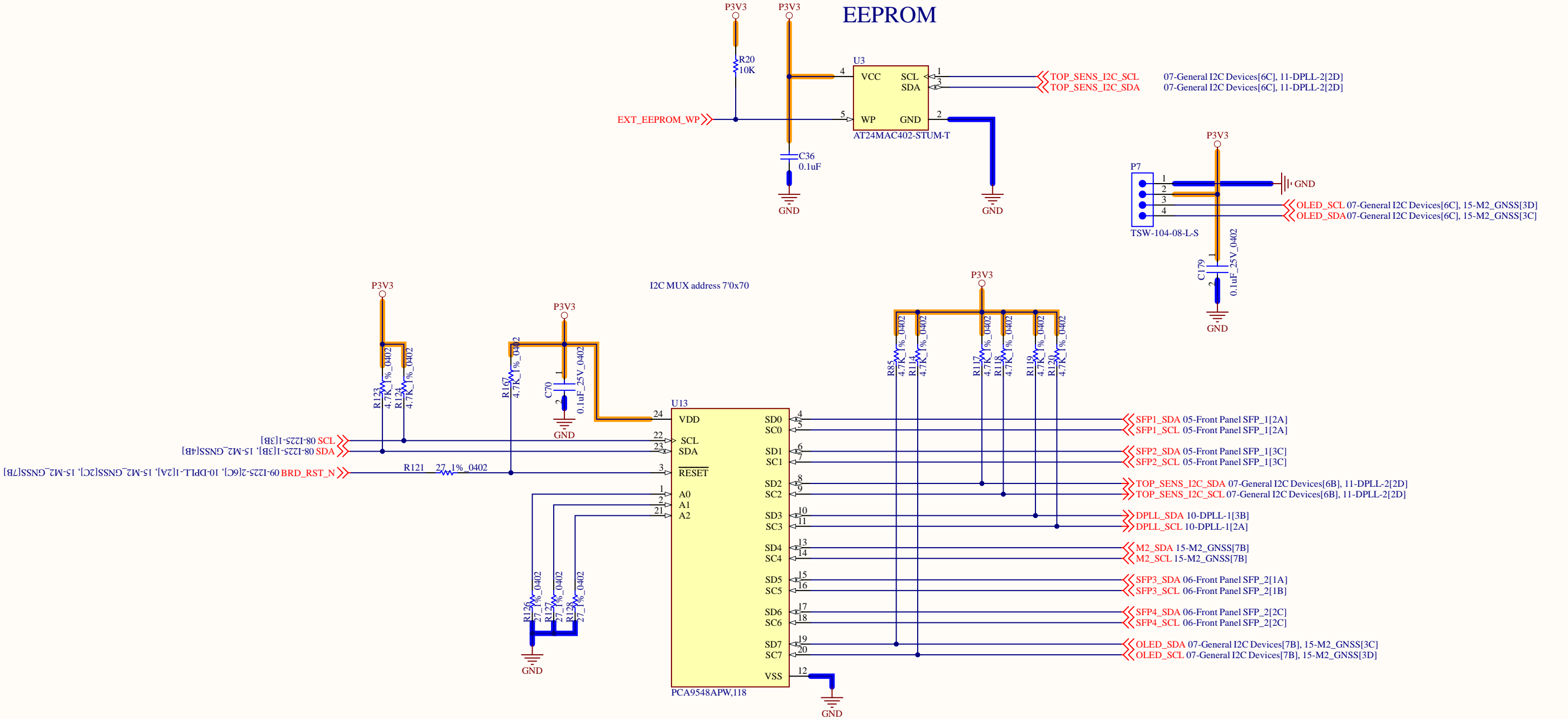
C

D



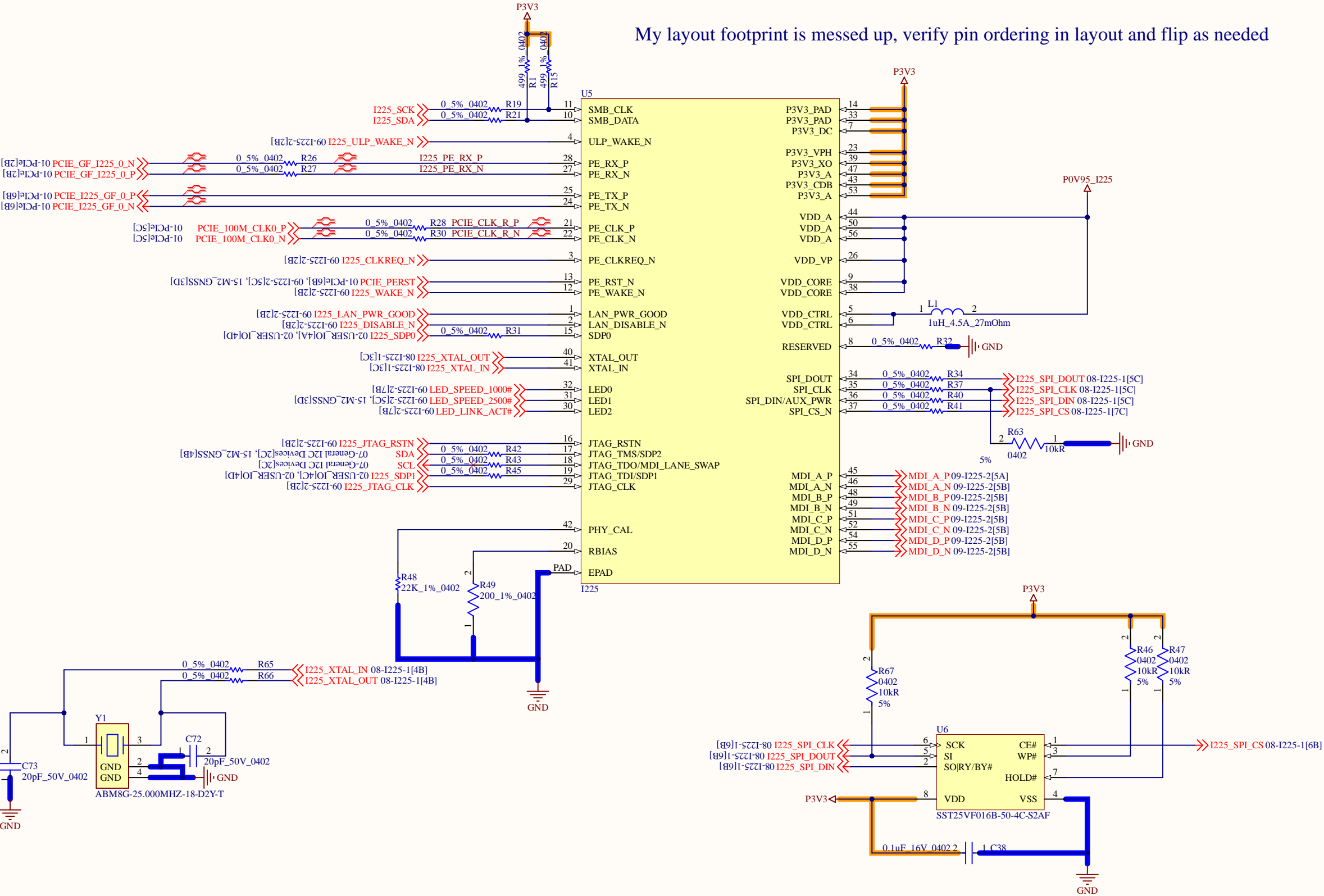
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Size	Number	Revision
B		
Date:	7.28.2025	Sheet of
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EEPROM

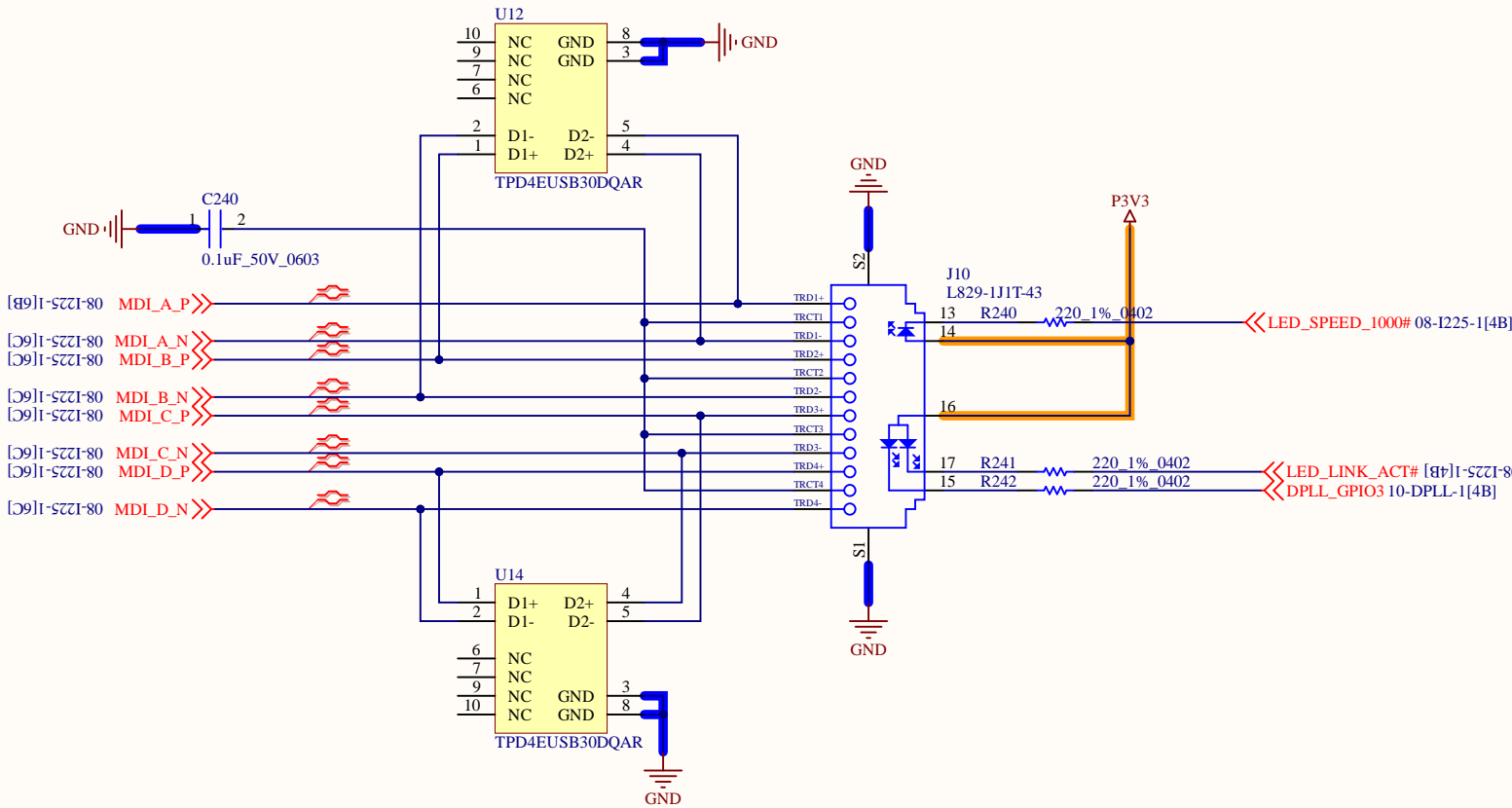
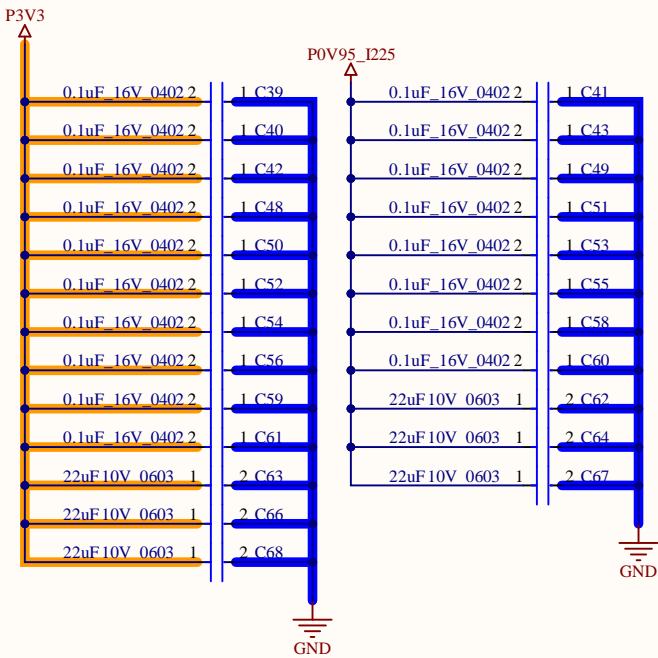
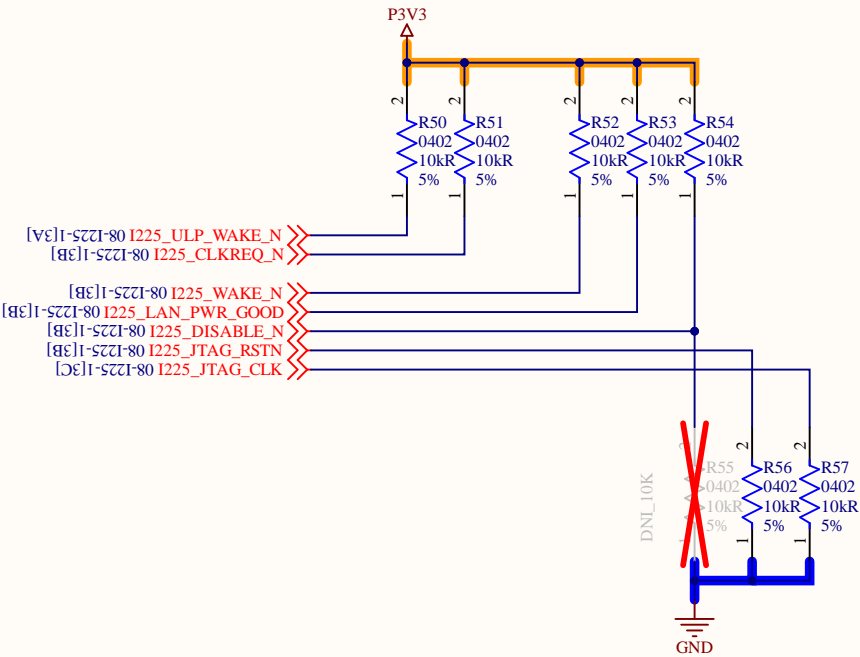


Title		
Size	Number	Revision
A3		
Date:	7.28.2025	Sheet of
File:	C:\Documents\...\07-General I2C Devices	Sheet By:

My layout footprint is messed up, verify pin ordering in layout and flip as needed

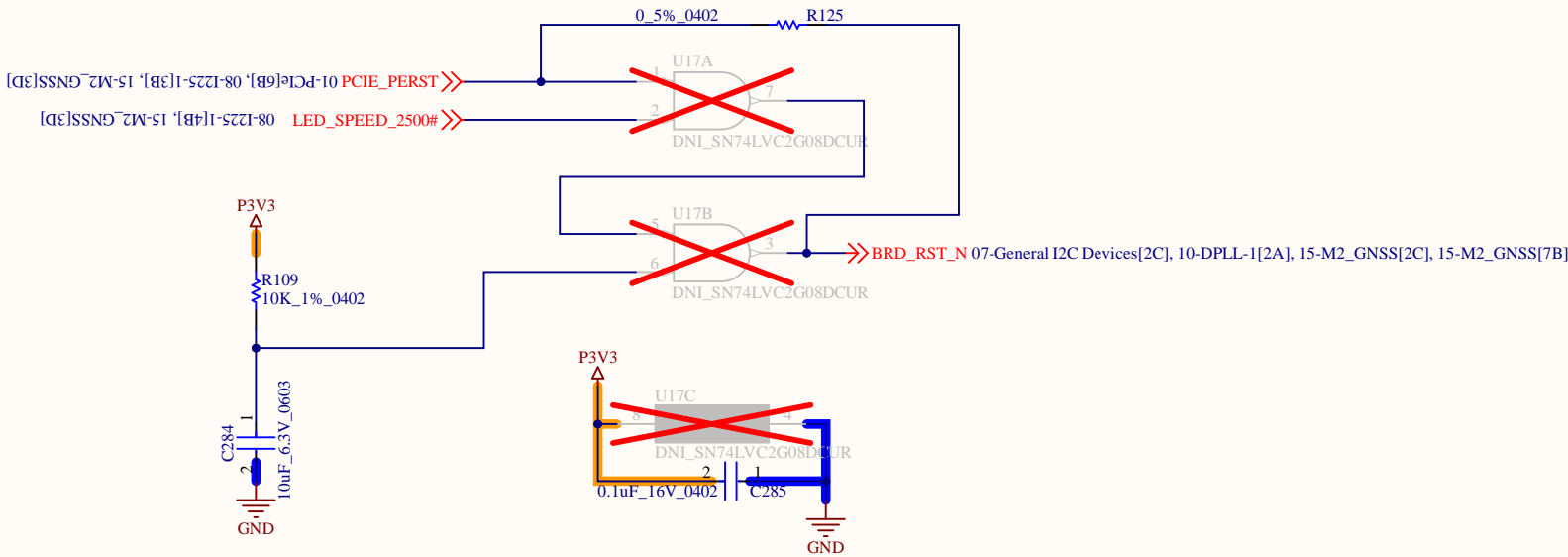


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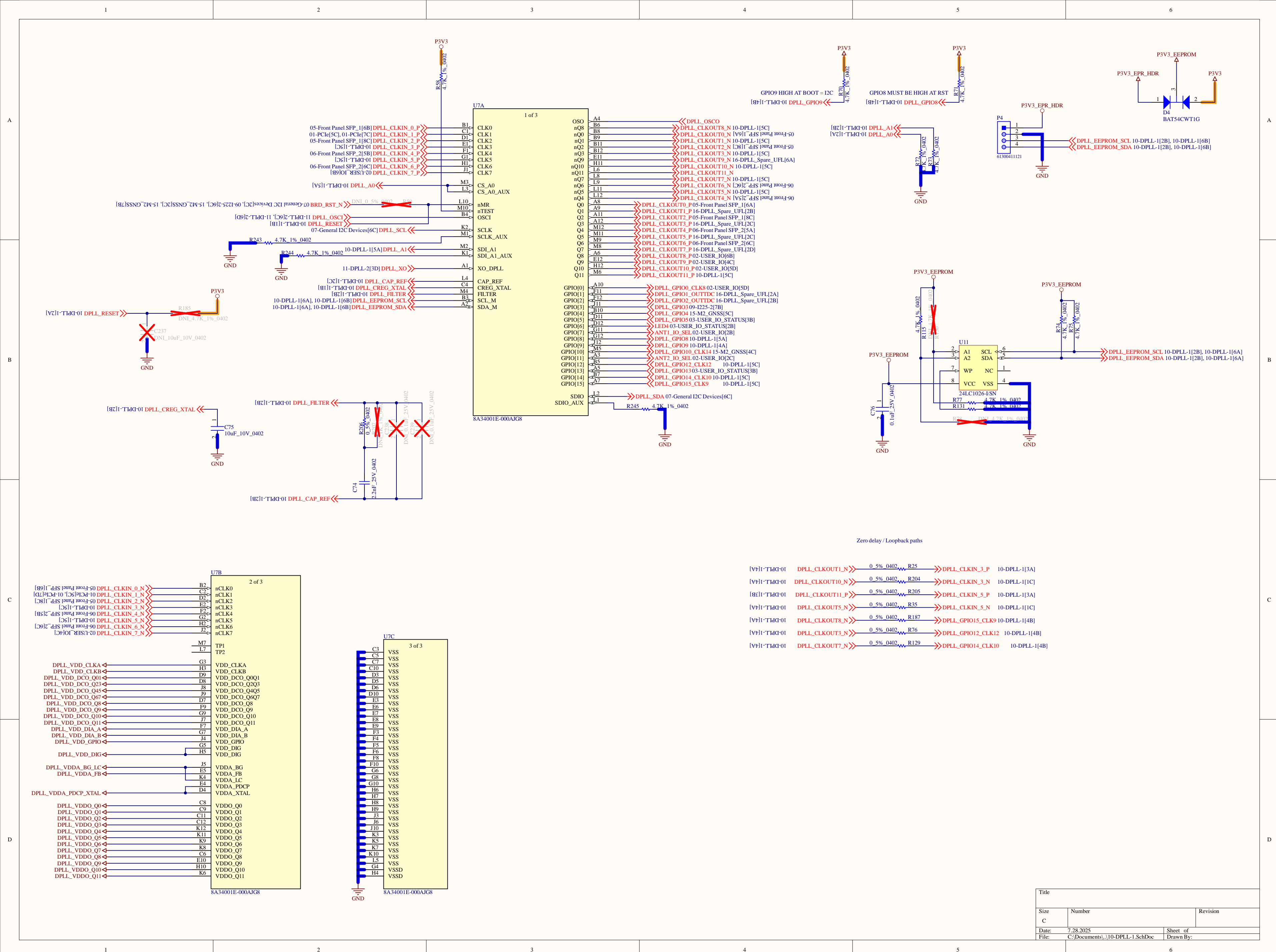


Software board hardware reset

PCIE Reset / SW LED pin / Power on reset



Title		
Size	Number	Revision
A3		
Date:	7.28.2025	Sheet of
File:	C:\Documents\...\09-I225-2.SchDoc	Drawn By:



A

B

C

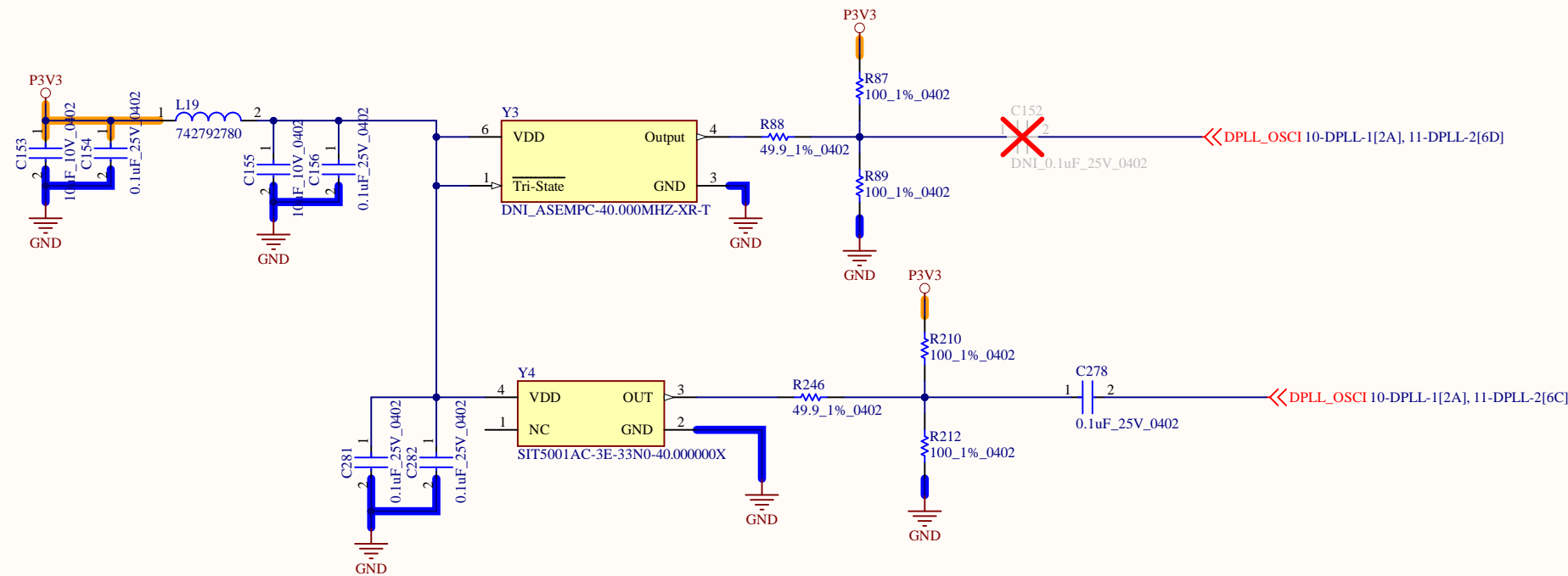
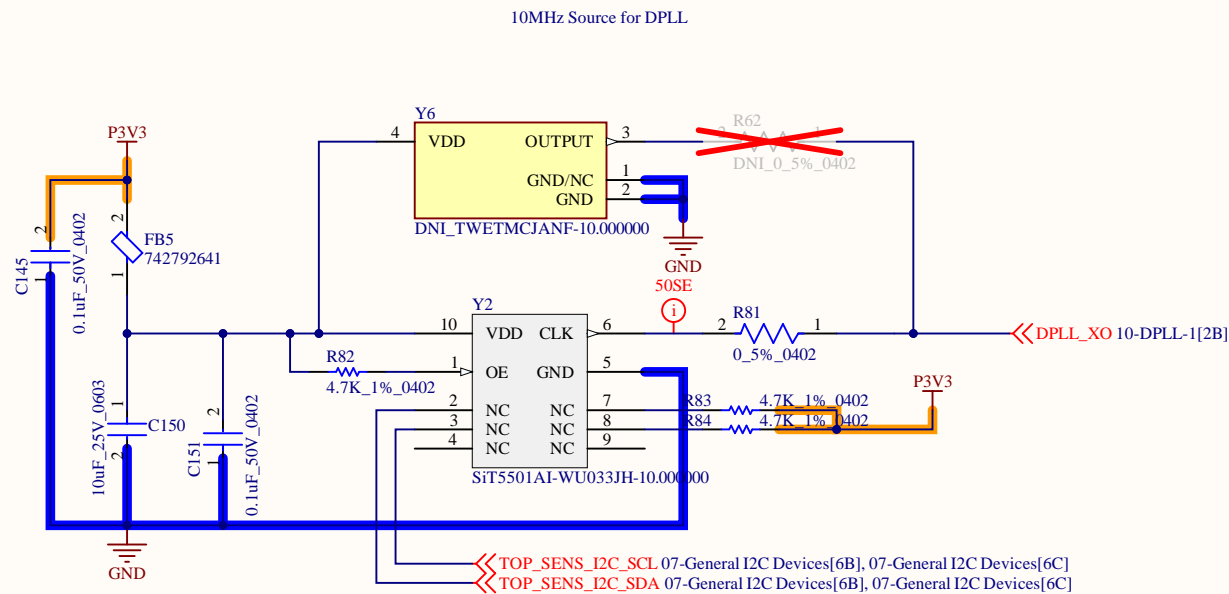
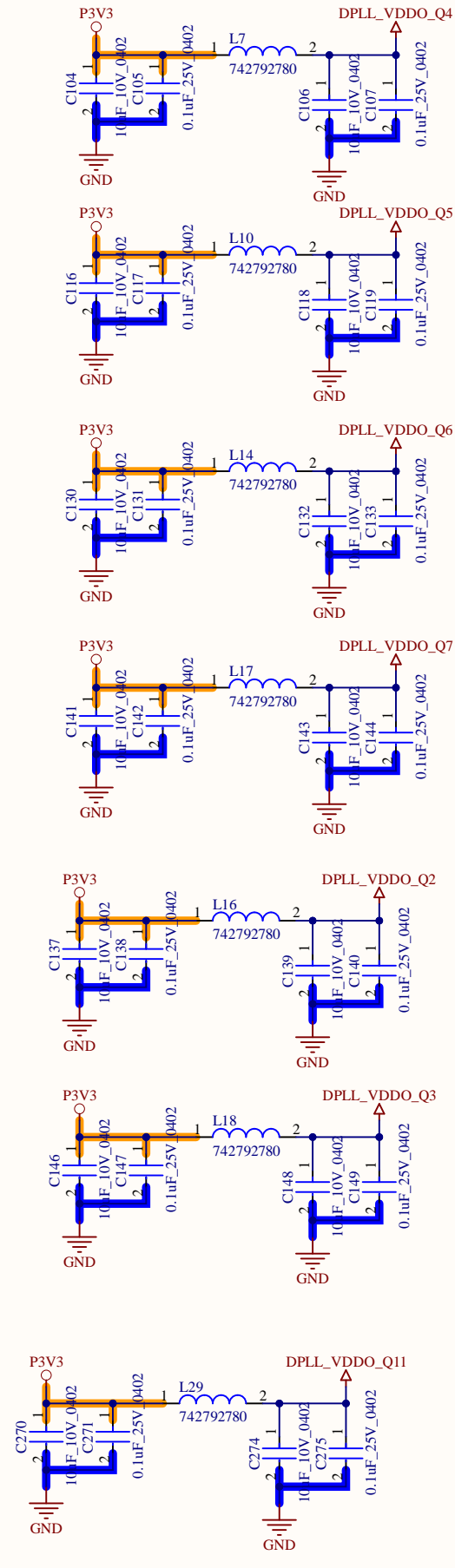
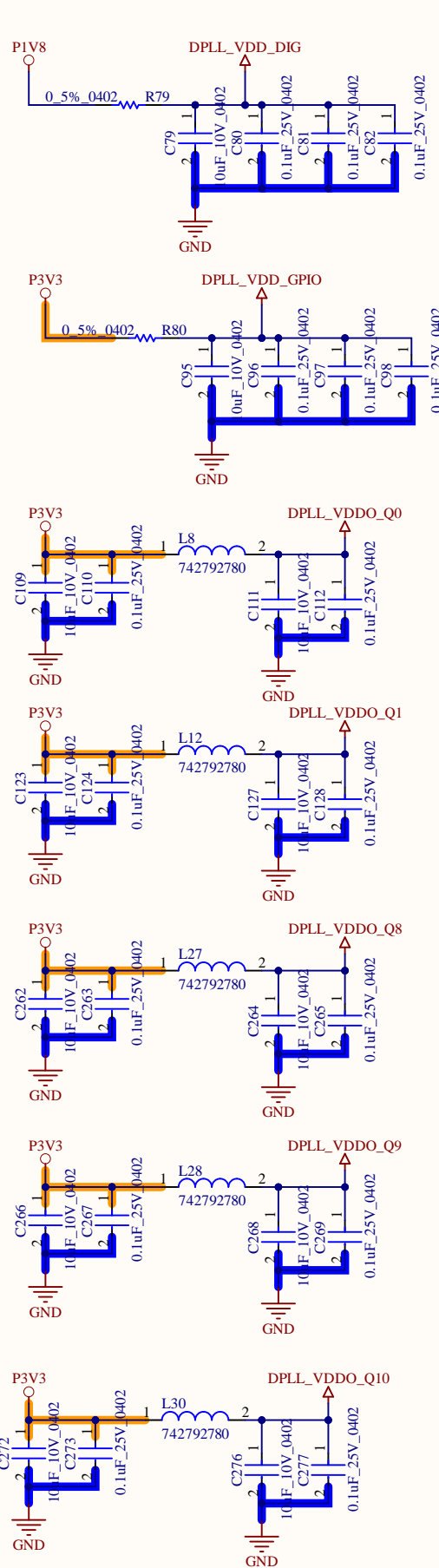
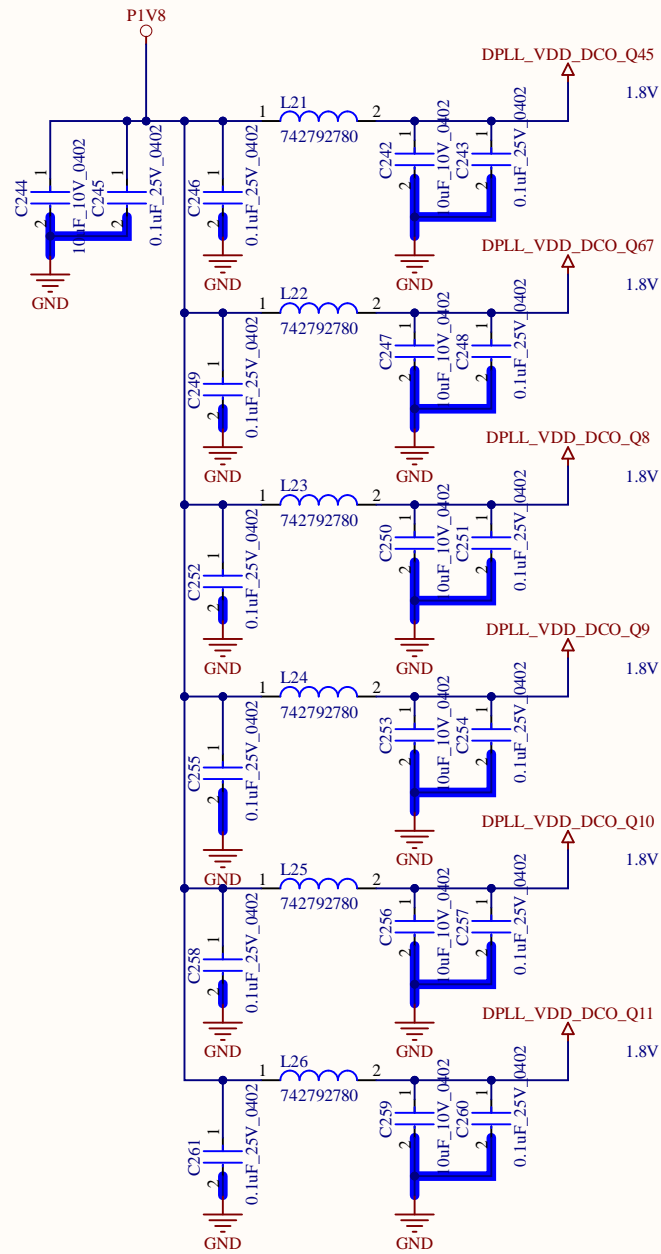
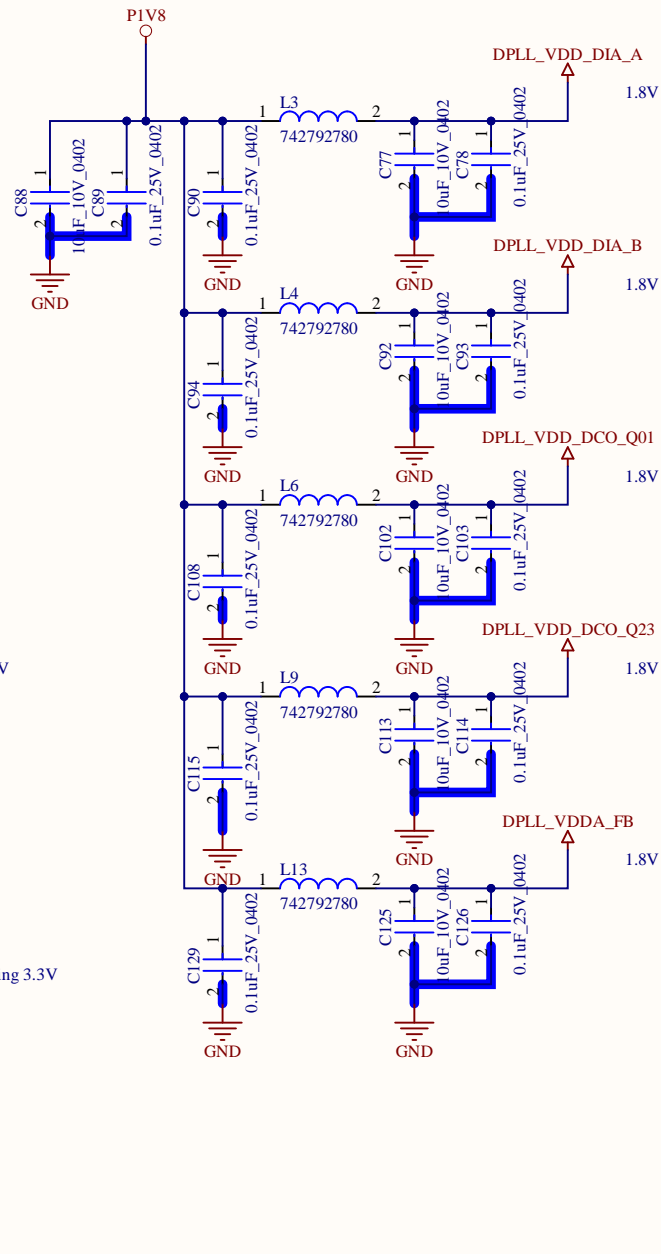
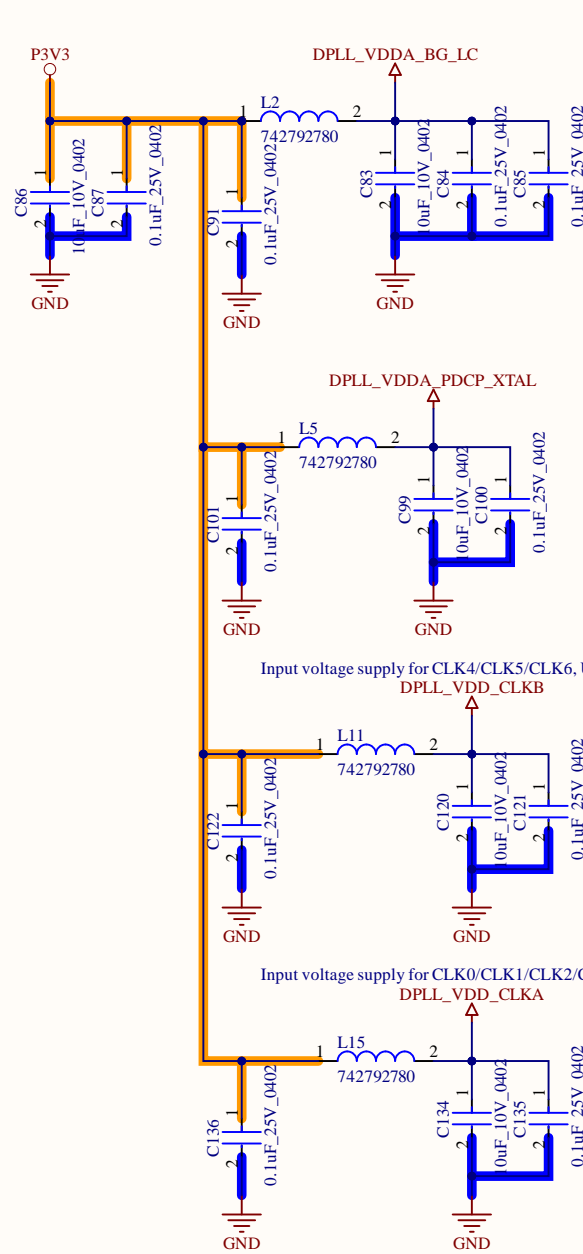
D

A

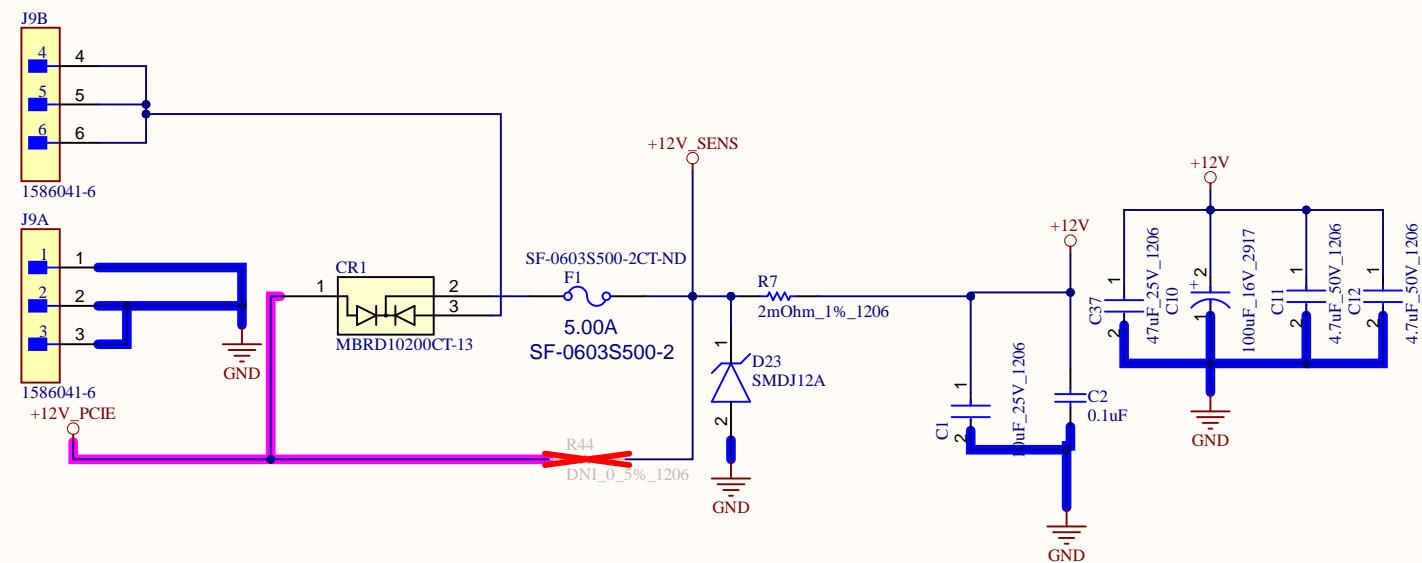
B

C

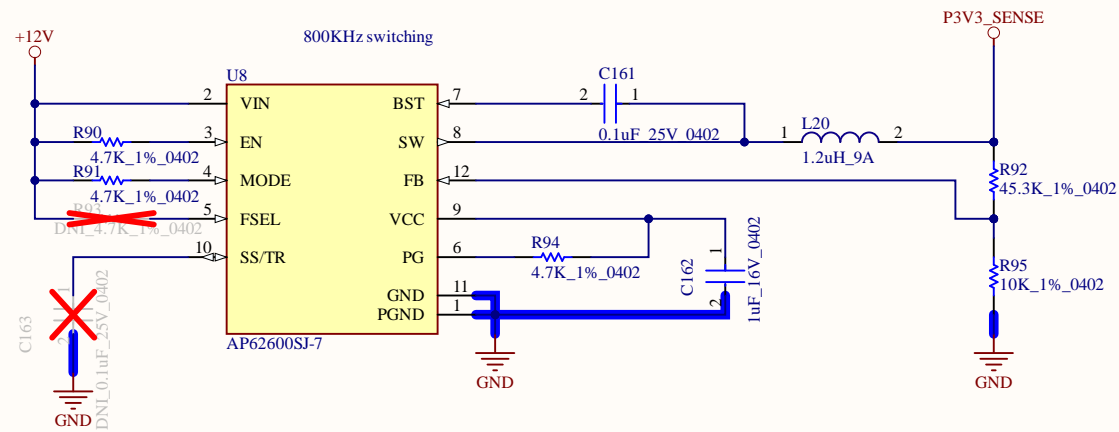
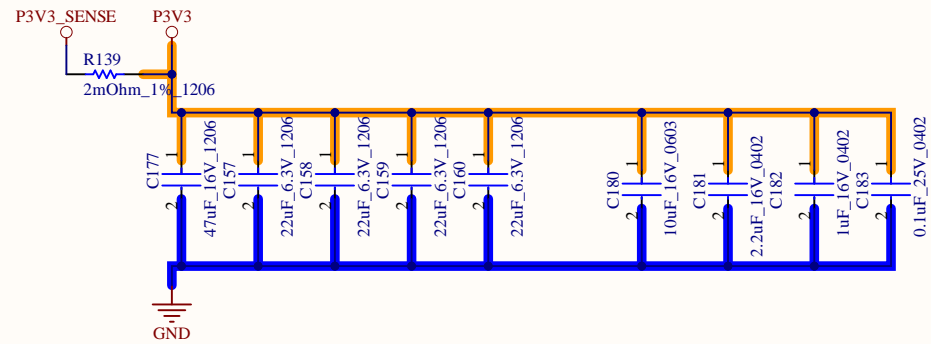
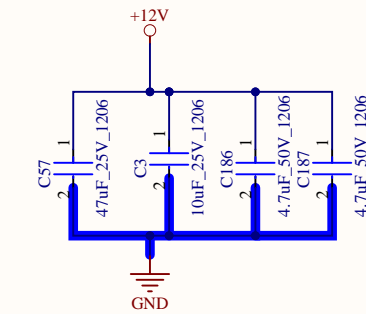
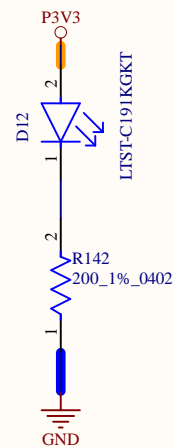
D



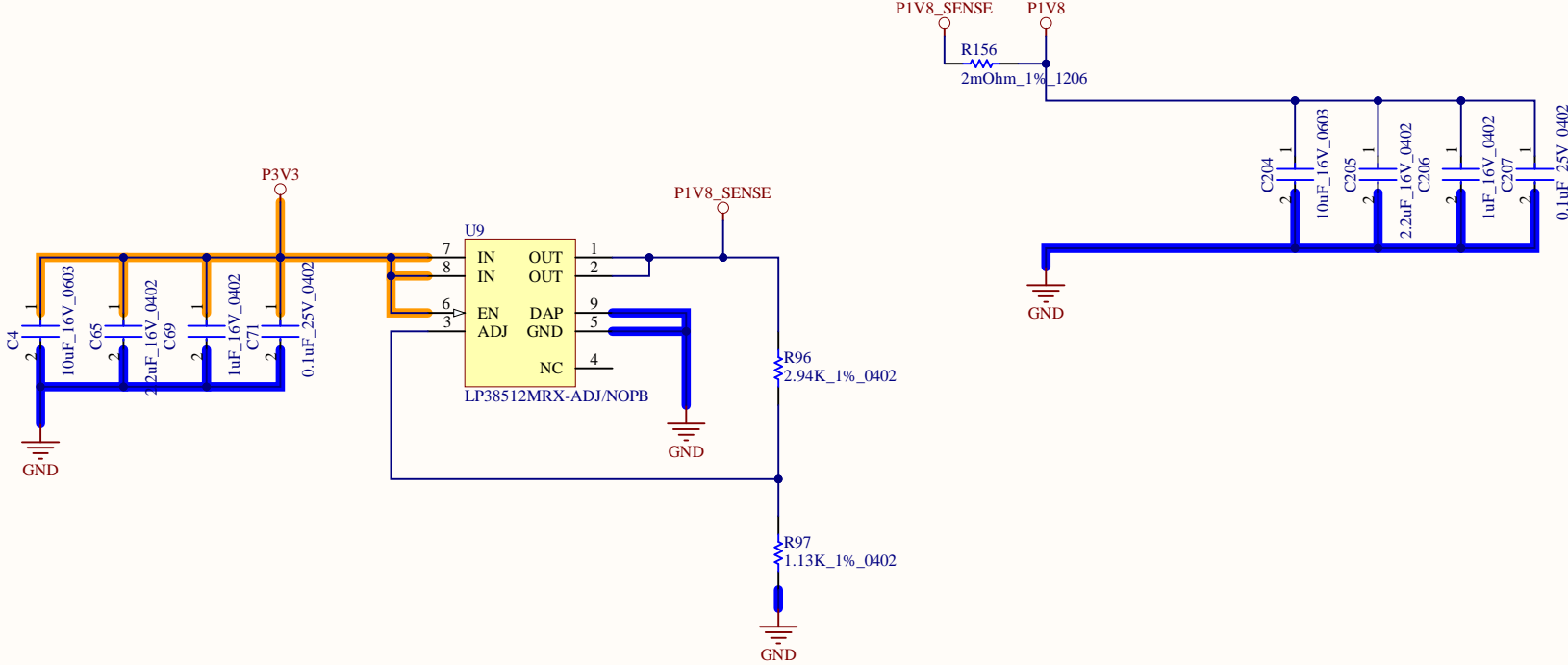
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Date:	7.28.2025	Sheet of
File:	C:\Documents\11-DPLL-2.SchDoc	Drawn By:



Title		
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A3		
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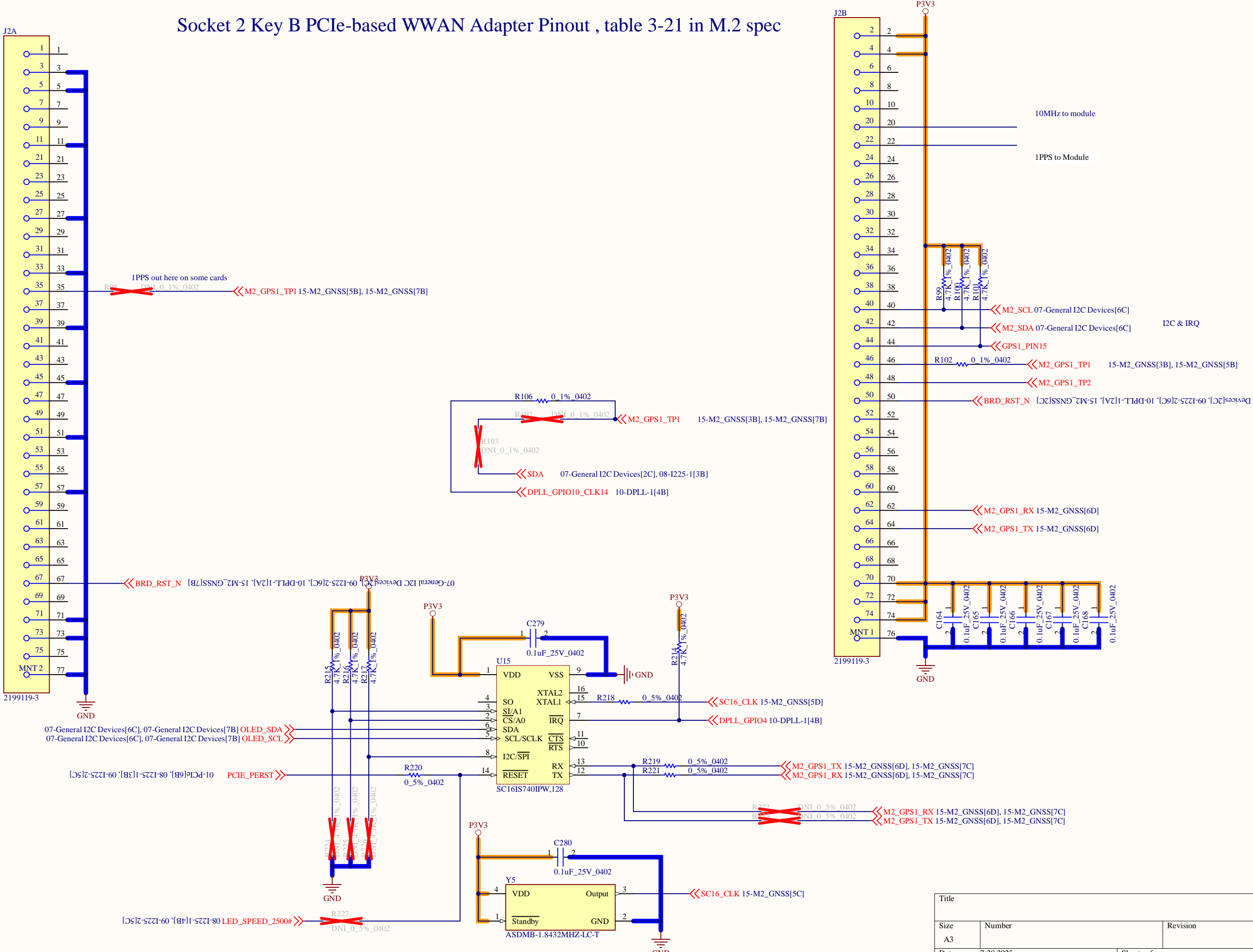


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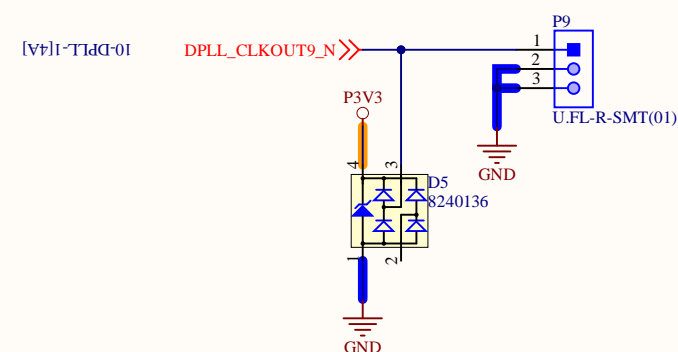
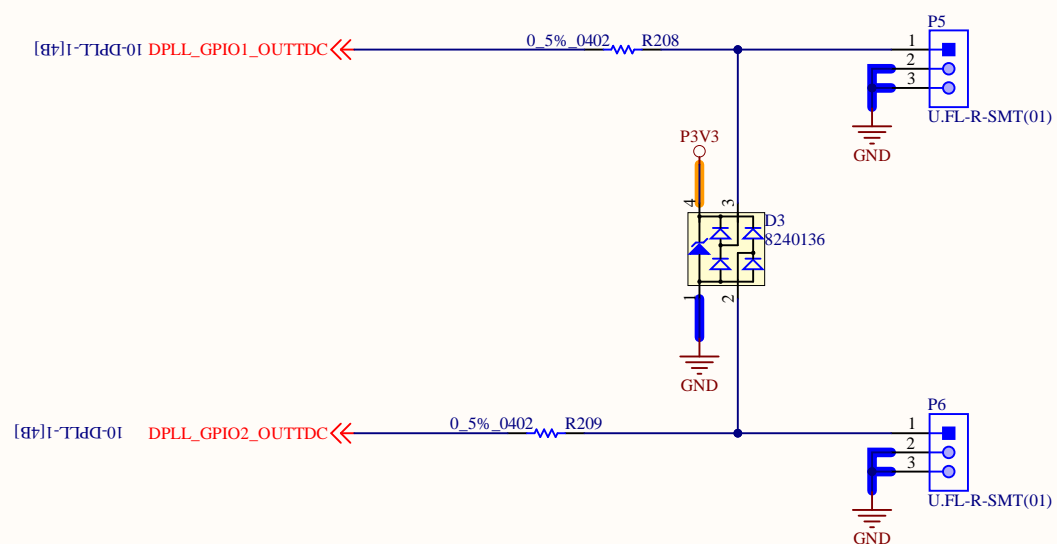


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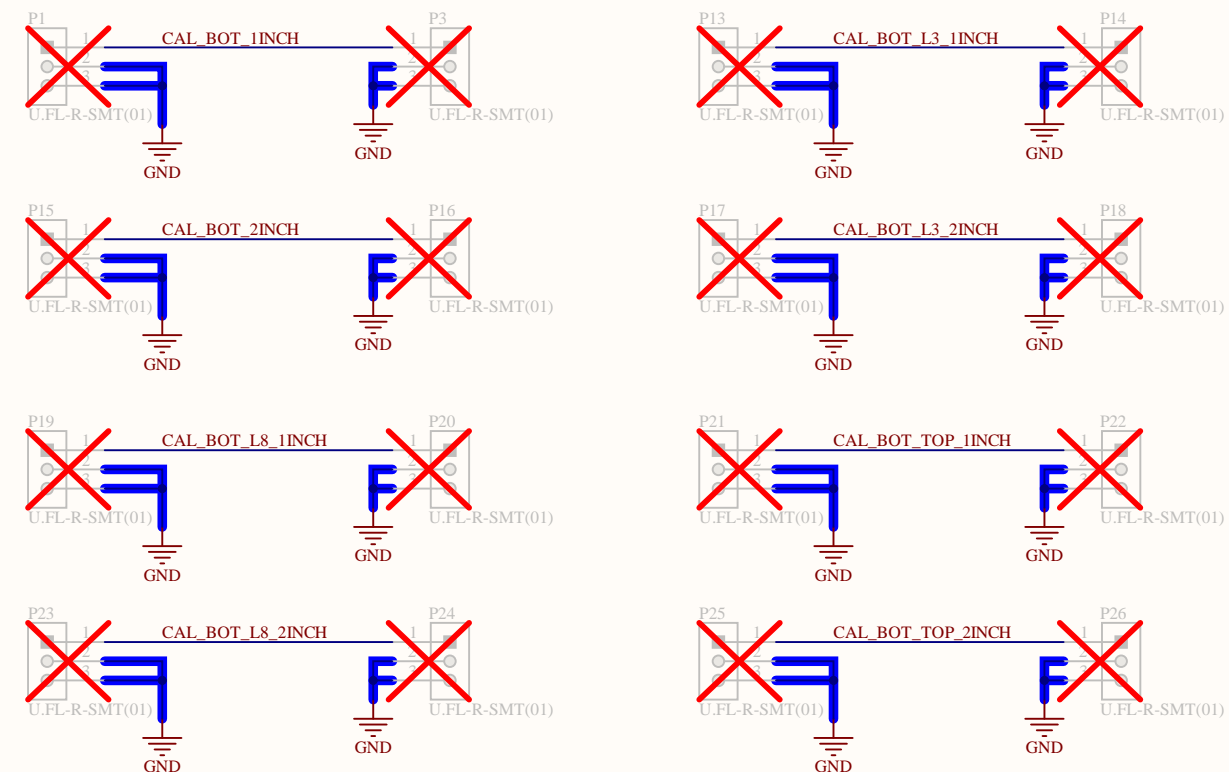
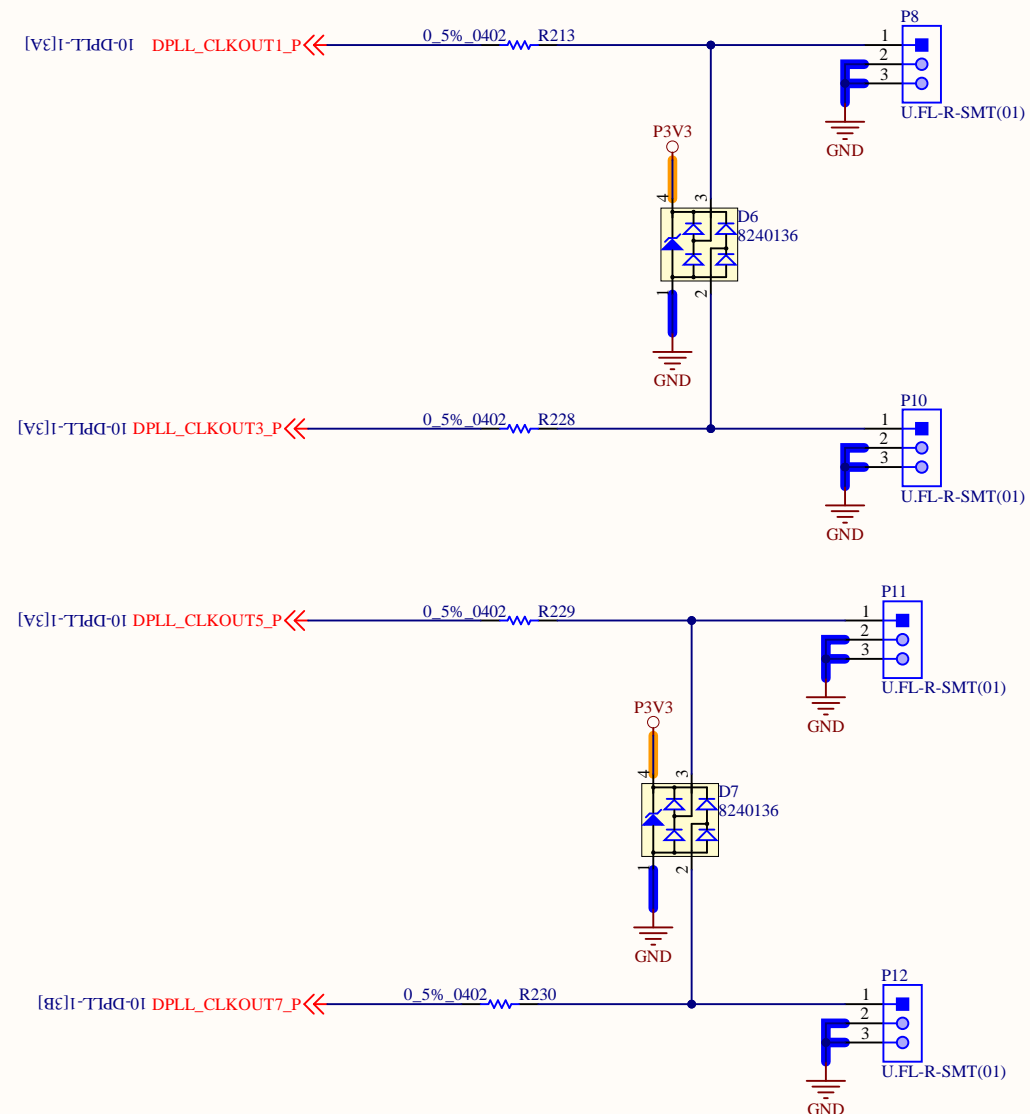
Socket 2 Key B PCIe-based WWAN Adapter Pinout , table 3-21 in M.2 spec



Title		
Size A3	Number	Revision
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File:	C:\Documents\115-M2 GNSS SchDoc	Drawn By:



Calibration traces



Title		
Size A3	Number	Revision
Date:	7.28.2025	Sheet of
File:	C:\Documents\...\16-DPLL Spare UFL Sch... Drawn By:	