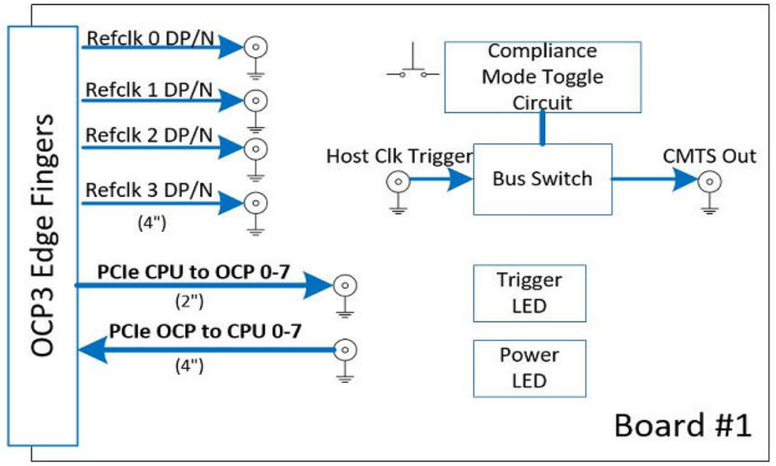
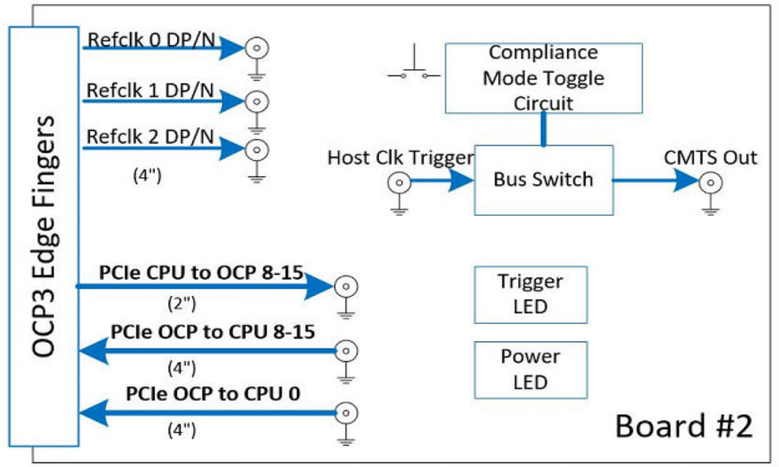
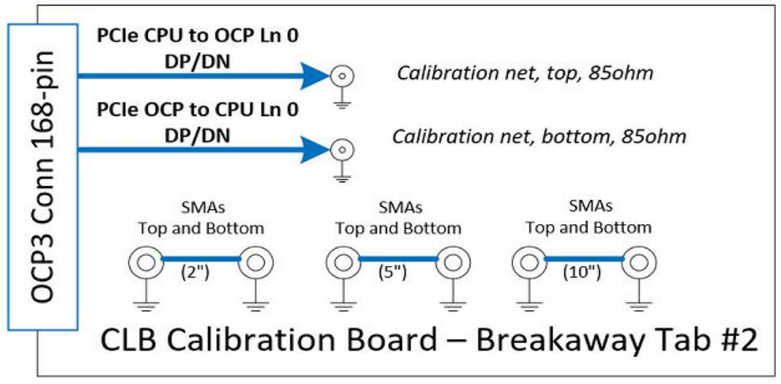
OCP 3.0 - PCIe CLB Gen 5 - X02

OCP3 Load Compliance Board (CLB)





Note: Board Refclk 3 removed to make room for PCIe OCP to CPU 0



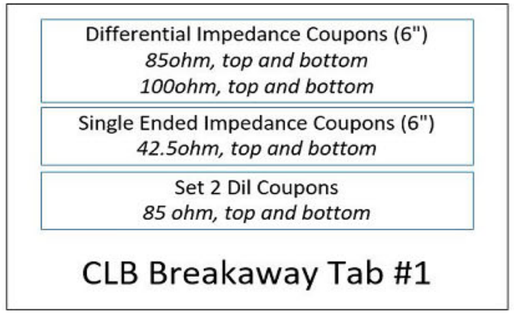


Table of Contents

PWA: 83DG8
PWB: RX1NY
Sch: C7D95

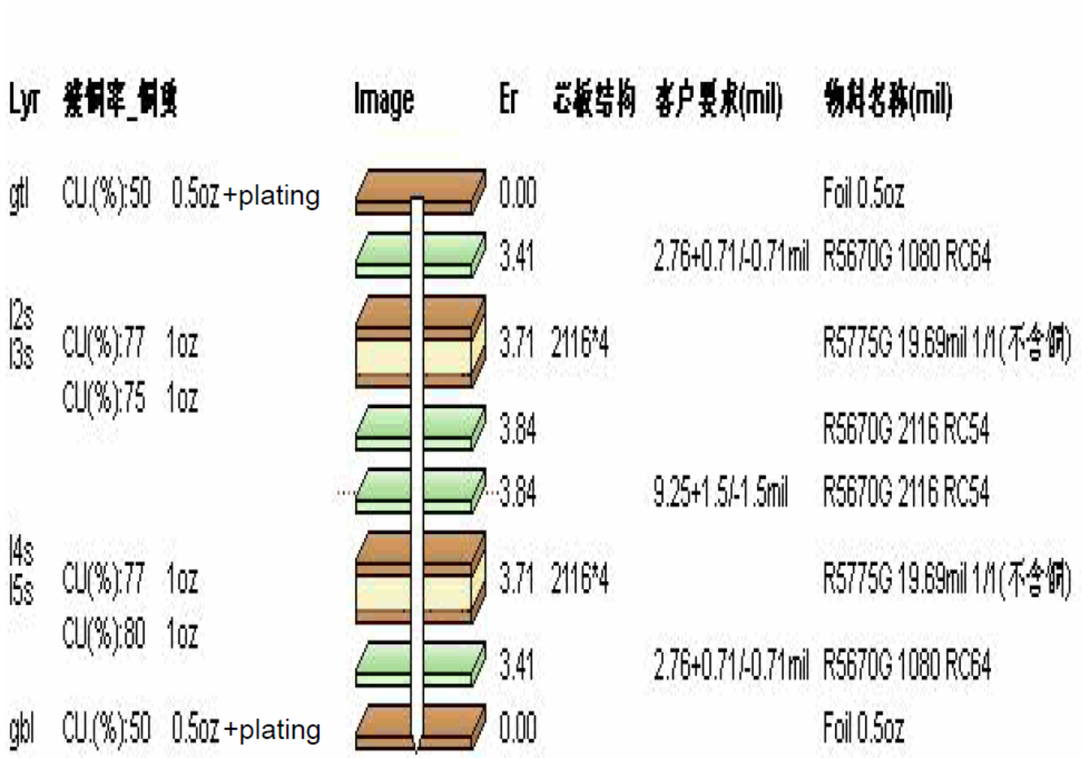
Change History:
X00 - Initial design
X01 - Schematic updated for new MMPX connectors, new stackup, CMTS circuit, Gen 5 capable clock buffer
X02 - PCB material information updated (page 2), no schematic changes

ADD C7D95 Schematic
ADD RX1NY PWB

TITLE	OCP3 SI GEN 5 RX CLB
DWG NO.	C7D95
REV.	X02
DATE	Wednesday, June 28, 2023
SHEET	1 of 12

Stackup

叠板图：



Finish Board Thickness(mil): 62.99+ 6.30/- 6.30 (over fingers)

Single Ended

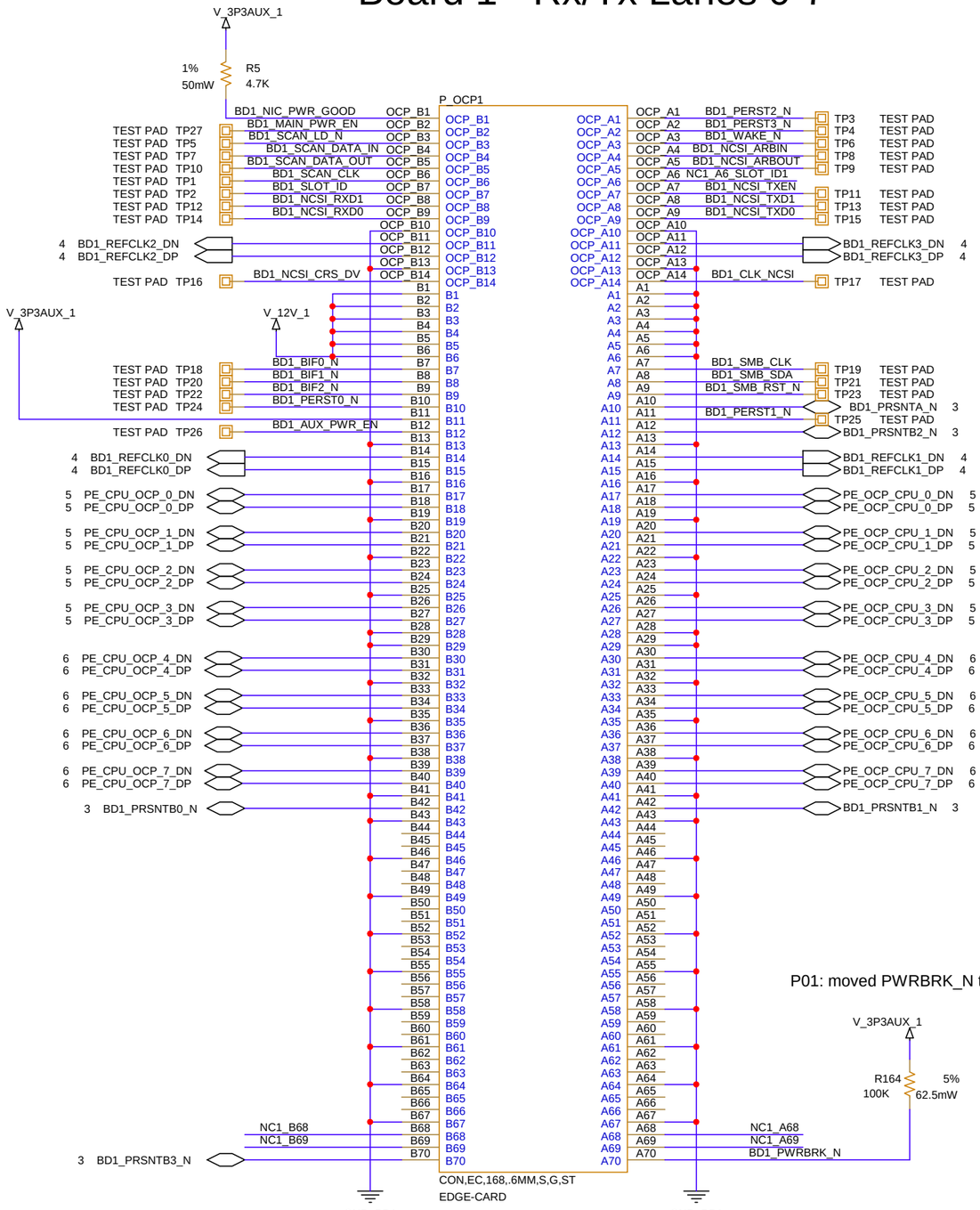
Index	Layer	Imp Model	WithCoat	Ref Layer	Orginal LW/LS(mil)	Adjusted LW/LS(mil)	Adjusted Imp(ohm)	Org Imp (ohm)
1	L1		Y	L2	ORG_LW: 6.000	ADJ_LW: 6.595	42.50	42.5+/-10%
2	L6		Y	L5	ORG_LW: 6.000	ADJ_LW: 6.600	42.81	42.5+/-10%

Differential

Index	Layer	Imp Model	WithCoat	Ref Layer	Orginal LW/LS(mil)	Adjusted LW/LS(mil)	Adjusted Imp(ohm)	Org Imp (ohm)
3	L1		Y	L2	ORG_LW: 5.000 ORG_S: 7.000	ADJ_LW: 5.455 ADJ_S: 6.545	84.99	85.0+/-10%
4	L6		Y	L5	ORG_LW: 5.000 ORG_S: 7.000	ADJ_LW: 5.500 ADJ_S: 6.500	85.08	85.0+/-10%

TITLE OCP3 SI GEN 5 RX CLB
DWG NO. C7D95 REV. X02
DATE Wednesday, June 28, 2023 SHEET 2 of 12

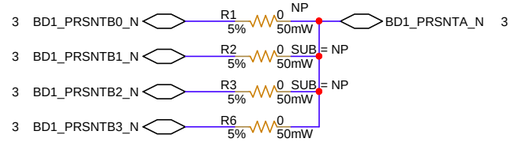
Board 1 - Rx/Tx Lanes 0-7



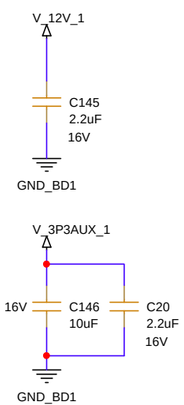
P01: moved PWRBRK_N to pin A70

ROOM = BRD1

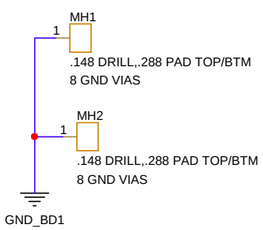
PRSNTB[3:0]_N = 1110 -> x8 link



P01: pin A6 is now SLOT ID1



Faceplate Mtg Holes



WARRANTY NOTE :

THIS CONTRIBUTION IS PROVIDED WITHOUT WARRANTY OF ANY KIND AND IS PROVIDED AS-IS, AND THE CONTRIBUTOR DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AS WELL AS ANY WARRANTIES EXPRESS, IMPLIED, OR STATUTORY.

TITLE	OCP3 SI GEN 5 RX CLB
DWG NO.	C7D95
REV.	X02
DATE	Wednesday, June 28, 2023
SHEET	3 of 12

Board 1 - Rx/Tx Lanes 0-7 (cont)

RSVD TEST

BD1_BTN_NC R7 0 50mW 5% BD1_BUS_SEL
SUB = NP
BD1_BTN_NO R8 0 50mW 5% BD1_555_TRI
SUB = NP

V_3P3AUX_1 R9 10K 1% 62.5mW BD1_BTN_NC
SW1 SPDT PUSHBUTTON BD1_BTN_NO GND_BD1

V_3P3AUX_1 R17 10K 1% 62.5mW

V_3P3AUX_1 C13 16V 6.3V 100uF C147 10uF C15 2.2uF 16V GND_BD1

V_3P3AUX_1 C2 10V 0.1uF U1 GND_BD1
U1 NC7SZ00 SC70 (A VCC GND Y, B)

V_3P3AUX_1 C8 10V 0.1uF U6 GND_BD1
U6 NC7SZ00 SC70

P2 2X1,VERT,HDR 2.54MM PITCH 78511-402HLF GND_BD1
R12 1K 1% 50mW

V_3P3AUX_1 C5 10V 0.1uF U5 GND_BD1
U5 NC7SZ00 SC70

C10 10uF 16V GND_BD1

V_3P3AUX_1 C3 10V 0.1uF U2 GND_BD1
U2 NC7SZ00 SC70

V_3P3AUX_1 C9 10V 0.1uF U7 GND_BD1
U7 NC7SZ00 SC70

V_3P3AUX_1 C4 10V 0.1uF U3 GND_BD1
U3 NC7SZ00 SC70

P1 2X1,VERT,HDR 2.54MM PITCH 78511-402HLF GND_BD1
R10 1K 1% 50mW

R14 0 5% 50mW BD1_555_TRI
BD1_555_OUT
BD1_555_RST_N

V_3P3AUX_1 R15 1K 1% 50mW C7 10uF 16V GND_BD1

U4 LMC555 SO8
GND TRIGGER_N OUT RESET_N V+ DISCHARGE THRESHOLD CNTRL_VLT
GND_BD1

V_3P3AUX_1 C1 10V 0.1uF GND_BD1

BD1_555_DISCHARGE

V_3P3AUX_1 R13 1K 1% 50mW R11 10K 1% 62.5mW C6 10uF 16V GND_BD1

R16 1K 1% 50mW BD1_555_OUT_JP P3 2X1,VERT,HDR 2.54MM PITCH 78511-402HLF GND_BD1

R18 0 5%

V_3P3AUX_1 R158 10K 1% 62.5mW NP P13 2X1,VERT,HDR 2.54MM PITCH 78511-402HLF GND_BD1

BD1_BUS_SEL

U24 SY75603ATWL VQFN16
IN_p IN_n NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 GND EPAD VDD OE0b OUT0_p OUT0_n OE1b OUT1_p OUT1_n
GND_BD1

V_3P3AUX_1 C16 0.1uF 10V
16V C163 1uF NP
GND_BD1 GND_BD1

CLK1_TRIG_SIGNAL_DP C11 10V 0.1uF CLK1_TRIG_SIGNAL_C_DP
CLK1_TRIG_SIGNAL_DN C12 10V 0.1uF CLK1_TRIG_SIGNAL_C_DN

R19 24.3 1% 62.5mW CLK1_TRIG_SIGNAL_R_DP

V_3P3AUX_1 R167 1% 10K 62.5mW

V_3P3AUX_1 C166 U26 0.1uF 10V GND_BD1
NC7SZ14 SOT353

V_12V_1 R154 1% 1K 50mW C150 16V 10uF
DS_BD1_TRIG GRN APH1608-TD47 0603
Q1 2N7002K SOT23

CMTS IN

P_BD1_TRIG_IN_P COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
CLK1_HOST_TO_TRIGGER_DP C148 10V 0.056uF SUB = NP GND_BD1

P_BD1_TRIG_IN_N COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
CLK1_HOST_TO_TRIGGER_DN C149 10V 0.056uF SUB = NP GND_BD1

CMTS OUT

P_BD1_CMTS_P COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
R21 24.3 1% 62.5mW CLK1_TRIG_SIGNAL_R_DN
P_BD1_CMTS_N COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1

TRIG LED

PWR LED

V_3P3AUX_1 R20 130 1% 62.5mW DS_BD1_PWR GRN APH1608-TD47 0603 GND_BD1

INPUT REFCLKS

P_BD1_CLK0_P BD1_REFCLK0_DP COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1
P_BD1_CLK0_N BD1_REFCLK0_DN COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1

P_BD1_CLK1_P BD1_REFCLK1_DP COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1
P_BD1_CLK1_N BD1_REFCLK1_DN COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1

P_BD1_CLK2_P BD1_REFCLK2_DP COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1
P_BD1_CLK2_N BD1_REFCLK2_DN COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1

P_BD1_CLK3_P BD1_REFCLK3_DP COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1
P_BD1_CLK3_N BD1_REFCLK3_DN COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD1

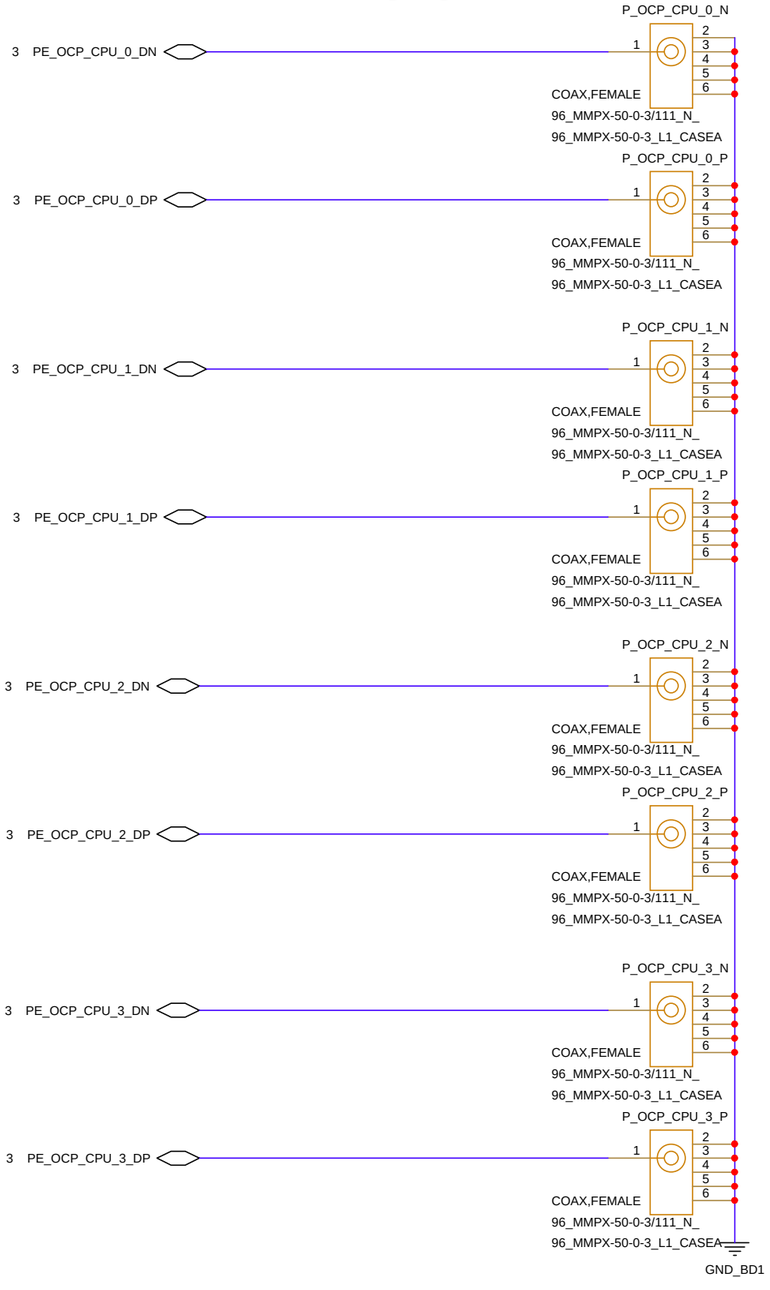
ROOM = BRD1

WARRANTY NOTE :
THIS CONTRIBUTION IS PROVIDED WITHOUT WARRANTY OF ANY KIND AND IS PROVIDED AS-IS, AND THE CONTRIBUTOR DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AS WELL AS ANY WARRANTIES EXPRESS, IMPLIED, OR STATUTORY.

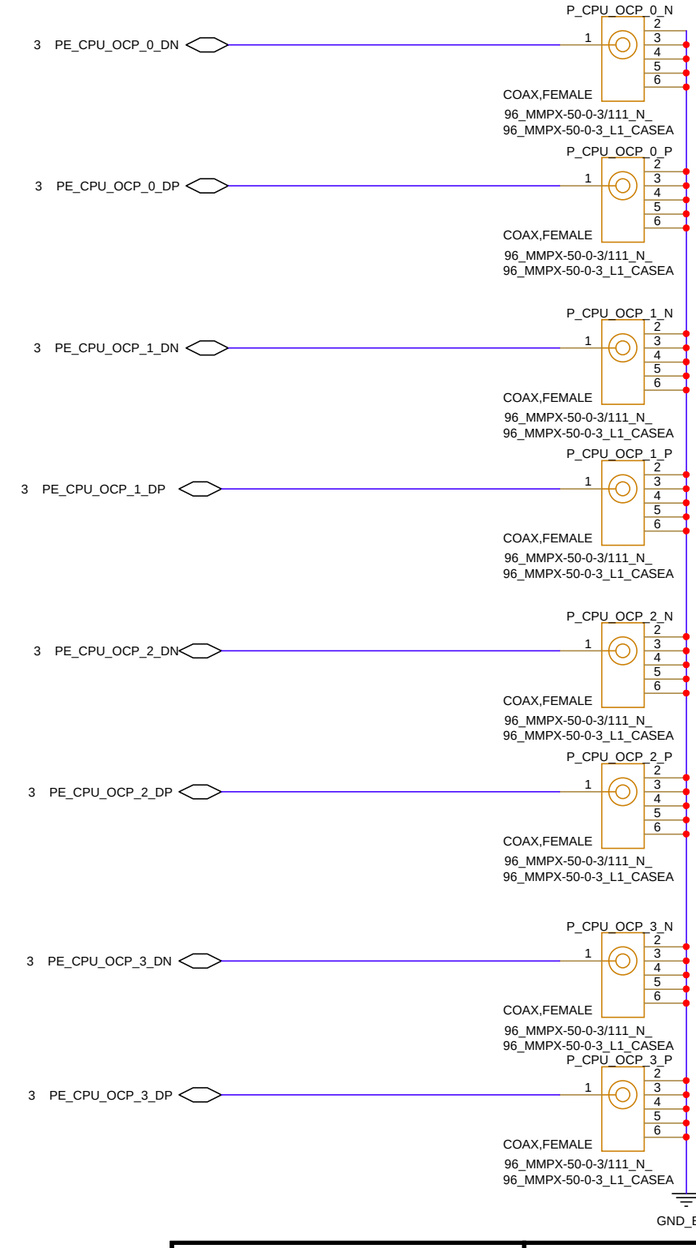
TITLE	OCP3 SI GEN 5 RX CLB
DWG NO.	C7D95
REV.	X02
DATE	Wednesday, June 28, 2023
SHEET	4 of 12

Board 1 - Rx/Tx Lanes 0-7 (cont)

CPU RX



CPU TX



ROOM = BRD1

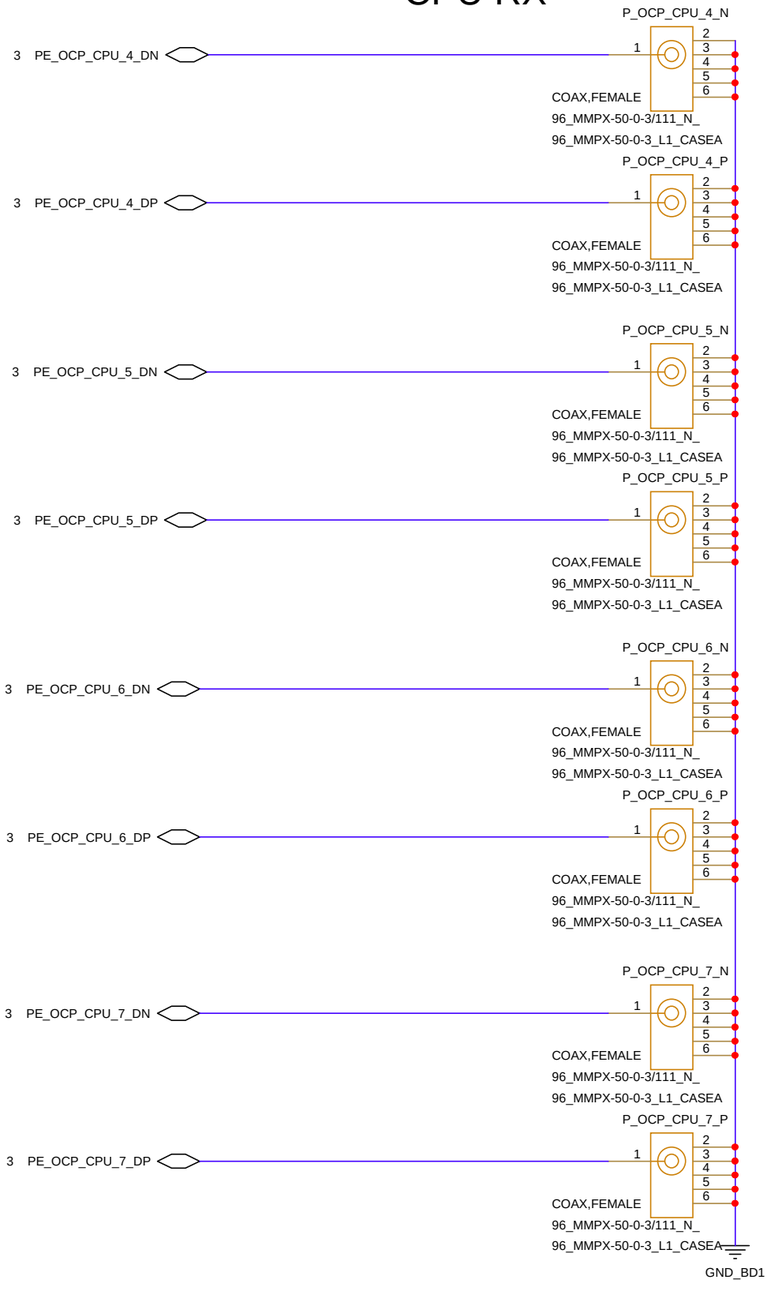
WARRANTY NOTE :

THIS CONTRIBUTION IS PROVIDED WITHOUT WARRANTY OF ANY KIND AND IS PROVIDED AS-IS, AND THE CONTRIBUTOR DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AS WELL AS ANY WARRANTIES EXPRESS, IMPLIED, OR STATUTORY.

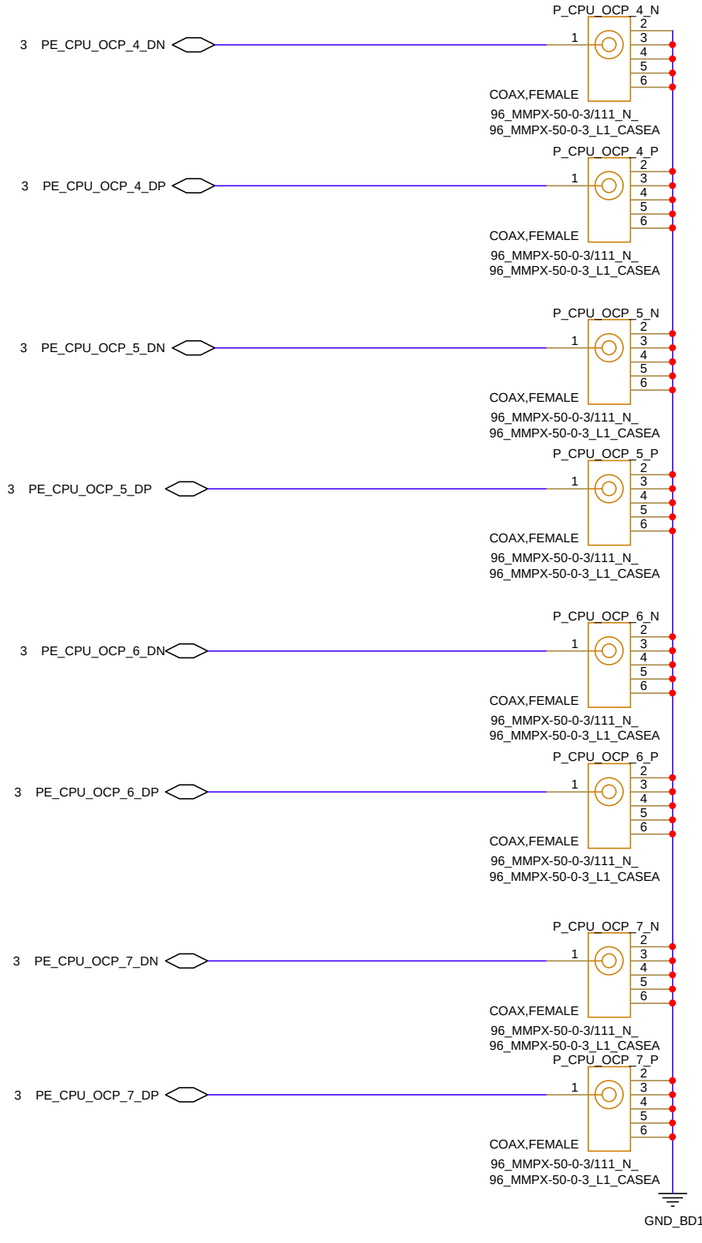
TITLE	OCP3 SI GEN 5 RX CLB		
DWG NO.	C7D95	REV.	X02
DATE	Wednesday, June 28, 2023	SHEET	5 of 12

Board 1 - Rx/Tx Lanes 0-7 (cont)

CPU RX



CPU TX



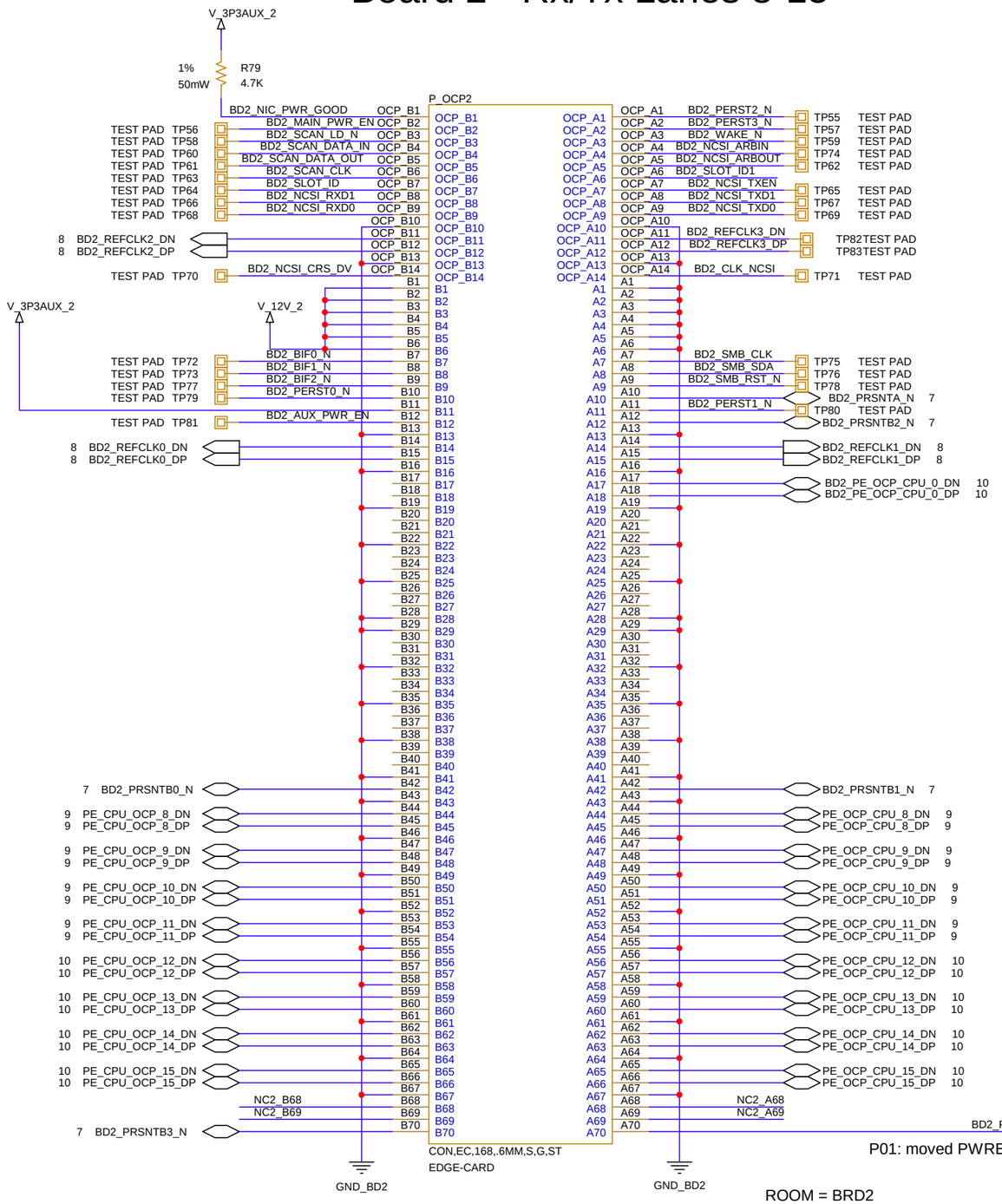
ROOM = BRD1

WARRANTY NOTE :

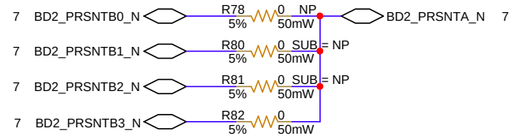
THIS CONTRIBUTION IS PROVIDED WITHOUT WARRANTY OF ANY KIND AND IS PROVIDED AS-IS, AND THE CONTRIBUTOR DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AS WELL AS ANY WARRANTIES EXPRESS, IMPLIED, OR STATUTORY.

TITLE	OCP3 SI GEN 5 RX CLB		
DWG NO.	C7D95	REV.	X02
DATE	Wednesday, June 28, 2023	SHEET	6 of 12

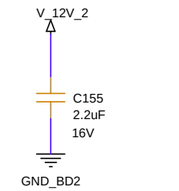
Board 2 - Rx/Tx Lanes 8-15

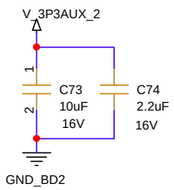


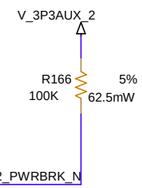
PRSNTB[3:0]_N = 1110 -> x8 link



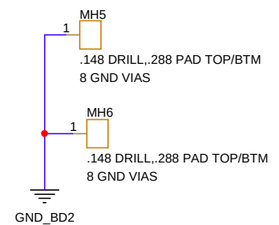
P01: pin A6 is now SLOT ID1







Faceplate Mtg Holes



TITLE	OCP3 SI GEN 5 RX CLB
DWG NO.	C7D95
REV.	X02
DATE	Wednesday, June 28, 2023
SHEET	7 of 12

Board 2 - Rx/Tx Lanes 8-15 (Cont.)

RSVD TEST

BD2_BTN_NC R84 5% 0 50mW BD2_BUS_SEL
SUB = NP
BD2_BTN_NO R85 5% 0 50mW BD2_555_TRI
SUB = NP

V_3P3AUX_2 R86 10K 1% 62.5mW BD2_BTN_NC
SW3 SPDT PUSHBUTTON BD2_BTN_NO GND_BD2

V_3P3AUX_2 R94 10K 1% 62.5mW

V_3P3AUX_2 C76 10V 0.1uF GND_BD2
U17 NC7SZ00 SC70 GND_BD2

V_3P3AUX_2 C82 10V 0.1uF GND_BD2
U22 NC7SZ00 SC70 GND_BD2

P8 2X1,VERT,HDR 2.54MM PITCH 78511-402HLF GND_BD2
R90 1K 1% 50mW

V_3P3AUX_2 C79 10V 0.1uF GND_BD2
U21 NC7SZ00 SC70 GND_BD2

C84 10uF 16V GND_BD2

V_3P3AUX_2 C77 10V 0.1uF GND_BD2
U19 NC7SZ00 SC70 GND_BD2

V_3P3AUX_2 C83 10V 0.1uF GND_BD2
U23 NC7SZ00 SC70 GND_BD2

V_3P3AUX_2 C78 10V 0.1uF GND_BD2
U18 NC7SZ00 SC70 GND_BD2

P7 2X1,VERT,HDR 2.54MM PITCH 78511-402HLF GND_BD2
R87 1K 1% 50mW

R91 5% 0 50mW BD2_555_TRI
BD2_555_OUT
BD2_555_RST_N

V_3P3AUX_2 R92 1% 1K 50mW
C81 10uF 16V GND_BD2
R95 5% 50mW 0

U20 LMC555 SO8
GND TRIGGER_N OUT RESET_N V+ DISCHARGE THRESHOLD CNTRL_VLT

V_3P3AUX_2 C75 10V 0.1uF GND_BD2
BD2_555_DISCHARGE

V_3P3AUX_2 R88 1K 1% 50mW
R89 10K 1% 62.5mW
C80 10uF 16V GND_BD2

R93 1% 1K 50mW BD2_555_OUT_JP
P9 2X1,VERT,HDR 2.54MM PITCH 78511-402HLF GND_BD2

V_3P3AUX_2 62.5mW R160 NP 10K 1%
P15 2X1,VERT,HDR 2.54MM PITCH 78511-402HLF GND_BD2
16V C165 1uF NP GND_BD2

BD2_BUS_SEL

U25 SY75603ATWL VQFN16
IN_p IN_n NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 GND EPAD
VDD OE0b OUT0_p OUT0_n OE1b OUT1_p OUT1_n

V_3P3AUX_2 C85 0.1uF 10V GND_BD2

CLK2_TRIG_SIGNAL_DP C86 10V 0.1uF CLK2_TRIG_SIGNAL_C_DP
R96 24.3 1% 62.5mW CLK2_TRIG_SIGNAL_R_DP
CLK2_TRIG_SIGNAL_DN C90 10V 0.1uF CLK2_TRIG_SIGNAL_C_DN

V_3P3AUX_2 R168 1% 10K 62.5mW

GND_BD2

V_3P3AUX_2 C87 6.3V 100uF C88 10uF 16V C89 2.2uF 16V GND_BD2

CMTS IN

P_BD2_TRIG_IN_P COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
CLK2_HOST_TO_TRIGGER_DP
C156 10V 0.056uF SUB = NP GND_BD2

P_BD2_TRIG_IN_N COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
CLK2_HOST_TO_TRIGGER_DN
C158 10V 0.056uF SUB = NP GND_BD2

V_3P3AUX_2 C167 10V 0.1uF GND_BD2
U27 NC7SZ14 SOT353 GND_BD2

TRIG LED

V_12V_2 R156 1% 1K 50mW DS_BD2_TRIG GRN APH1608-TD47 0603
C157 16V 10uF
Q3 2N7002K SOT23 GND_BD2

CMTS OUT

P_BD2_CMTS_P COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
R99 24.3 1% 62.5mW CLK2_TRIG_SIGNAL_R_DN
P_BD2_CMTS_N COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
GND_BD2

PWR LED

V_3P3AUX_2 R97 130 1% 62.5mW DS_BD2_PWR GRN APH1608-TD47 0603 GND_BD2

INPUT REFCLKS

7 BD2_REFCLK0_DP P_BD2_CLK0_P COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
7 BD2_REFCLK0_DN P_BD2_CLK0_N COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD2

7 BD2_REFCLK1_DP P_BD2_CLK1_P COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
7 BD2_REFCLK1_DN P_BD2_CLK1_N COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD2

7 BD2_REFCLK2_DP P_BD2_CLK2_P COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA
7 BD2_REFCLK2_DN P_BD2_CLK2_N COAX,FEMALE 96_MMPX-50-0-3/111_N_ 96_MMPX-50-0-3_L1_CASEA GND_BD2

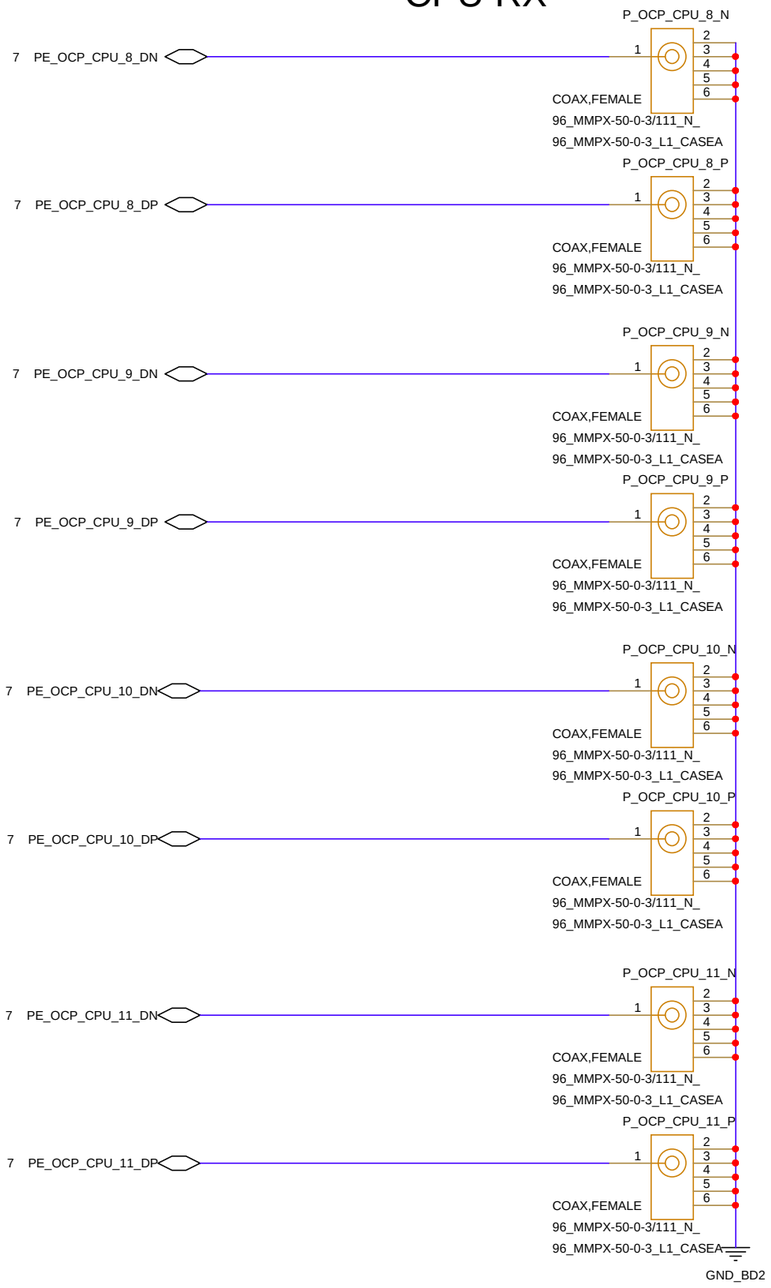
ROOM = BRD2

WARRANTY NOTE :
THIS CONTRIBUTION IS PROVIDED WITHOUT WARRANTY OF ANY KIND AND IS PROVIDED AS-IS, AND THE CONTRIBUTOR DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AS WELL AS ANY WARRANTIES EXPRESS, IMPLIED, OR STATUTORY.

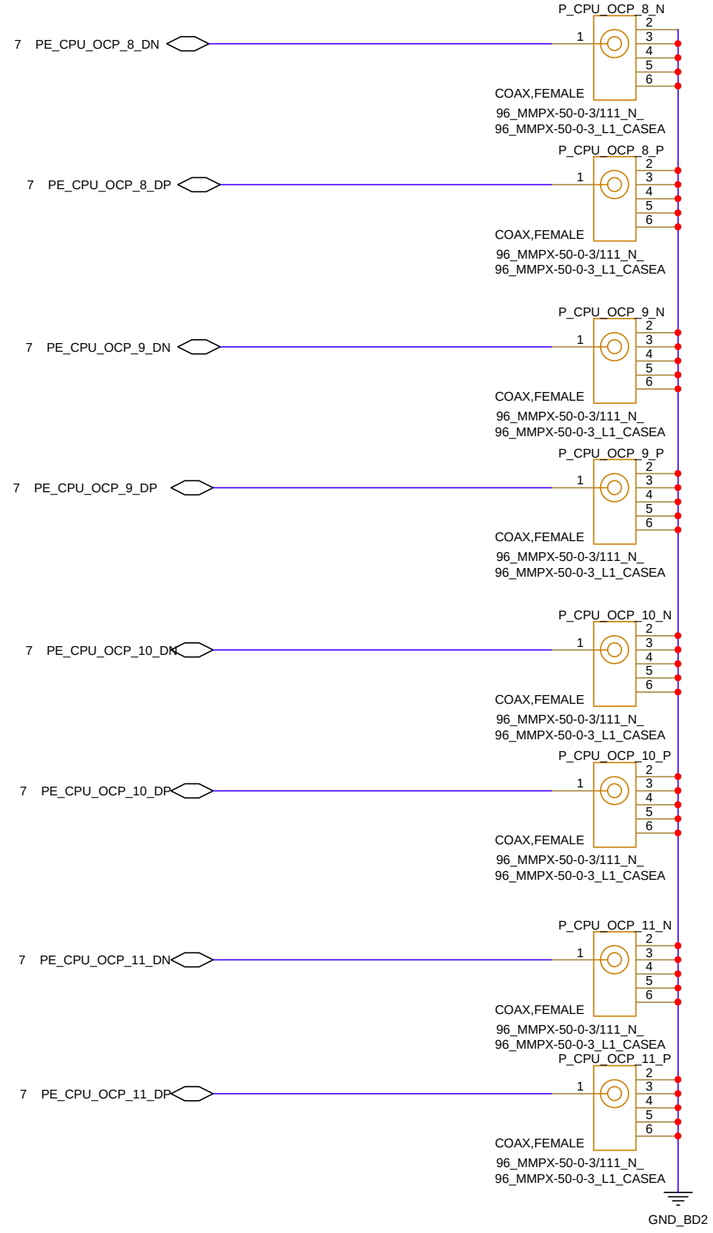
TITLE	OCP3 SI GEN 5 RX CLB
DWG NO.	C7D95
REV.	X02
DATE	Wednesday, June 28, 2023
SHEET	8 of 12

Board 2 - Rx/Tx Lanes 8-15 (Cont.)

CPU RX



CPU TX



ROOM = BRD2

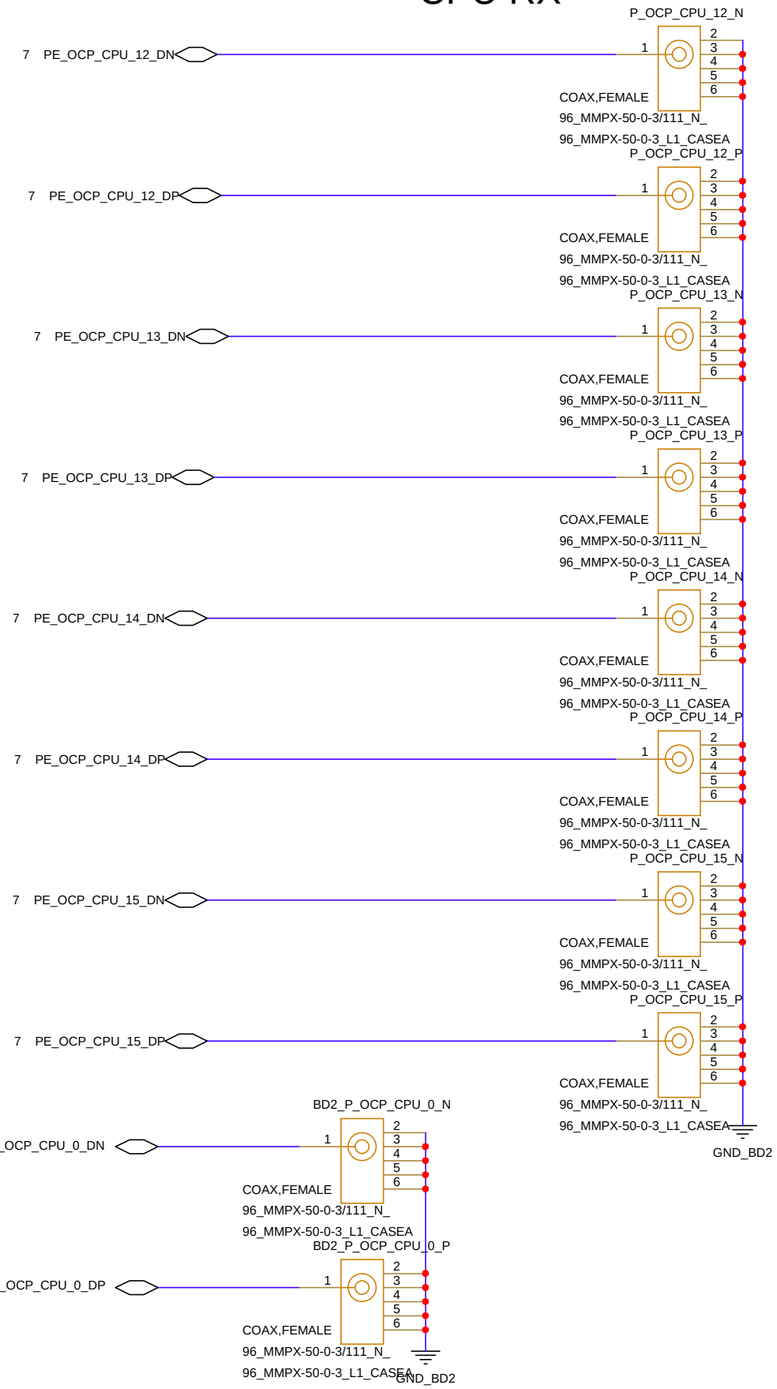
WARRANTY NOTE :

THIS CONTRIBUTION IS PROVIDED WITHOUT WARRANTY OF ANY KIND AND IS PROVIDED AS-IS, AND THE CONTRIBUTOR DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AS WELL AS ANY WARRANTIES EXPRESS, IMPLIED, OR STATUTORY.

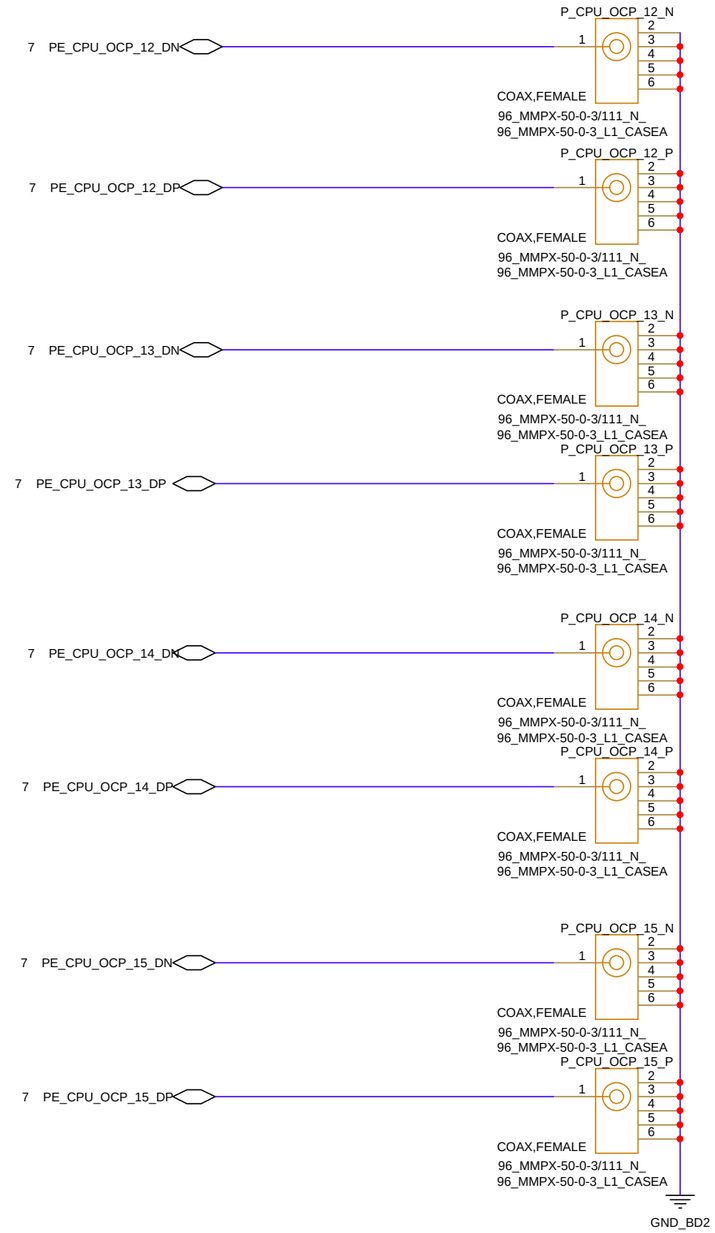
TITLE	OCP3 SI GEN 5 RX CLB		
DWG NO.	C7D95	REV.	X02
DATE	Wednesday, June 28, 2023	SHEET	9 of 12

Board 2 - Rx/Tx Lanes 8-15 (Cont.)

CPU RX



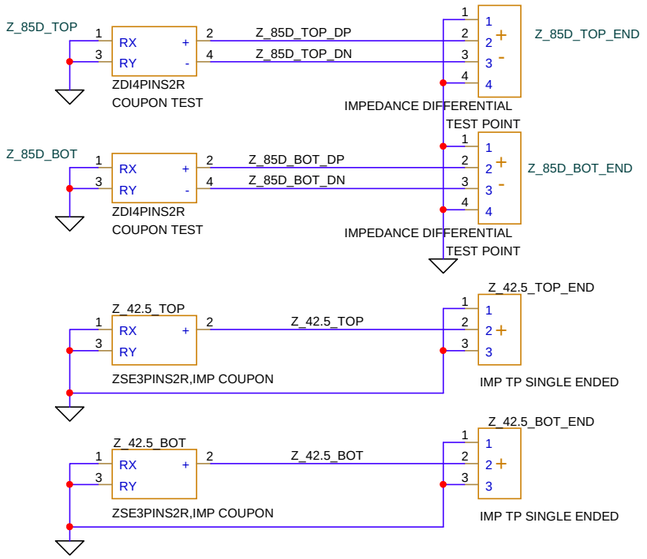
CPU TX

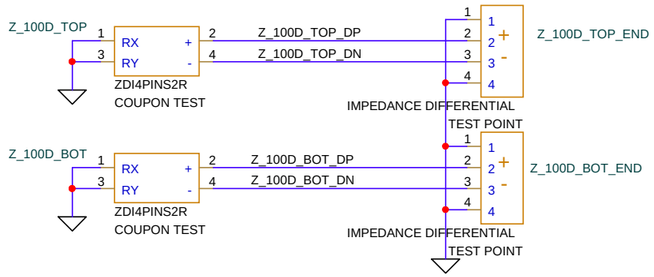


ROOM = BRD2

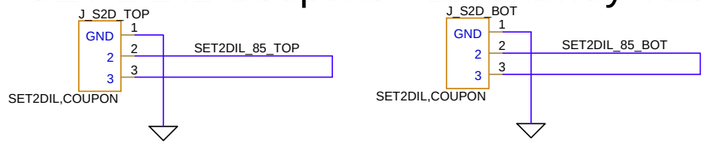
WARRANTY NOTE : THIS CONTRIBUTION IS PROVIDED WITHOUT WARRANTY OF ANY KIND AND IS PROVIDED AS-IS, AND THE CONTRIBUTOR DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AS WELL AS ANY WARRANTIES EXPRESS, IMPLIED, OR STATUTORY.	TITLE	OCP3 SI GEN 5 RX CLB	
	DWG NO.	C7D95	REV. X02
	DATE	Wednesday, June 28, 2023	SHEET 10 of 12

Impedance Coupons - Breakaway Tab 1
(6 inches)

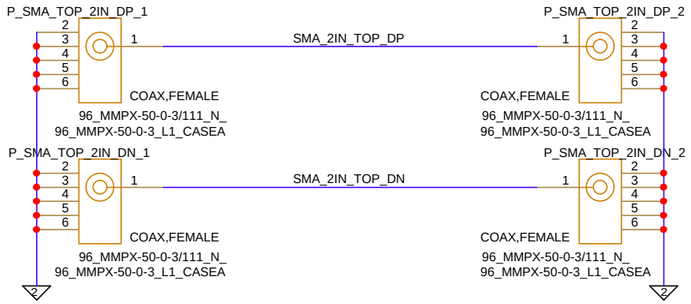


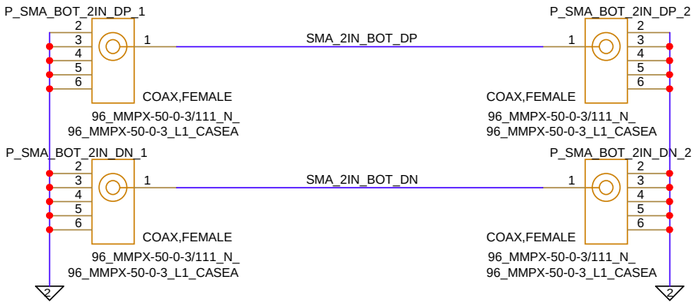


SET 2 DIL Coupons - Breakaway Tab 1



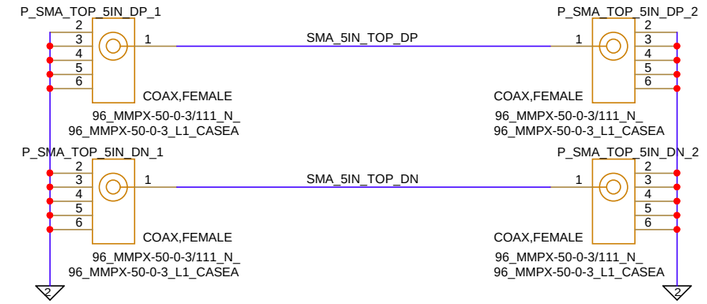
SMAs (2 in) - Breakaway Tab 2

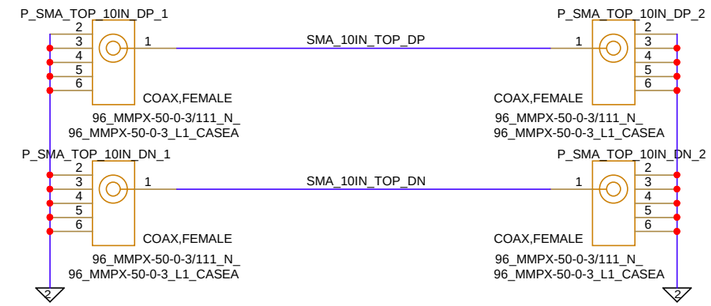


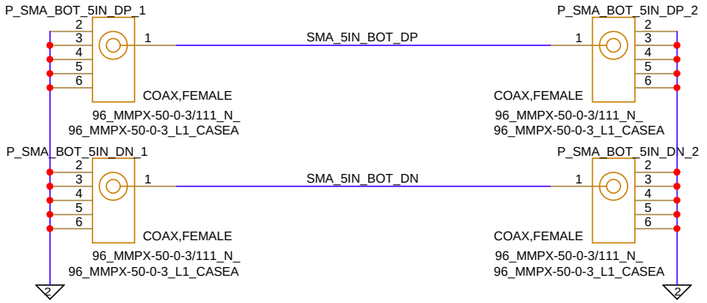


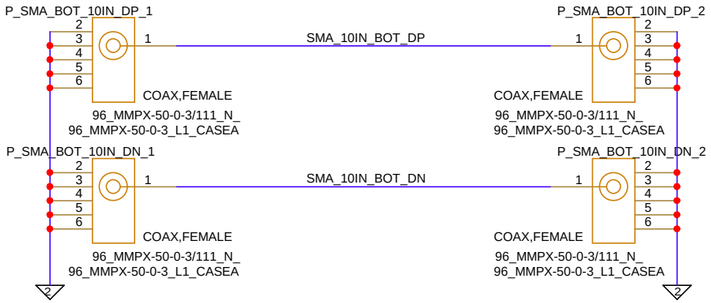
2D BARCODE
TYPE T
LBL4

SMAs (5 in and 10 in) - Breakaway Tab 2







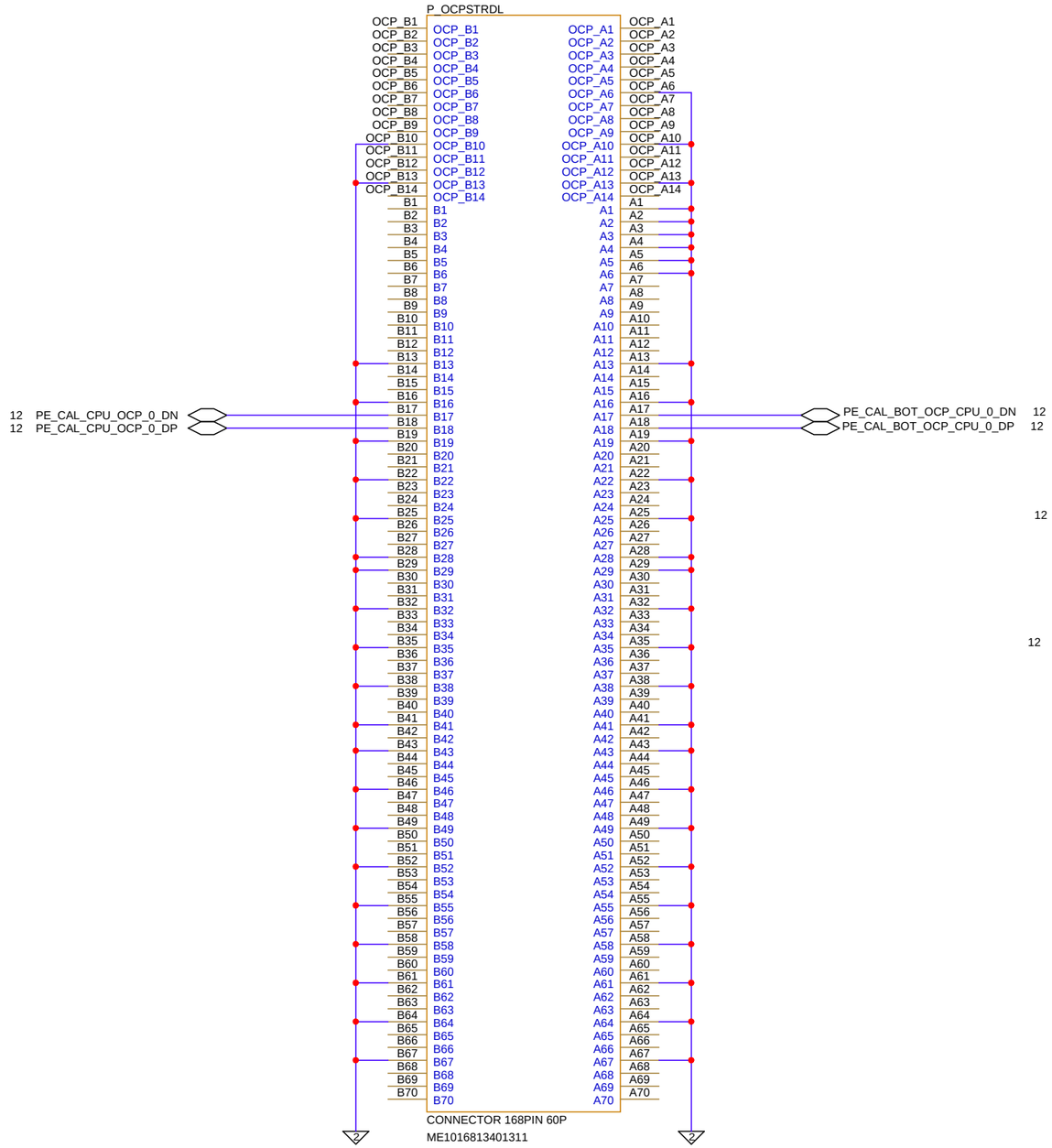


WARRANTY NOTE :

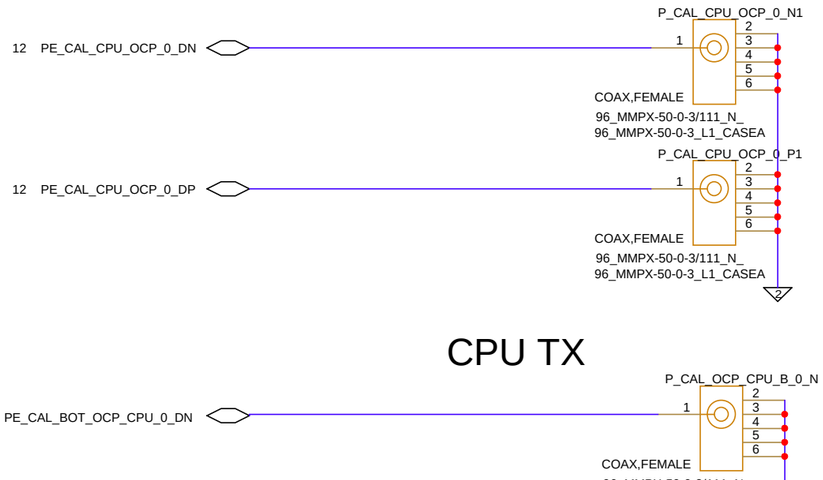
THIS CONTRIBUTION IS PROVIDED WITHOUT WARRANTY OF ANY KIND AND IS PROVIDED AS-IS, AND THE CONTRIBUTOR DISCLAIMS ALL WARRANTIES, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AS WELL AS ANY WARRANTIES EXPRESS, IMPLIED, OR STATUTORY.

TITLE	OCP3 SI GEN 5 RX CLB	
DWG NO.	C7D95	REV. X02
DATE	Wednesday, June 28, 2023	SHEET 11 of 12

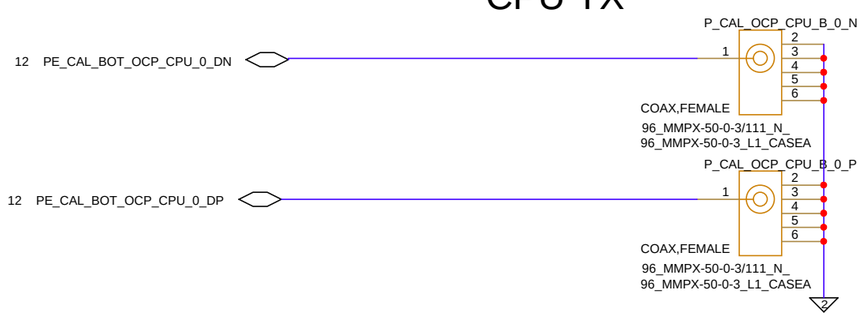
CLB CALIBRATION BOARD - Breakaway Tab 2



CPU RX



CPU TX



ROOM = CAL

TITLE	OCP3 SI GEN 5 RX CLB
DWG NO.	C7D95
REV.	X02
DATE	Wednesday, June 28, 2023
SHEET	12 of 12