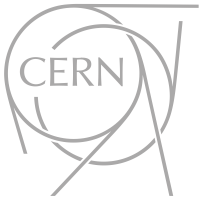
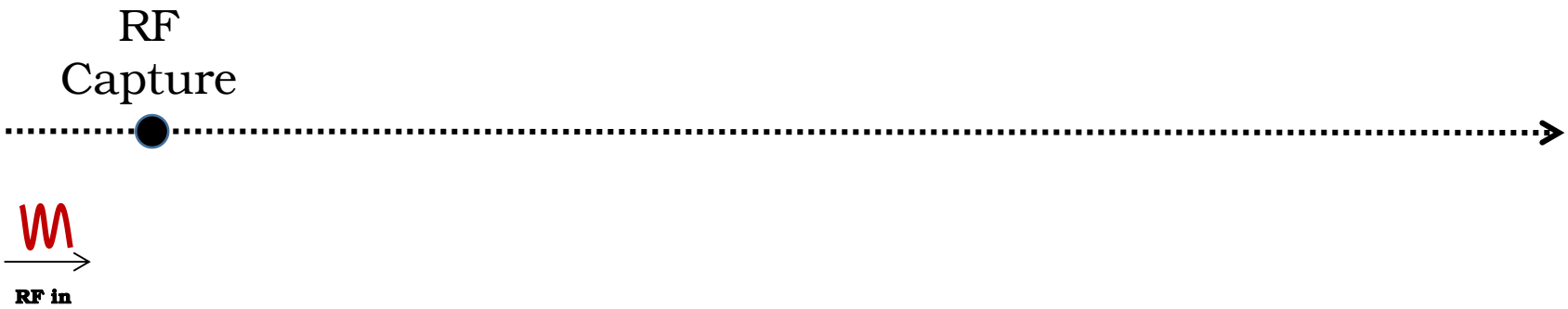
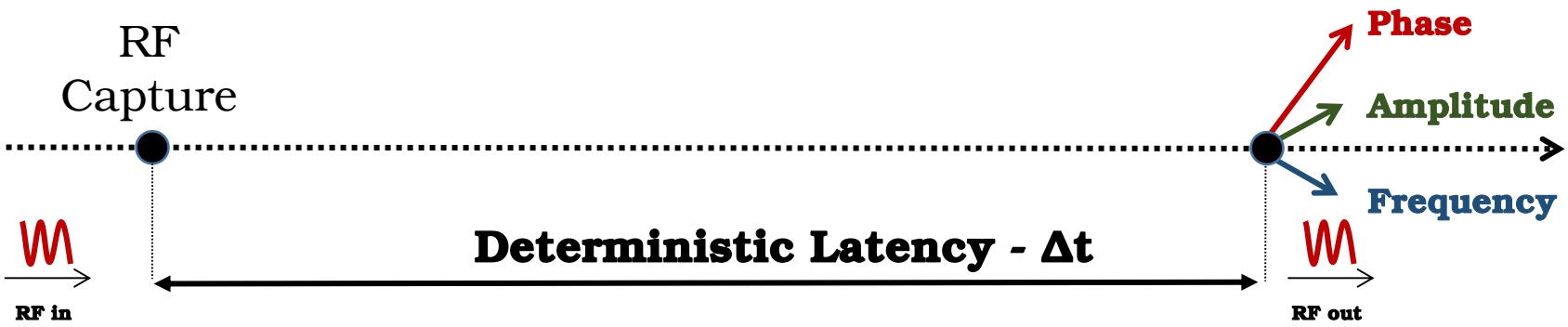
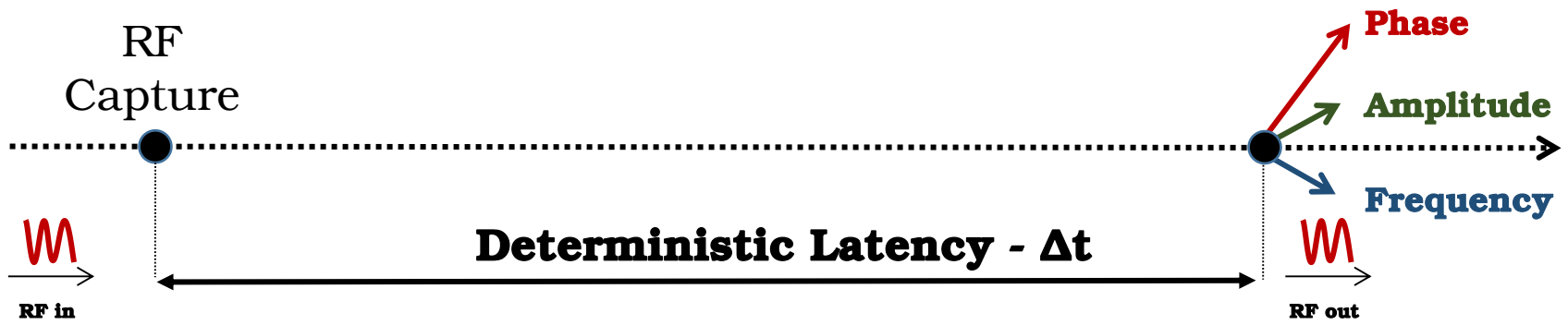
RF over Ethernet

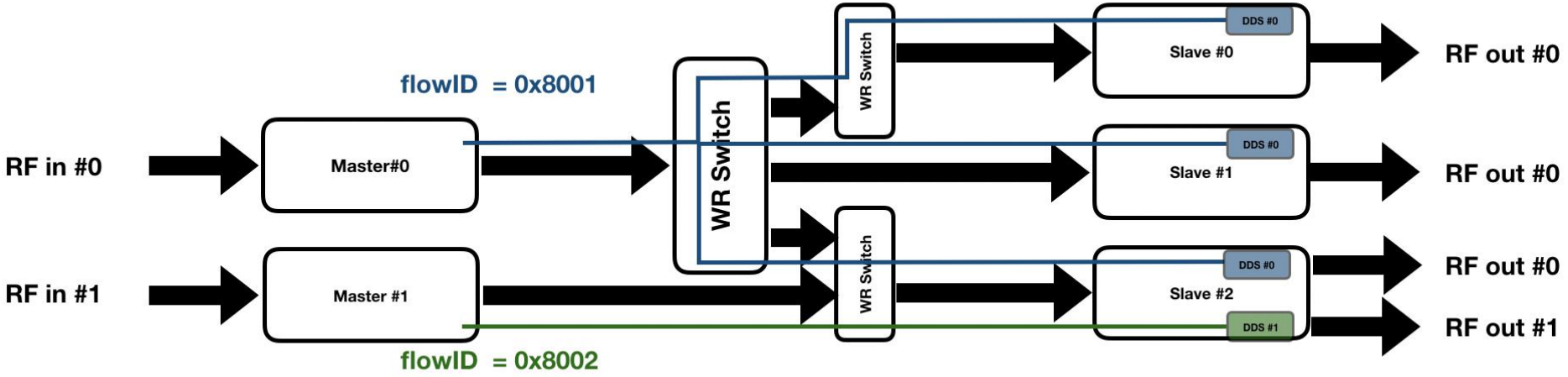


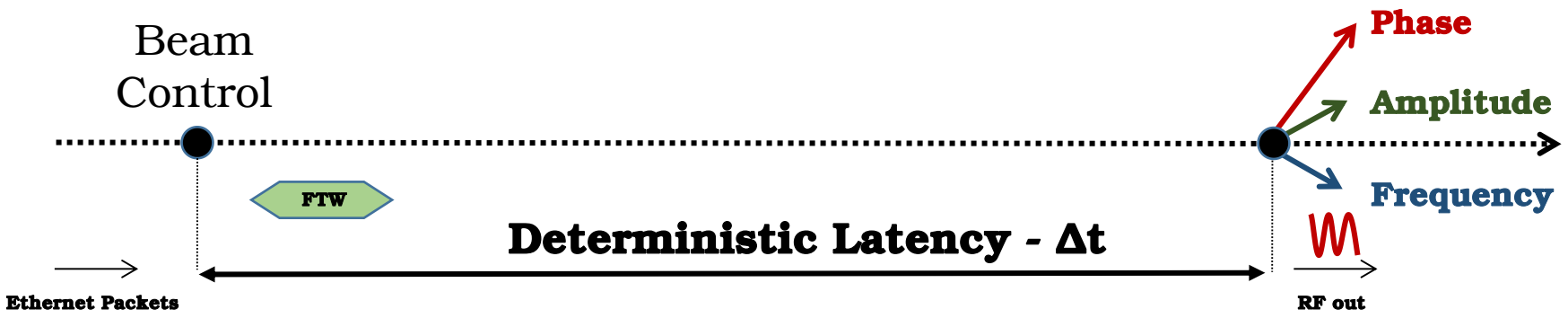
- **Overview + background**
- **SPS LLRF Protocol**
- **RoE IEEE1914.3 protocol**
- **Summary**

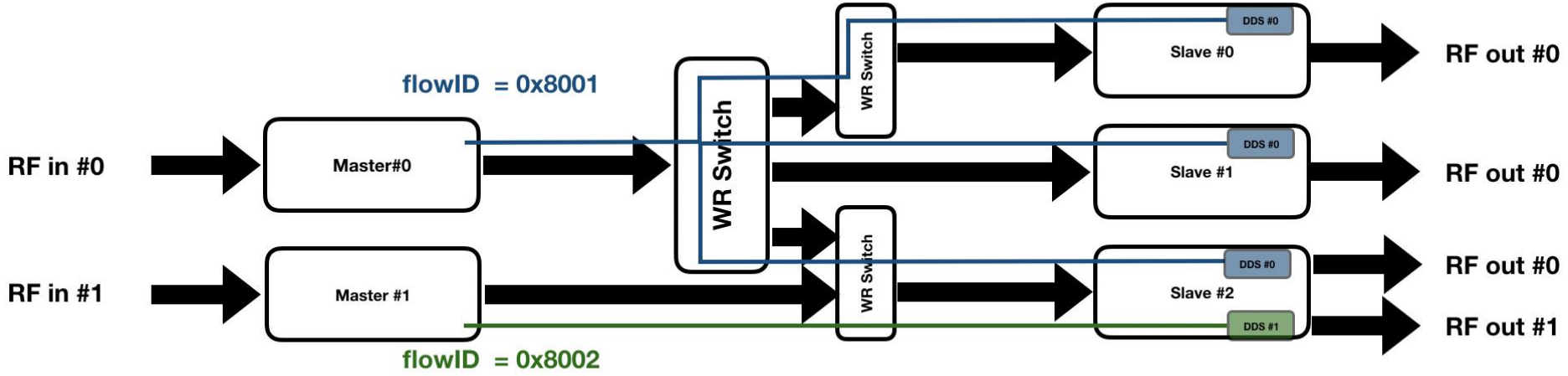

RF
Capture
RF in

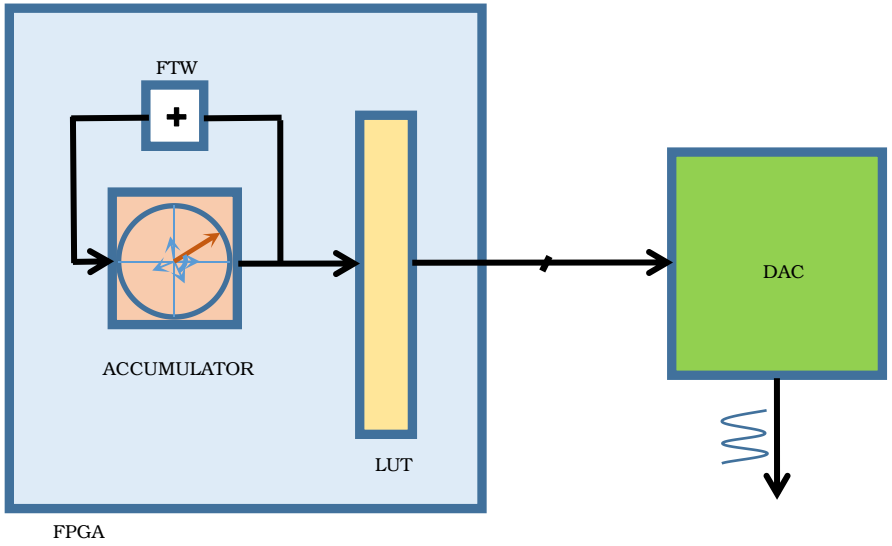

RF
Capture
Phase
Amplitude
Frequency
Deterministic Latency - Δt
RF in
RF out

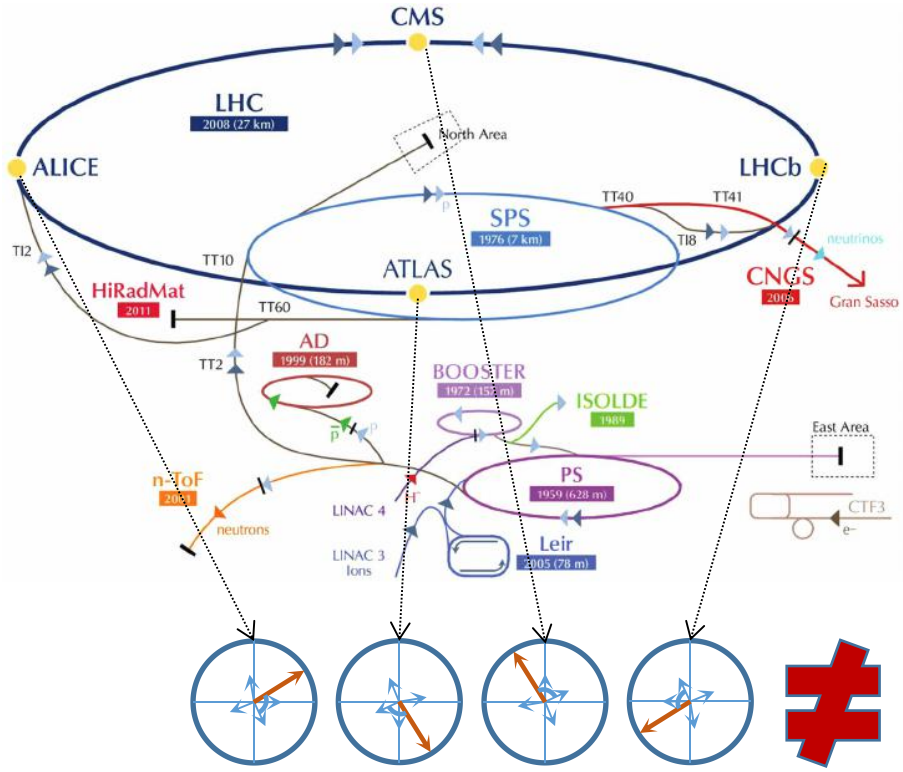

RF
Capture
Phase
Amplitude
Frequency
Deterministic Latency - Δt
RF in
RF out


RF in #0
RF in #1
Master#0
Master #1
flowID = 0x8001
flowID = 0x8002
WR Switch
WR Switch
WR Switch
DDS #0
Slave #0
DDS #0
Slave #1
DDS #0
DDS #1
Slave #2
RF out #0
RF out #0
RF out #0
RF out #1


Beam
Control
Phase
Amplitude
Frequency
FTW
Deterministic Latency - Δt
Ethernet Packets
RF out


RF in #0
RF in #1
Master#0
Master #1
flowID = 0x8001
flowID = 0x8002
WR Switch
WR Switch
WR Switch
Slave #0
Slave #1
Slave #2
DDS #0
DDS #0
DDS #0
DDS #1
RF out #0
RF out #0
RF out #0
RF out #1

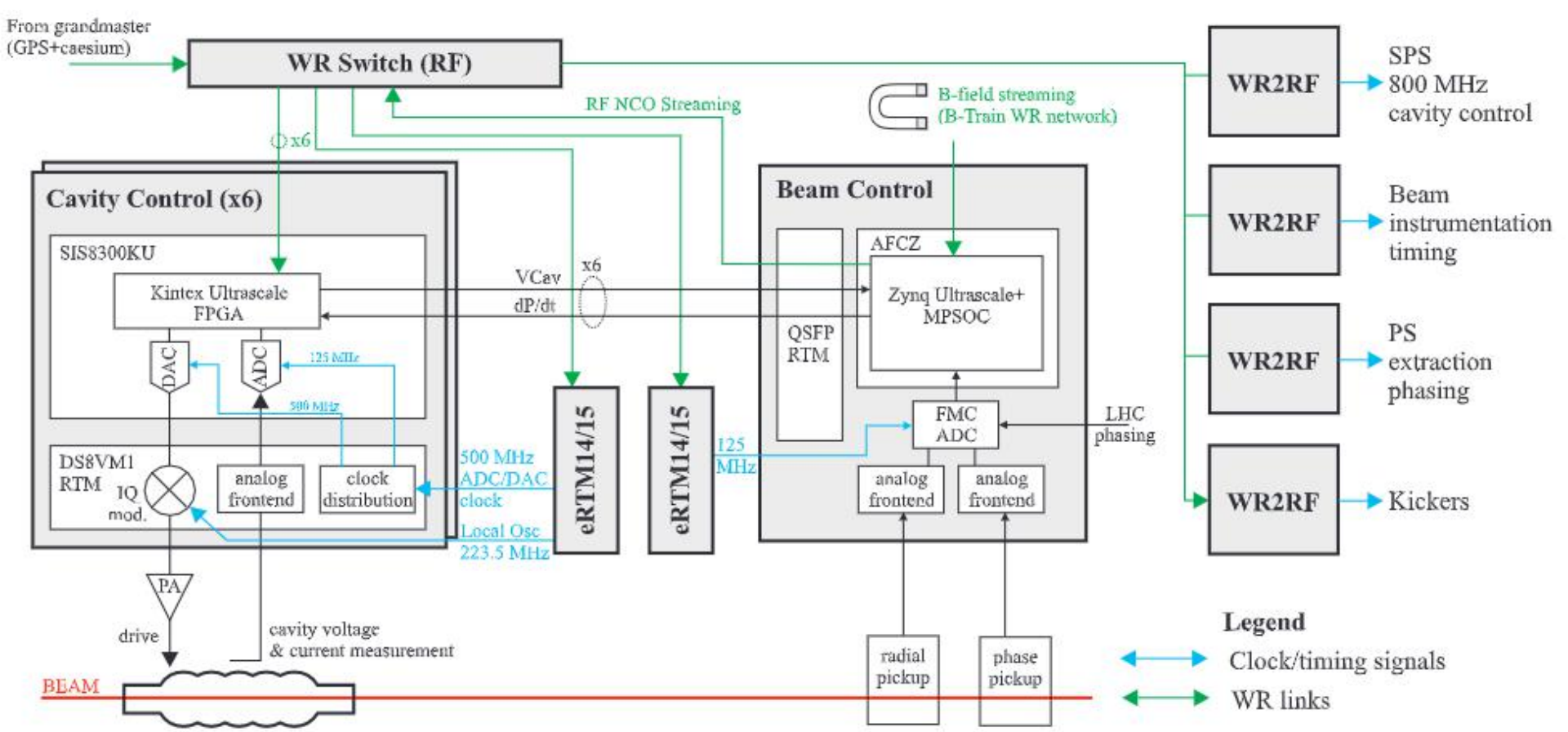




If each slave replays FTWs when using free running local oscillators/PLLs, their Numerically Controlled Oscillators (NCO) cannot be guaranteed to be aligned.

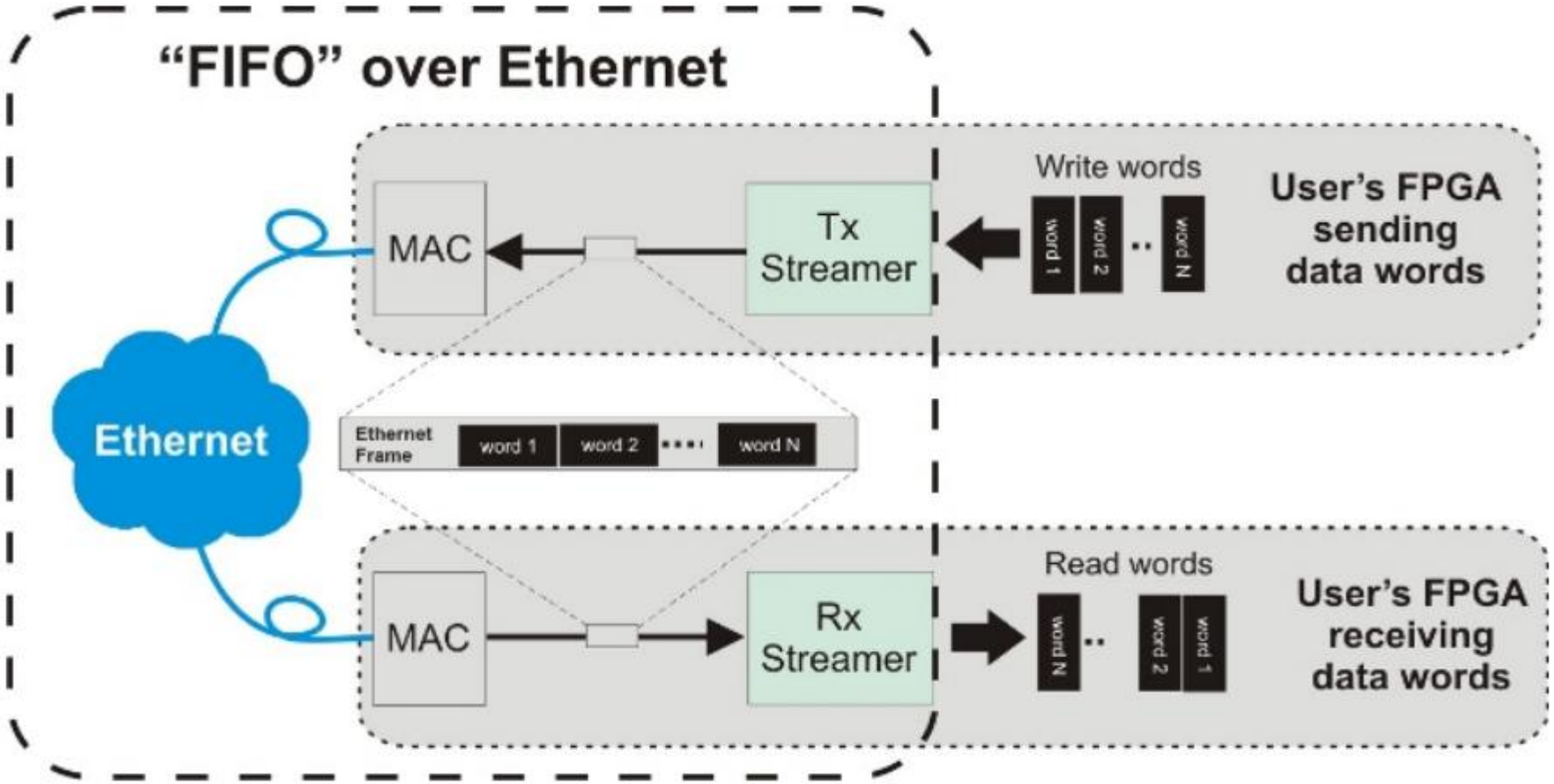
NCOs without WR timing

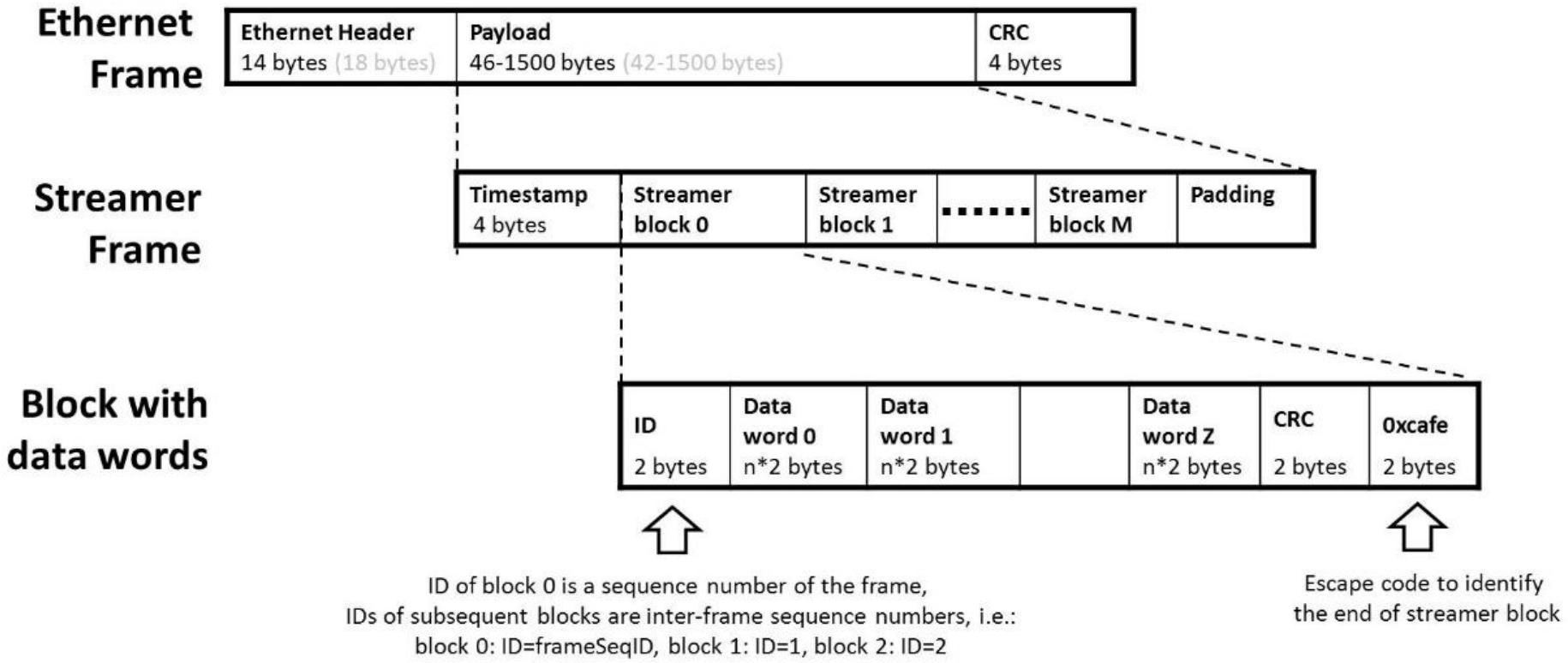
NCOs with WR timing



Each cavity controller and WR2RF card "plays" the same FTW at the same time.

A packet is sent once per turn from beam control and contains the frequency setpoint for the next turn. This sequence of packets forms an RFtrain.


"FIFO" over Ethernet
Write words
User's FPGA sending data words
MAC
Tx Streamer
word 1
word 2
word N
Ethernet
Ethernet Frame
word 1
word 2
word N
MAC
Rx Streamer
Read words
User's FPGA receiving data words
word N
word 2
word 1



The TX side of WR Streamers takes the application data (streamer block) and adds a TX timestamp.

On receipt, the RX logic "holds" the packet in its fifo until the local time has reached TXtimestamp + RXlatency. RXlatency is determined locally and for SPS LLRF is 16us.

RoE structure-aware direct digital synthesis mapping using an OUI subType

Specification

Version 1.4

2020-01-17

Revision History Table

Version		
0.1	2019-08	Preliminary discussion and draft with ComCores
1.0	2019-11-20	First complete version by John Gill
1.1	2019-11-24	Review by Maciej Lipinski
1.2	2019-11-26	Maciej Lipinski updated Table 1 – subType mapping
1.3	2019-12-09	John Gill: added subclause 1.2 Background and clause 5. Example frame and review
1.4	2020-01-16	John Gill and Maciej Lipinski: feedback and joint review

http://roe-mapping.web.cern.ch/documents/RoE-DDS-mapping-v1.4.pdf

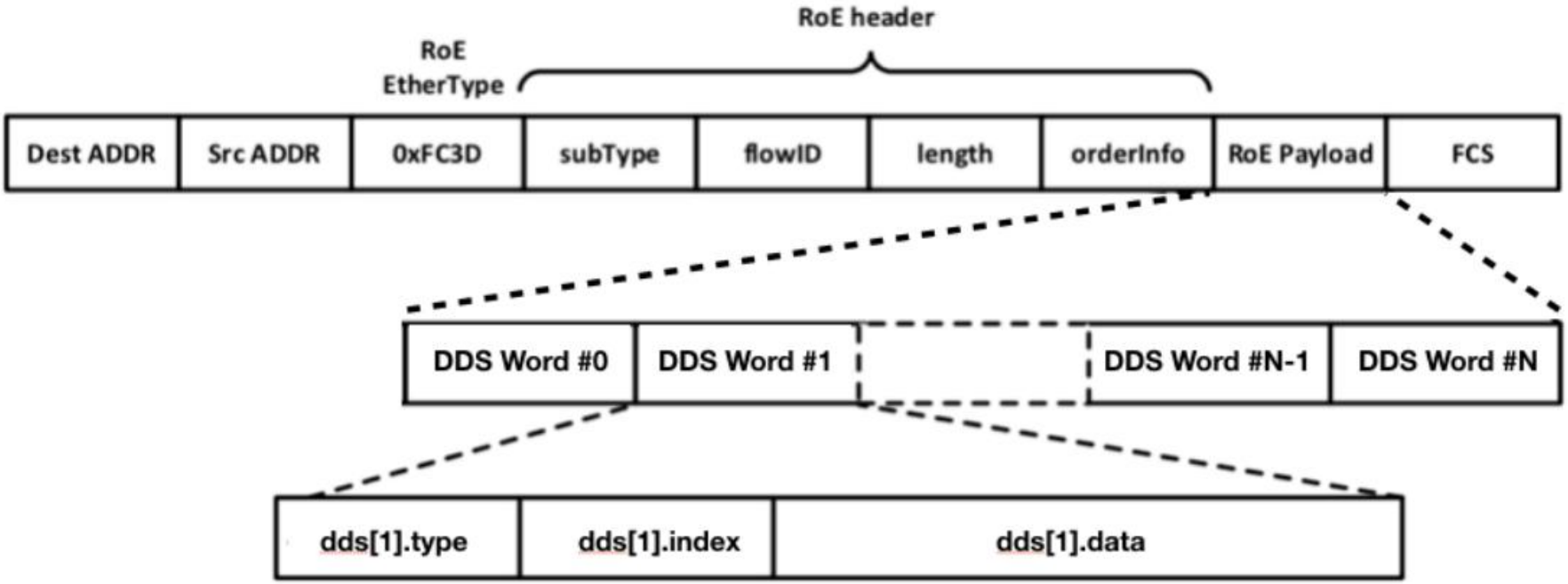


Figure 1 — RoE structure-aware DDS mapping encapsulation

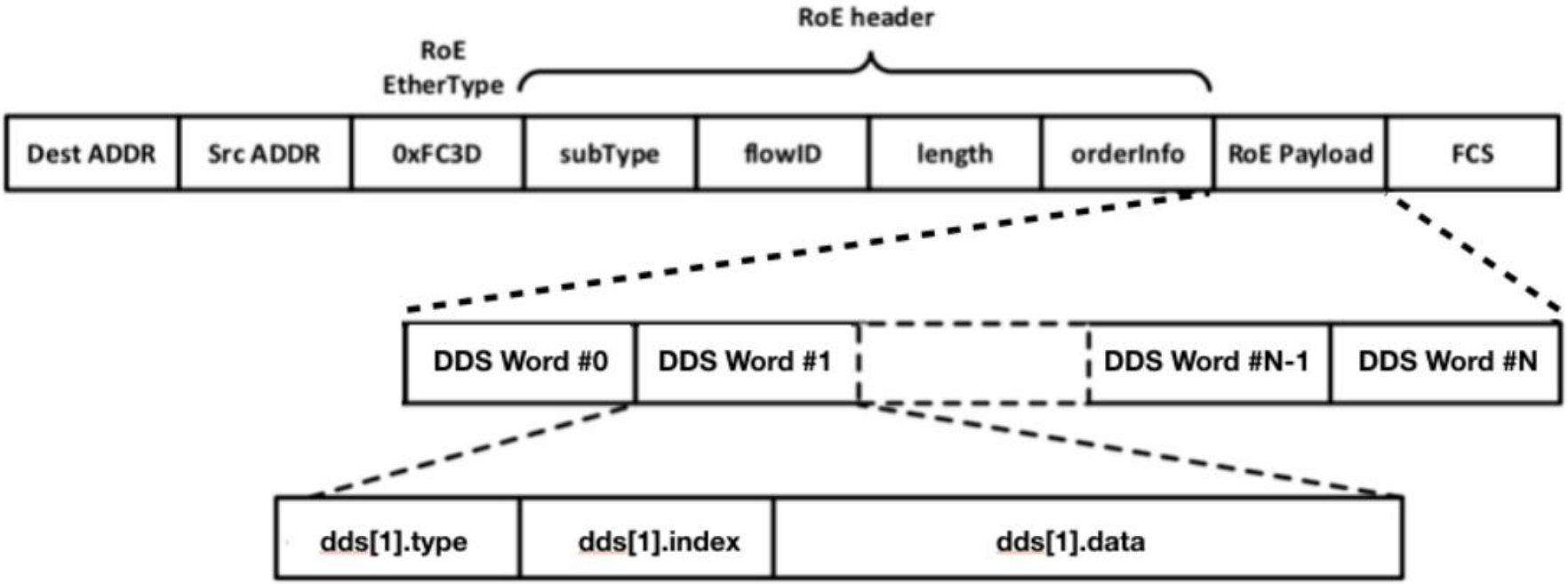


Figure 1 — RoE structure-aware DDS mapping encapsulation

DDS word name	Value of dds.type	DDS words properties				DDS word category
		Contains dds.index	Form of dds.data	DDS word size in bits (.ddsLengthW)	Requires presentation time	
Padding	**0**	No	N/A	4	No	Padding
TAI time	**1**	No	**.tai**	4 + 96	No	Time
RF time	**2**	No	**.rftime**	4 + 64	No	Time
Phase	**3**	Yes	**.phase**	4 + 4 + 64	Yes	Configuration
Operating Frequency	**4**	Yes	**.opFreq**	4 + 4 + 112	Yes	Configuration
FTW	**5**	Yes	**.ftw**	4 + 4 + 64	Yes	Control
Maximum Voltage	**6**	Yes	**.maxVolt**	4 + 4 + 16	Yes	Control
Event without Data	**7**	Yes	**.event**	4 + 4 + 40	Yes	Control
Event with Data	**8**	Yes	**.eventD**	4 + 4 + 104	Yes	Control
Control and Status Flags	**9**	Yes	**.csFlags**	4 + 4 + 32	Yes	Control
Reserved	**10-14**	Yes	Not specified	4 + 4 + 4 + 4 x (**dds.data.lengthD** + 1)	Not specified	Special
Extended	**15**	Yes	Not specified	4 + 4 + (4 x **N**) + 8 + 4 x (**dds.data.lengthD** + 1)	Not specified	Special

Table 2 — RoE structure-aware DDS words

WR Streamers

https://ohwr.org/project/wr-cores/wikis/WR-Streamers

RoE IEEE 1914.3 DDS protocol

http://roe-mapping.web.cern.ch/documents/RoE-DDS-mapping-v1.4.pdf