Digitized Clocking Technology

Achieving time synchronization inside a system and across distributed systems

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AHEAD OF WHAT'S POSSIBLE™

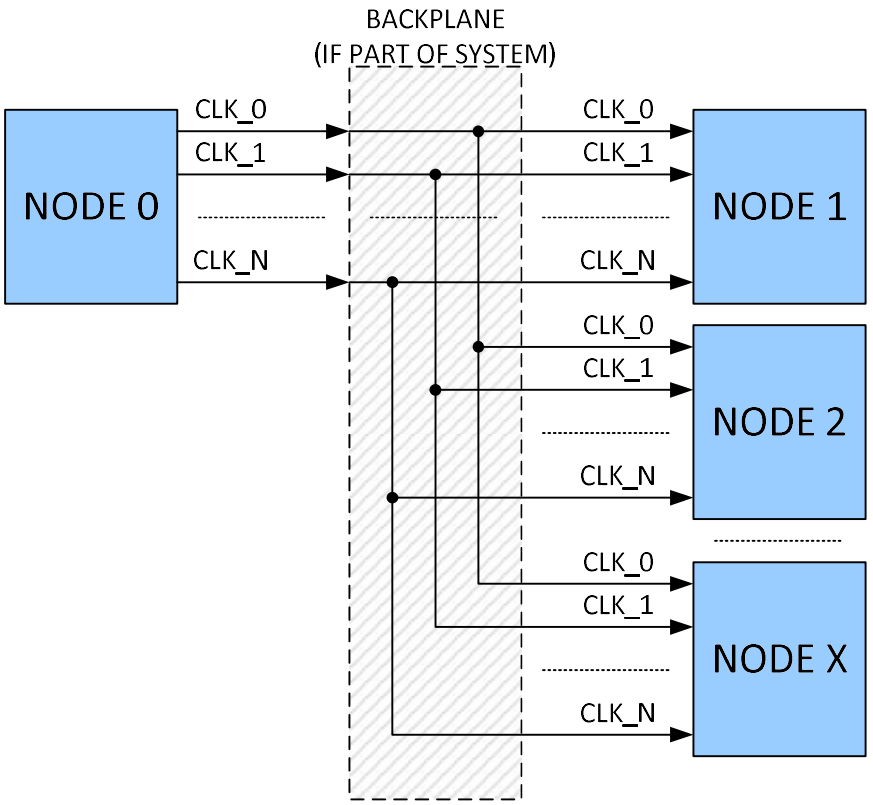
Topics

- Digitized Clocking technology concept
- Applying Digitized Clocking to distributed systems
- AD9546 Digitized Clocking Evaluation System

What is Digitized Clocking

- We talk of Digitized Clocking as a technology that transports clocks digitally on a serial bus (like Ethernet, but any Operation & Maintenance bus is fine)
- But Digitized Clocking can be seen as a technology to achieve clock domain synchronization
  - Within a system composed of multiple cards
  - Or
  - Between GPS equipped distributed systems
  - Or
  - Between distributed systems connected using optical fiber
- We achieved 100 ps synchronization on the AD9546 Digitized Clocking Evaluation System

Analog Clock Transport within a system

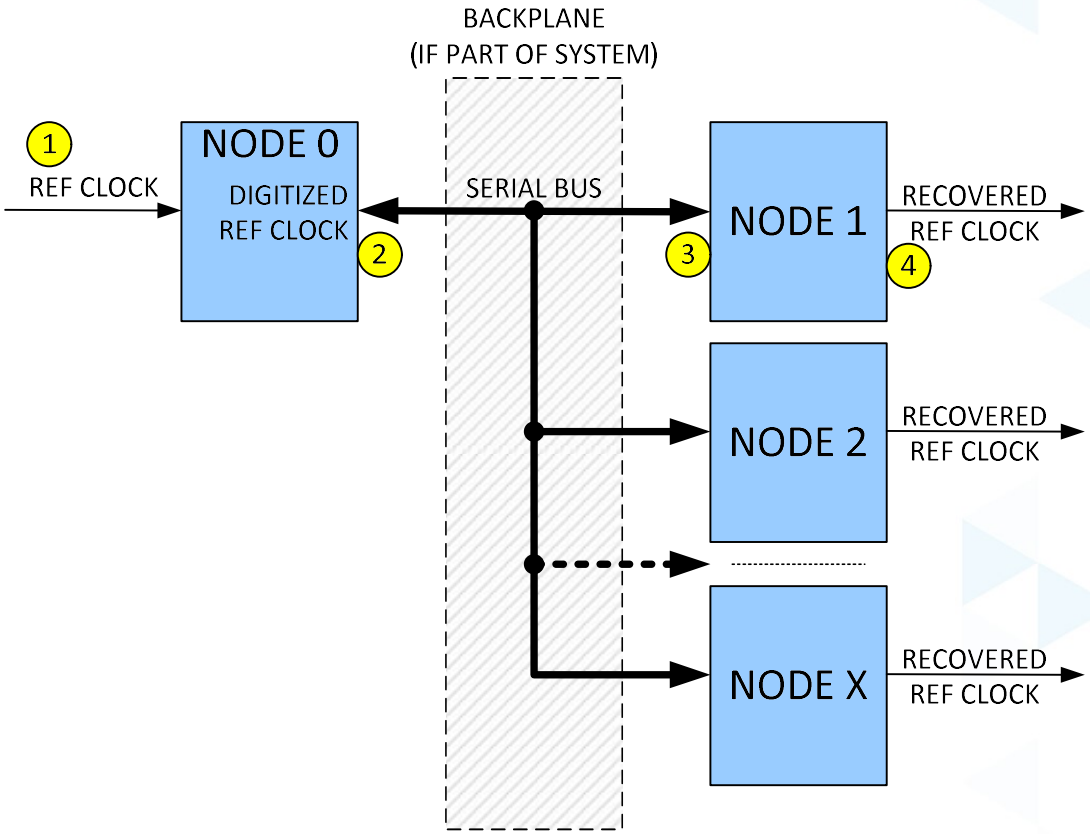


- CLK_0, CLK_1, …, CLK_N are transported from NODE 0 to NODE 1, NODE 2, …, NODE X
- Problems:
  - Each clock incurs propagation delays that need to be measured and compensated in real time
    - Round Trip Connections have to be created → very complicated design → design time increases
  - Cross coupling occurs between clocks → very difficult to eliminate → design time increases
  - If clocks go through a backplane, the backplane needs to be redesigned each time a new clock must be transported

- **Digitized Clocking Technology overcomes these problems**

Digitized Clocking Concept

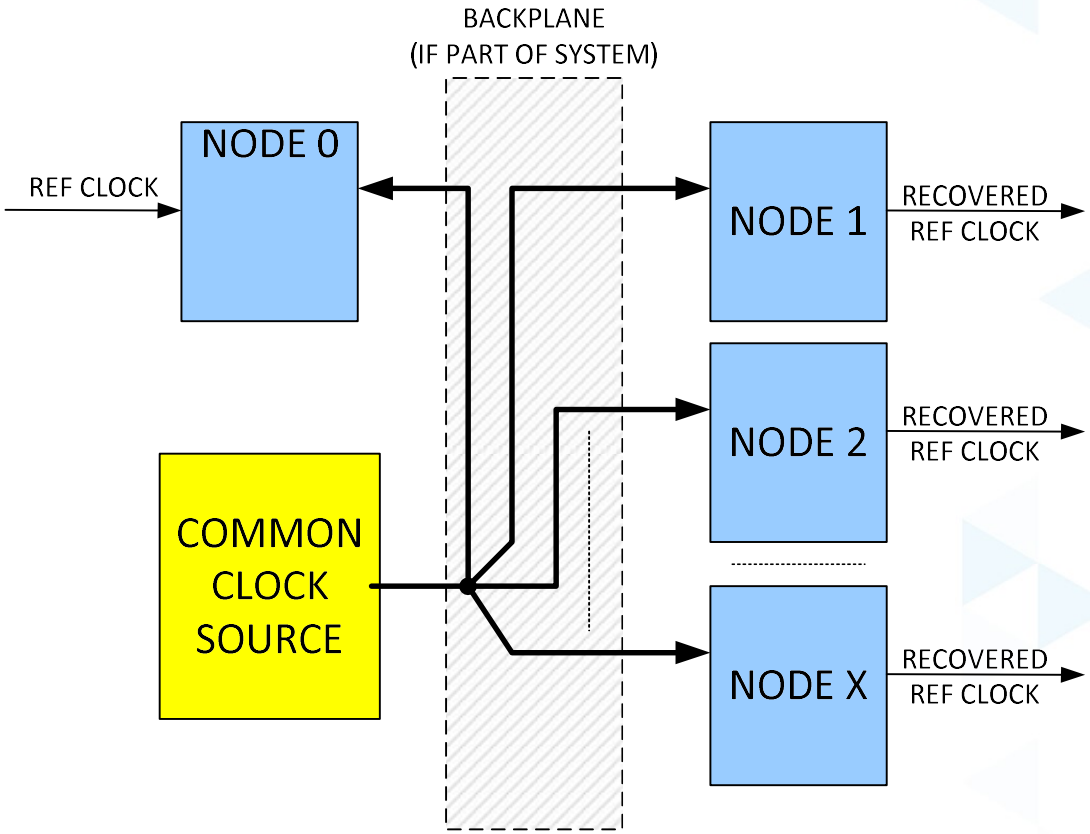
Assume all nodes share the same time base



- ① NODE 0 receives REF CLOCK
- ② NODE 0 time stamps REF CLOCK
  - i.e. NODE 0 digitizes REF CLOCK
  - NODE 0 creates time codes (i.e. REF CLOCK time stamps referenced to the shared time base)
  - NODE 0 sends time codes to the other nodes using the serial bus
- ③ Any NODE 1,…,X receives time codes through serial bus
- ④ That NODE 1,…,X generates a clock with the same frequency and phase as REF CLOCK
  - i.e. NODE 1,…,X recovers REF CLOCK
- Any control/communications bus in the system can be used

- **Absolute key point: All nodes share the same time base**

How a Shared Time Base is Realized

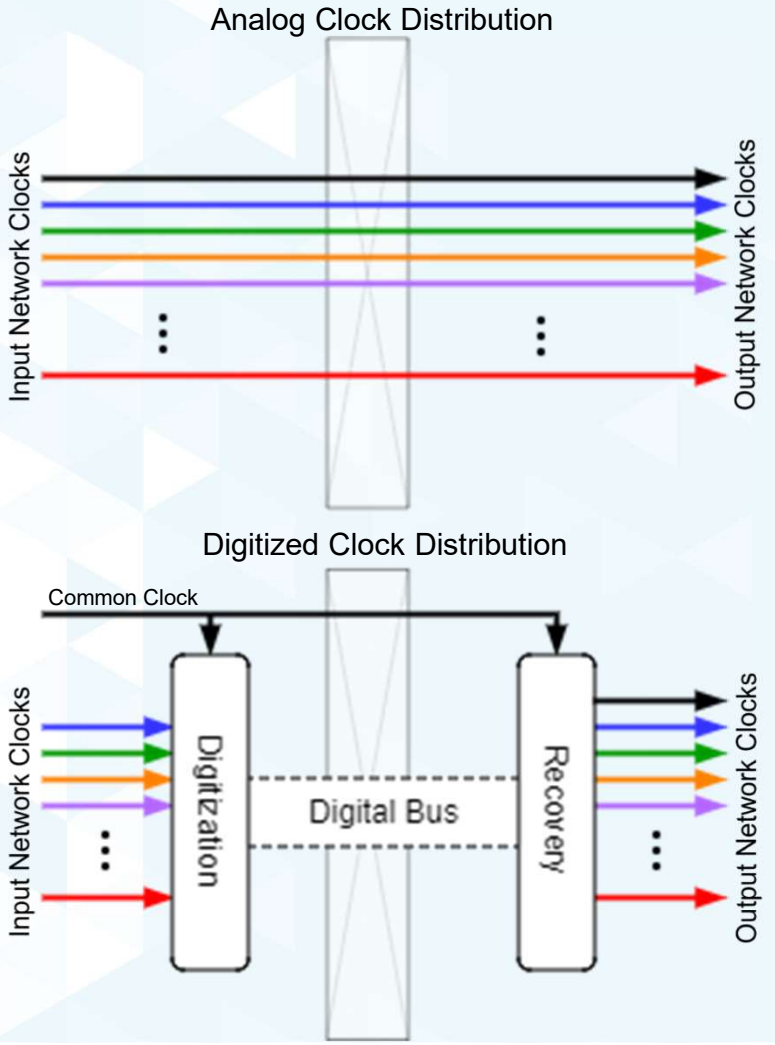


- Clock source sends the same analog clock to all nodes
  - It is called common clock
  - Any node can be a common clock source
- Propagation delays must be compensated
  - Ensures all nodes have the same time base
  - We use round trip delay measurements approach
    - It means creating loop backs for common clock connections
- User sends a sync signal to all nodes to create the common time base epoch

- **This is how Digitized Clocking works!**

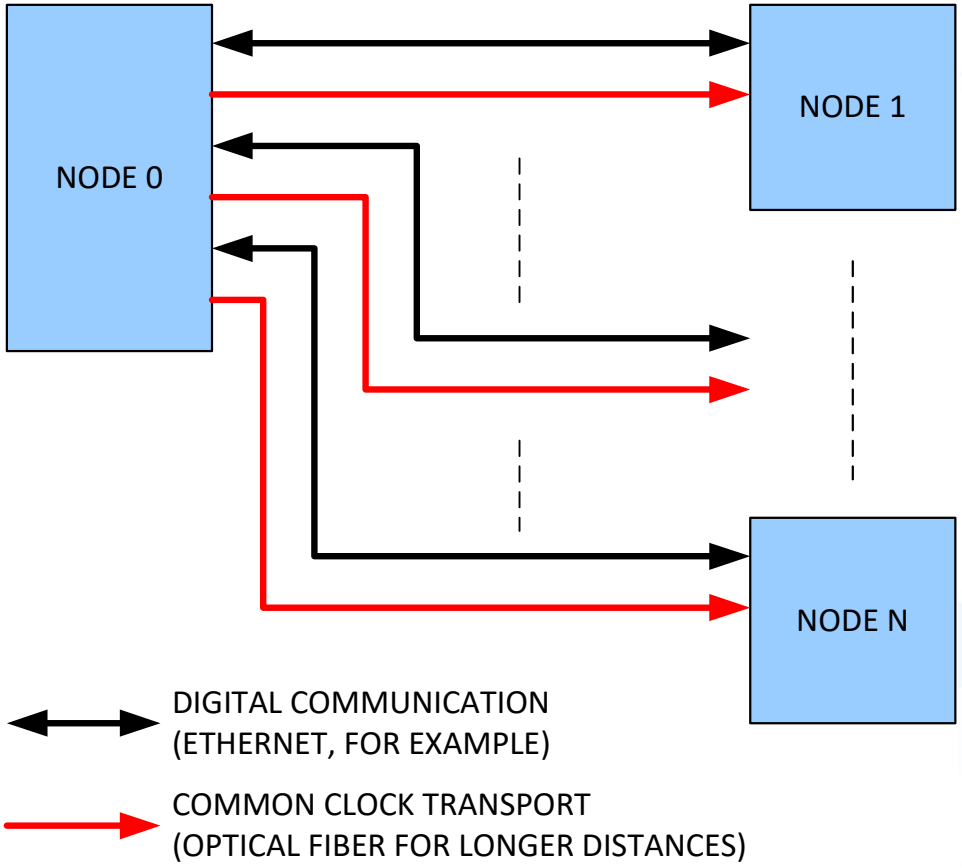
Digitized Clocking Value in Clocking Systems

- Clocks distributed digitally from a source to *x end-points* over a Digital Bus with precise frequency and phase.
- Number of clocks transmitted limited only by digital bus BW
- Uses one analog clock referred to as the common clock
- Phase delay errors are easily corrected digitally.
- No cross-coupling risks to other clock domains in the system
  - Eliminates risk mitigating strategies around this effect.
- Can be implemented using existing Backplane designs
  - Reducing analog clocking design
- System upgrades are backward compatible
- In a demo system, we achieved 100 ps synchronization
- In 5G systems: Ideally suited to meet synchronization requirements for IEEE-1588 boundary clocks per ITU-T G.8273.2 Subclass C (8 ns) and Subclass D (4 ns)



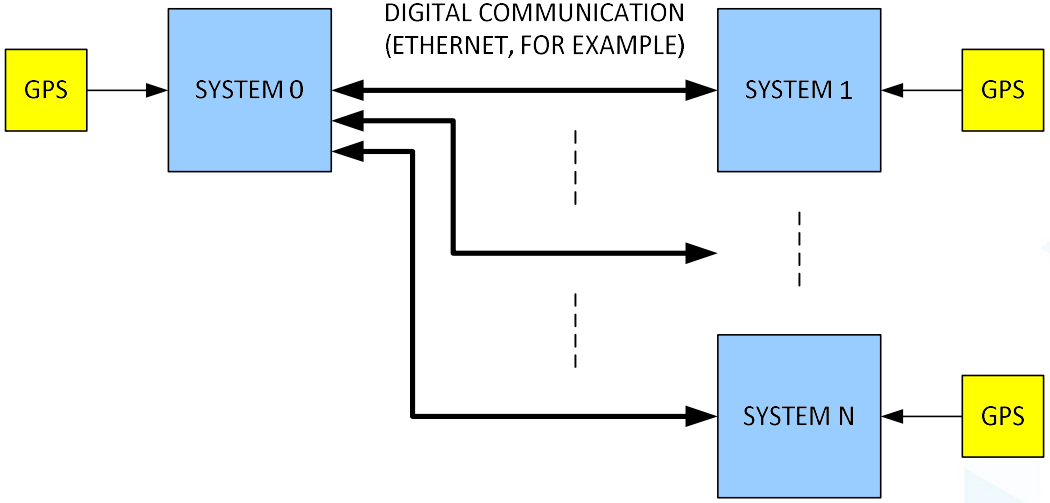
Applying Digitized Clocking to distributed systems

Using optical fiber for common clock transport



- If Nodes cannot be connected through PCB traces, then optical fibers can be used
- Common clock transported through optical fiber
- Epoch:
  - 1Hz clock transported embedded in the common clock
  - Main node sends a sync command through digital communication bus
- Time codes transported through digital communication bus (Ethernet, for example)

Synchronizing distributed systems equipped with GPS



- Multiple systems, each equipped with GPS → all can have the same time base
  - All systems have the same time base
  - GPS works as the common clock between all systems
- But a sync signal to create the common time base epoch is still needed
  - 1Hz clock already provided by GPS
  - Main node sends a sync command through digital communication bus
- System 0:
  - time stamps the clock that needs to be synchronized across all systems
  - Sends the time codes to Systems 1, 2, …, N
- Systems 1, 2, …, N recreate the clock in phase and frequency

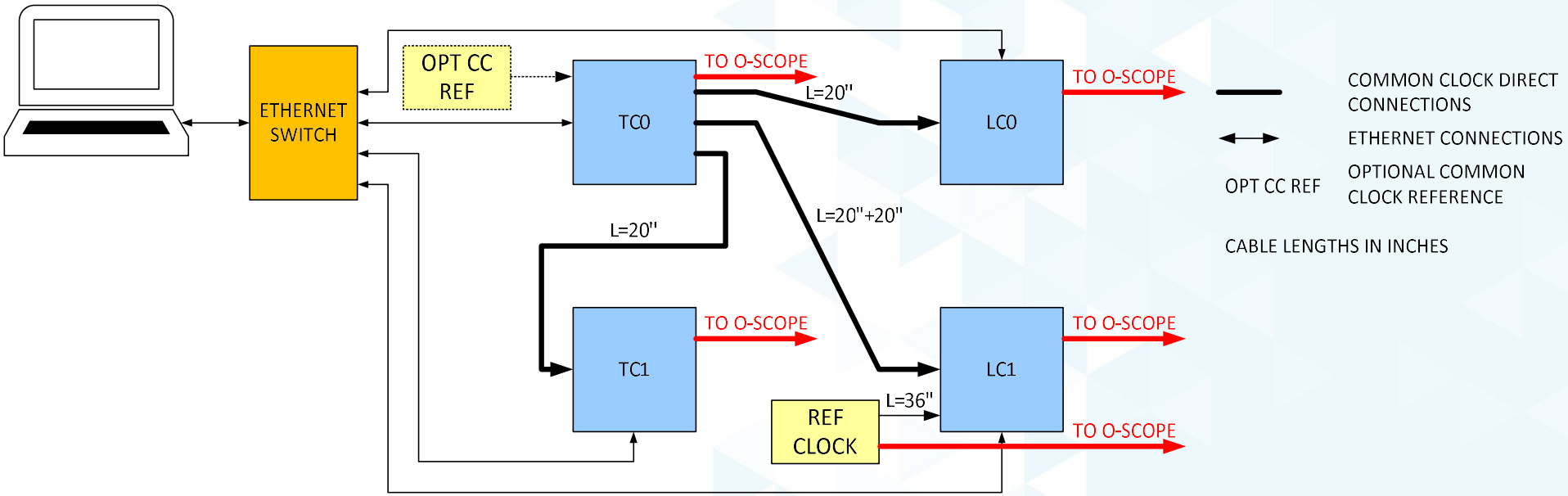
- Issues:
  - every system must have GPS and this may not be possible or feasible
  - If GPS disappears from one system, that system may lose its synchronization with the other systems that have GPS

AD9546 Digitized Clocking Eval System

AD9546 Digitized Clocking Evaluation System

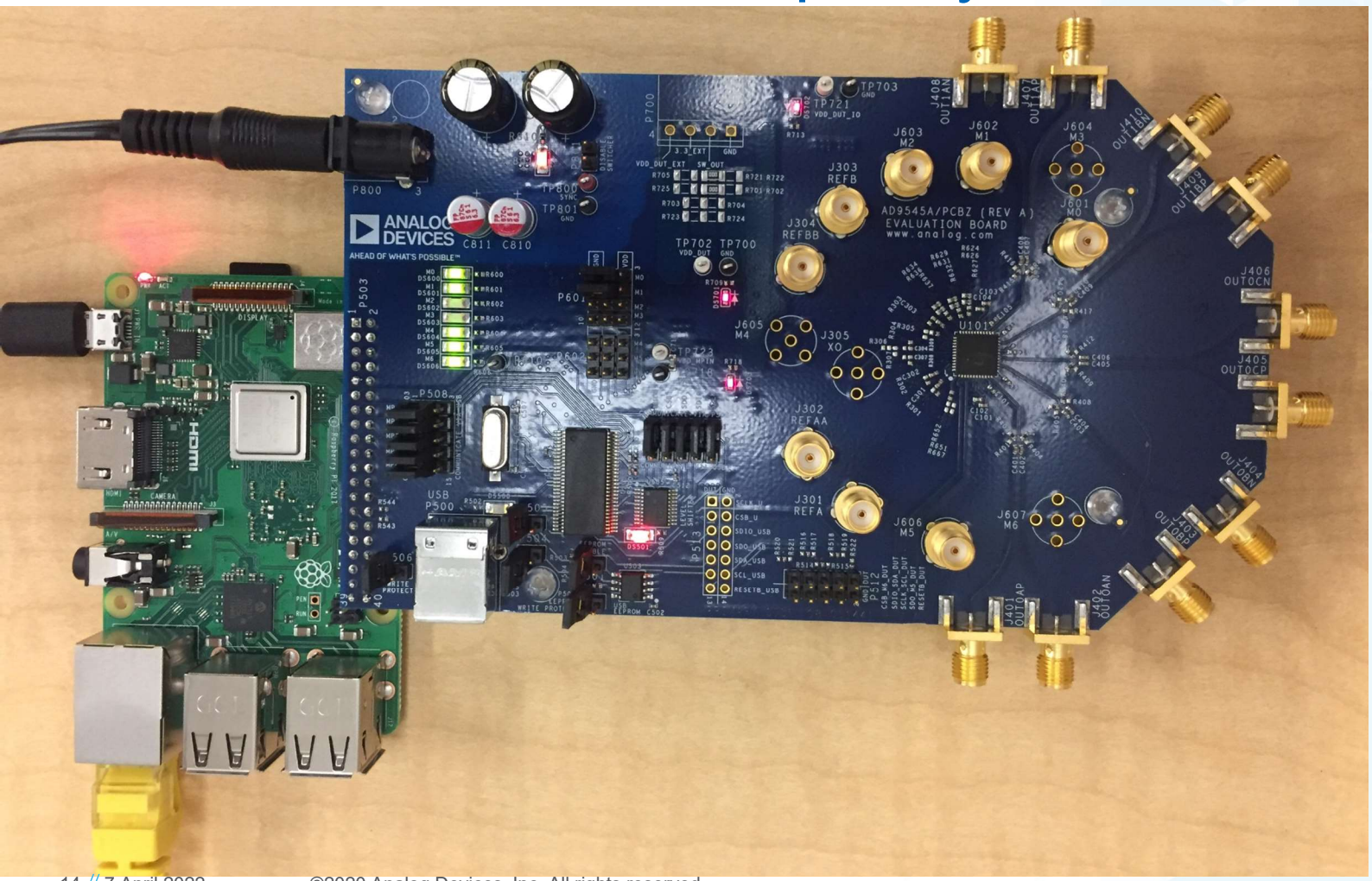
- Platform to evaluate Digitized Clocking technology
- Simulates a typical multiline card Network switch/router from the clock transportation perspective
- Both the frequency and phase of the reference clock are transported over a single digital bus
- Uses up to 6 AD9546 evaluation boards
  - 2 are considered master nodes and are called Timing Cards
  - Remaining boards are called Line Cards
- Supports multiple configurations:
  - 1T2L = one timing card and two line cards
    - Frequency and phase transport
    - Frequency transport only is also supported
  - 2T2L = two timing cards and two line cards
    - Frequency and phase transport
  - 2T3L, 2T4L
- **These slides present only the 2T2L configuration frequency and phase transport**

Evaluation System Concept



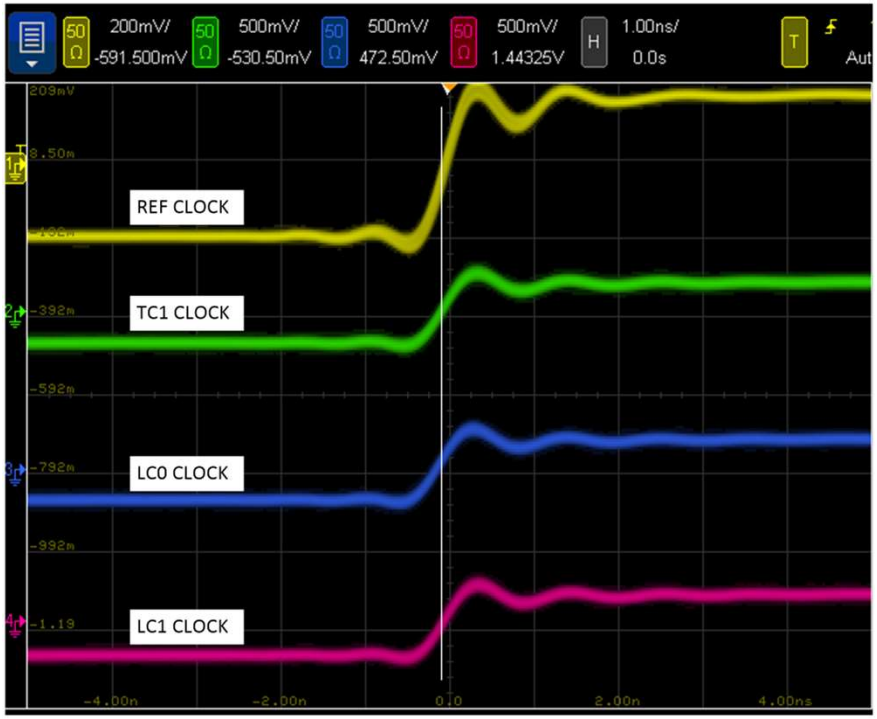
- Clocks are then showed on oscilloscope having the same frequency and being in phase with the reference clock at LC1
- PC based software manages the process

Card = AD9546 and Raspberry PI 3 Model B+



- Each AD9546 is managed by a Raspberry PI 3 Model B+ through SPI
- Raspberry PI MCU implements Ethernet comm between cards
  - Any ctrl/comms bus in the system can be used
    - Ex: OaM (Operations and Maintenance) bus is fine
- Digitized Clocking Time Codes are distributed using Ethernet

2T2L Frequency and Phase Transport Results



- Recovered clocks at TC1, LC0 and LC1 perfectly aligned to Reference clock provided at LC1
- Recovered clocks also have the same frequency
- 1T2L results are identical
  - TC0 clock replaces TC1 clock in the picture

Backup: 1T2L Connections