

A

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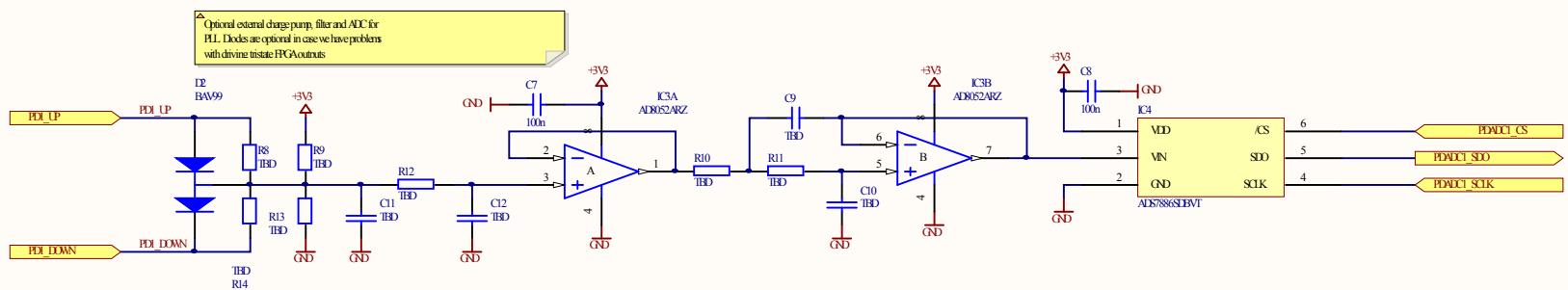
E

C

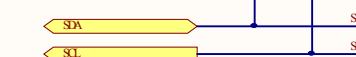
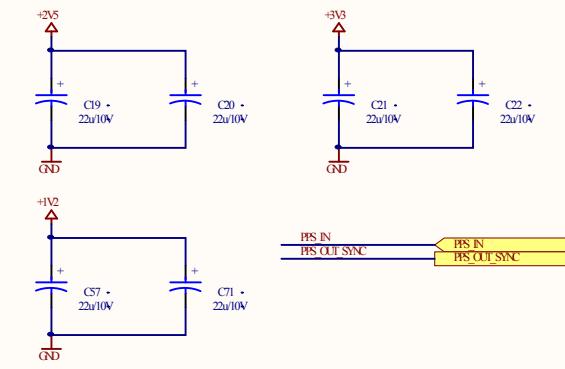
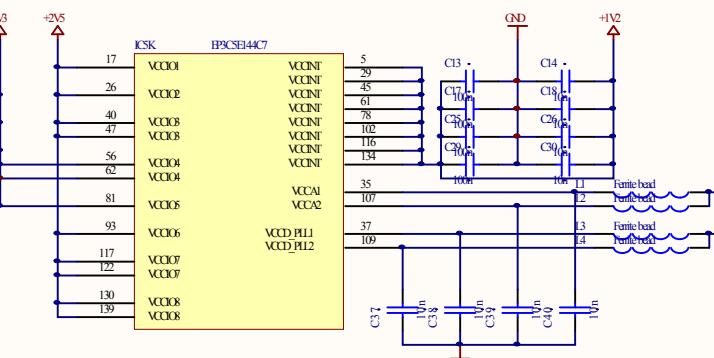
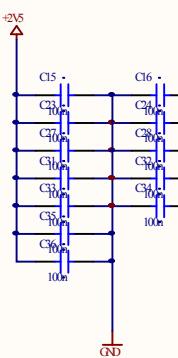
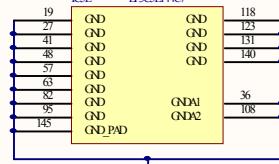
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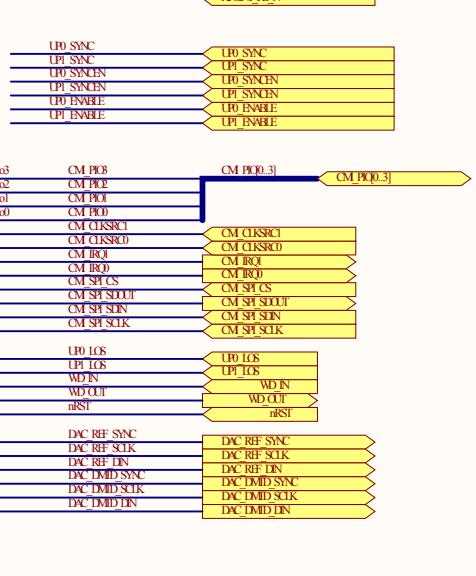
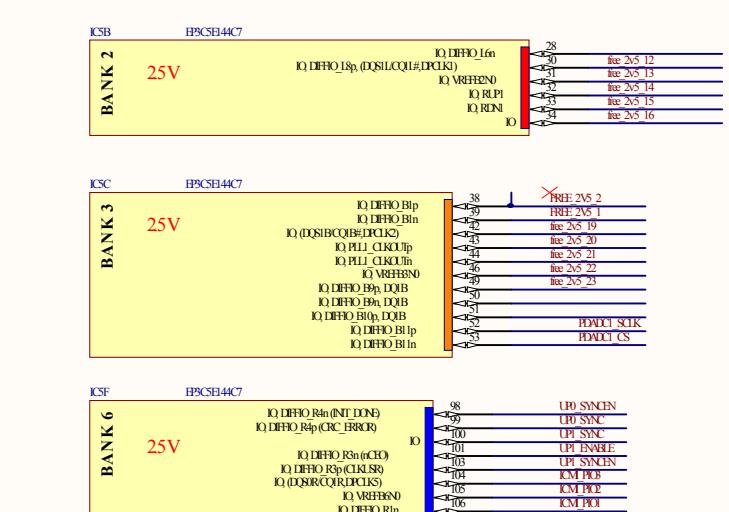
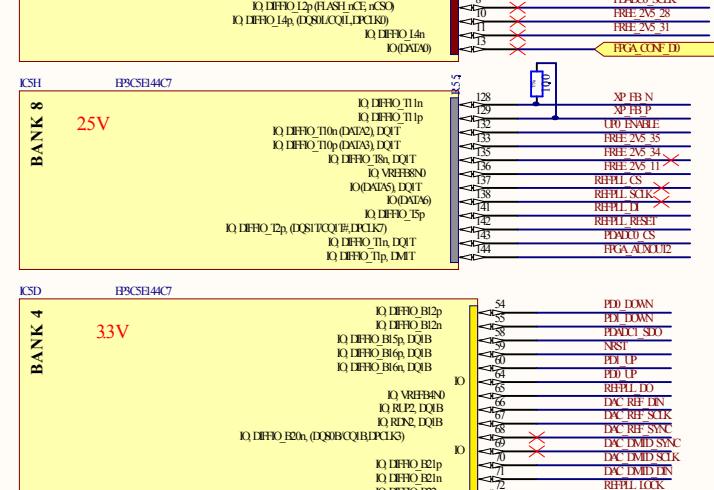
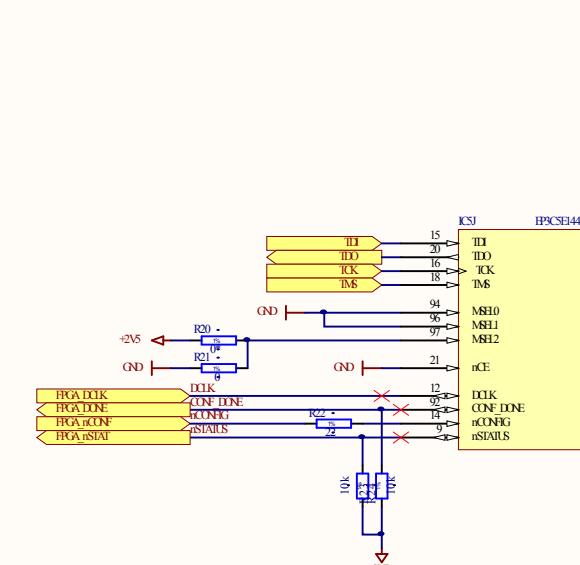
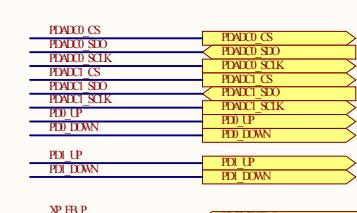
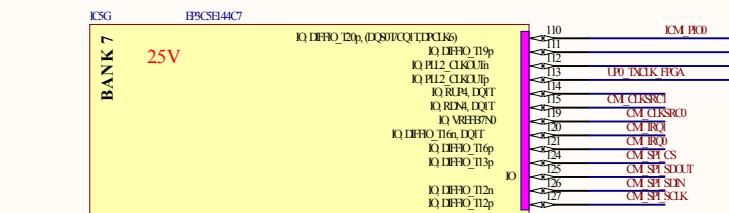
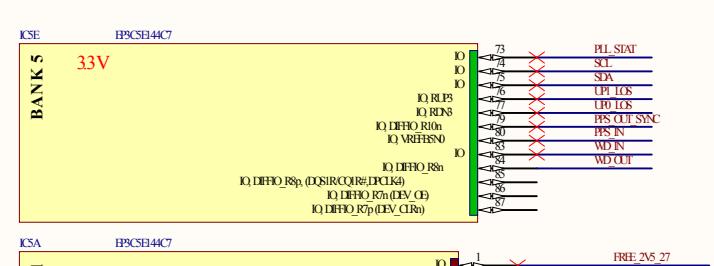
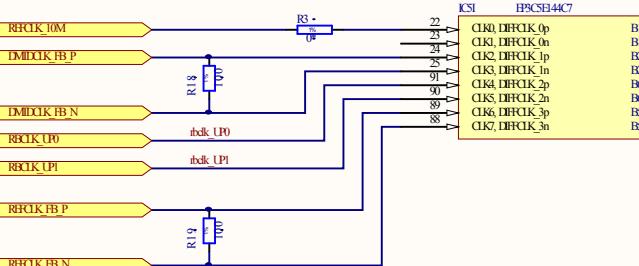
四



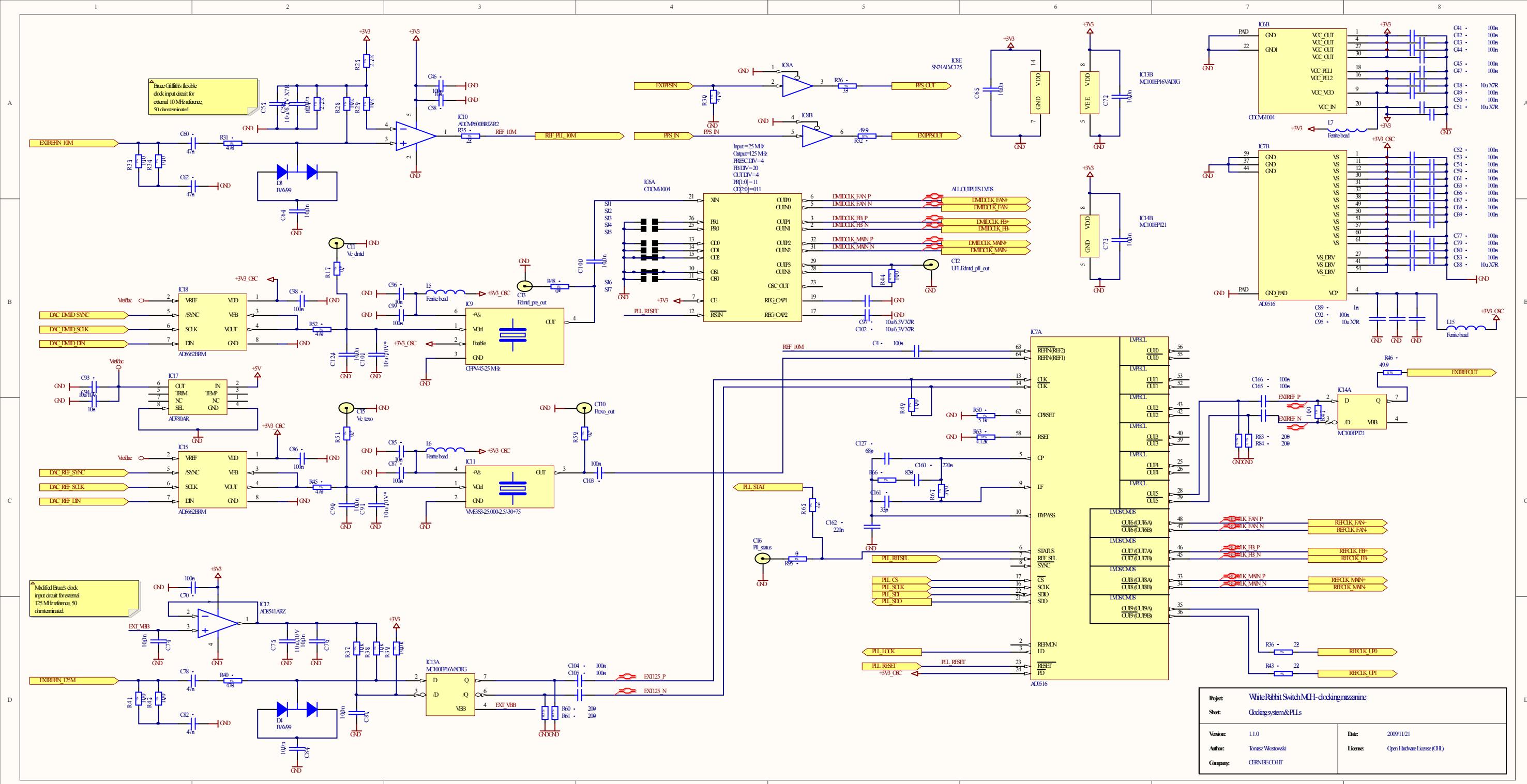
<b>Title</b>	<b>WhiteRabbit Switch MCH-I docking mechanism Analog phase detector &amp; ADC</b>	
<b>Size</b>	<b>Number</b>	<b>Revision</b>
A		0.05
<b>Date</b>	2010/04/01	<b>Sheet of</b>
<b>File</b>	<i>Z:\home\CKB\analog_phase_detector\SchDoc</i>	<b>Drawn By</b>

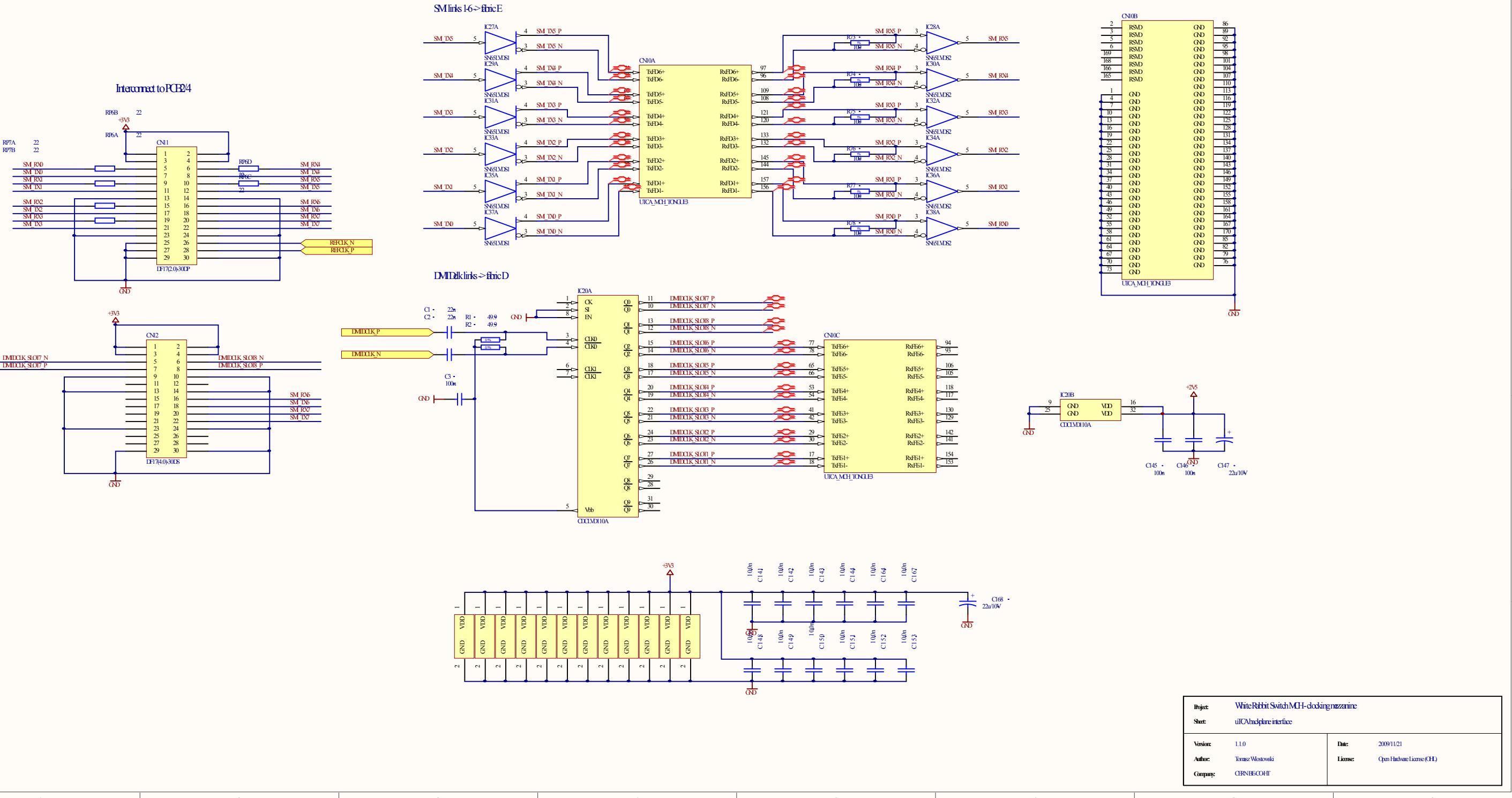


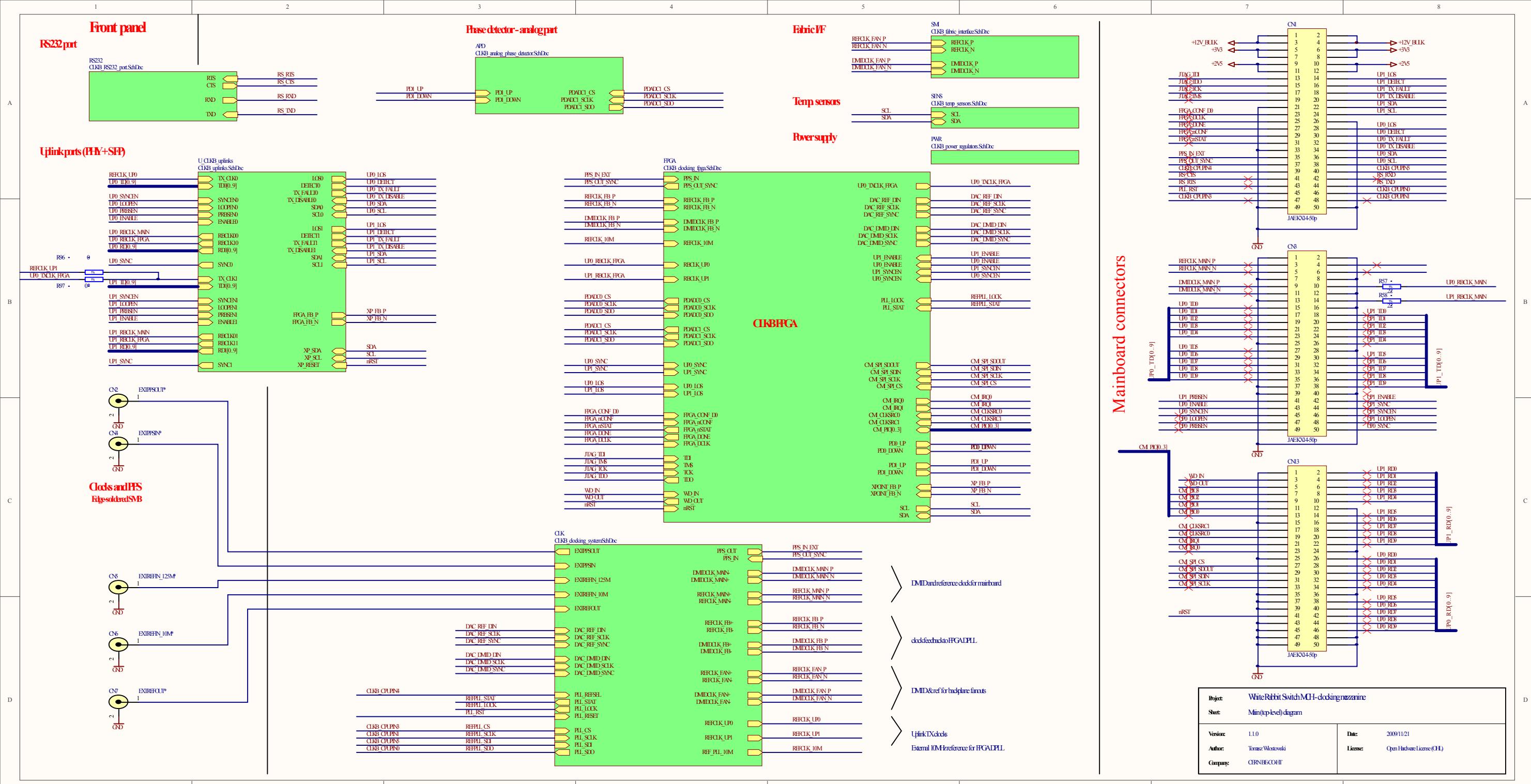
PC addresses:  
ADN4600: 0x90  
IMP100: 0x91 0x92

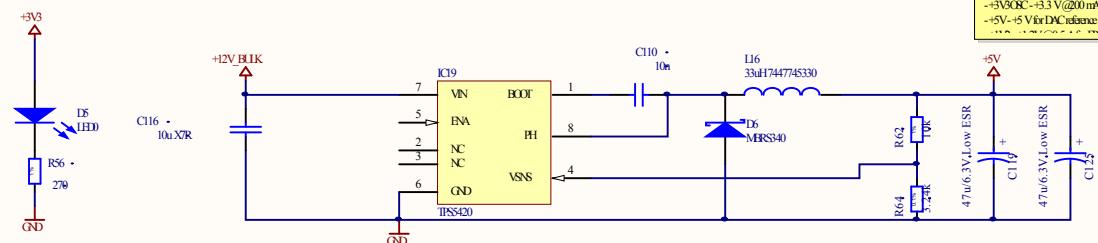


<b>Project:</b>	WhiteRabbit Switch MII-clocking nzzanine
<b>Sheet:</b>	ClockingPGA
<b>Version:</b>	1.1.0
<b>Author:</b>	Tomasz Włostowski
<b>Company:</b>	CRBN BECOH
<b>Date:</b>	2009/11/21
<b>License:</b>	Open Hardware License (OHL)



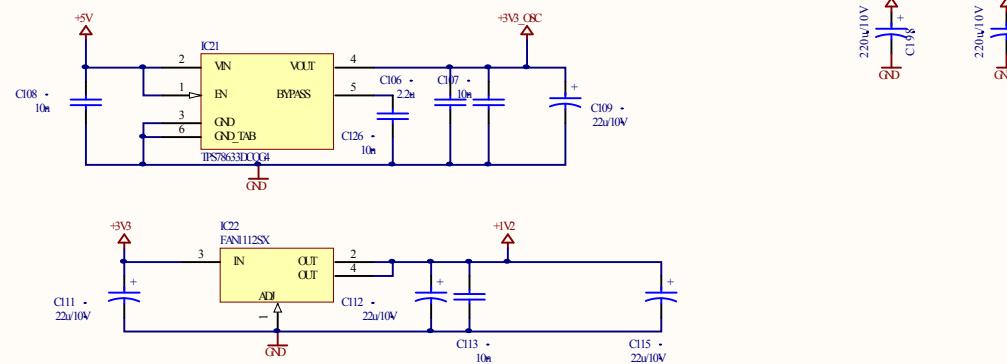






**Input voltages (from main MCH board):**  
 - +12V\_BULK backplane bulk power (+12 V)  
 - +2V5 from main regulator (+2.5 V, several amps)  
 - +3V3 from main regulator (+3.3 V, several amps)

**Output voltages:**  
 - +3V3\_BULK: +3.3 V @ 200 mA ultralownoise supply for VCSOs and DACs  
 - +5V: +5 V for DC reference and +3V3\_BULK LDO supply



Title: White Rabbit Switch MCH-clocking pizarrine Power supply regulators		
Size: A4	Number:	Revision:
Date: 20100401		Sheet of 1
File: Zhome_C1KB power regulators ShDc		Drawn By:

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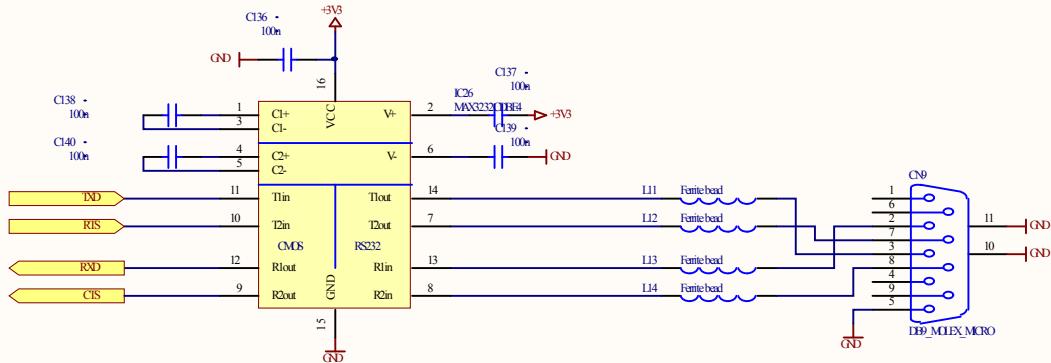
D

A

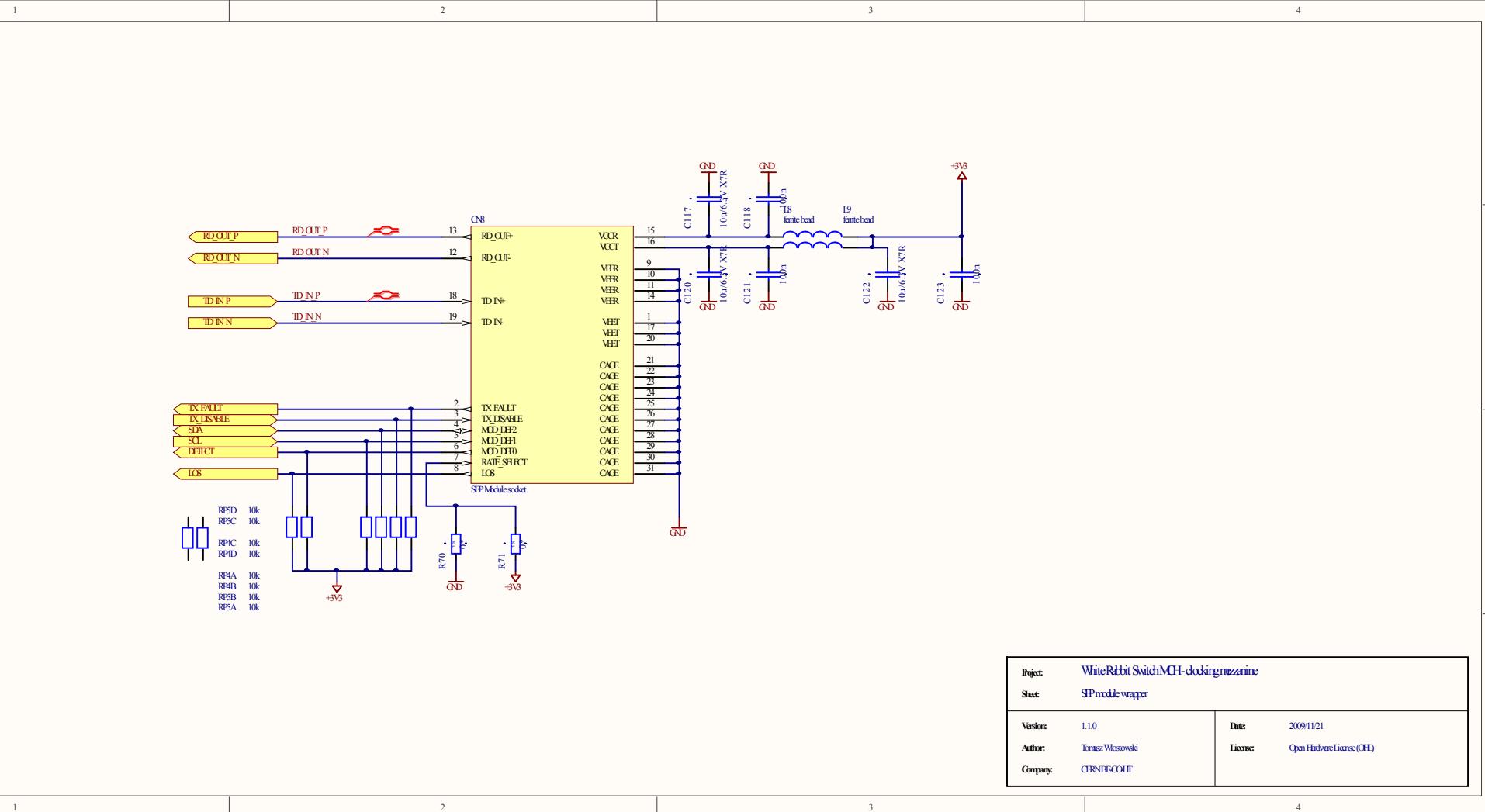
B

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Title		
White Rabbit Switch MCH clocking mezzanine		RS232 port
Size A		Number
Date	20100401	Sheet of
File	Zhome_C1KB_RS232_port_SchDc	Drawn By:



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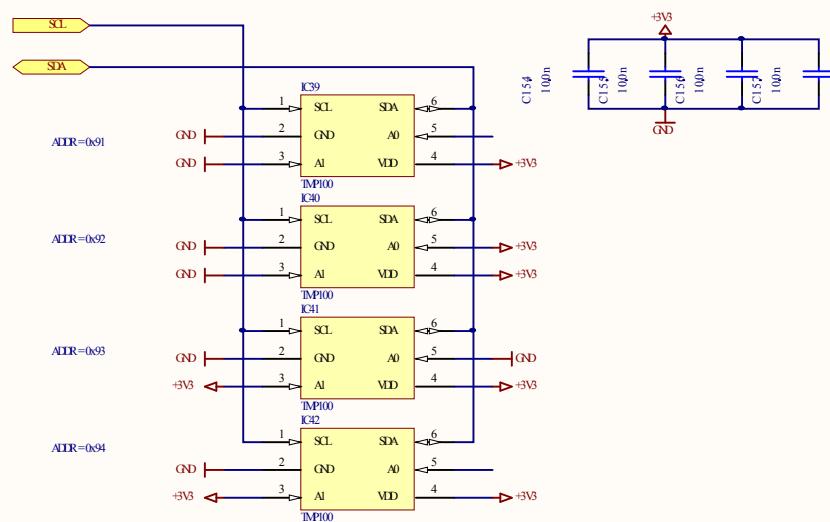
E

C

C

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E



<b>Title</b>	<b>WhiteRabbit Switch MCH-docking nozzle Temperature sensors</b>		
<b>Size</b>	Number		Revision
A			
<b>Date</b>	2010-04-01	<b>Sheet of</b>	
<b>File</b>	zplane_CIRB temp_sensors.Slddrw	<b>Drawn By:</b>	
3		4	

