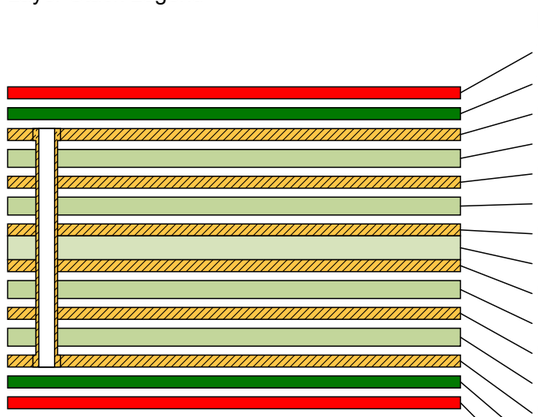
| REV | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| X1 | ADDED Y5 CIRCUIT | 04/14/2023 | |
| | | | |
| | | | |

Layer Stack Legend



| Layer | Thickness | Description |
|---|---|---|
| Top Overlay | | |
| Top Solder | 0.043mm | |
| L01-Top Layer | 0.035mm | Copper Foil |
| *0.074mm* | | |
| L02-GND | 0.035mm | Copper Foil |
| *0.095mm* | | |
| L03-PWR | 0.035mm | Copper Foil |
| *0.920mm* | | |
| L04-PWR | 0.035mm | Copper Foil |
| *0.095mm* | | |
| L05-GND | 0.035mm | Copper Foil |
| *0.074mm* | | |
| L06-Bottom Layer | 0.035mm | Copper Foil |
| Bottom Solder | 0.043mm | |
| Bottom Overlay | | |

Total thickness: 1.555mm

TABLE 1: DIFFERENTIAL CONTROLLED IMPEDANCE

| Trace layer | Reference layers | Target Impedance | Wide Trace Width | Gap | Target Tolerance |
|---|---|---|---|---|---|
| L01-Top Layer | L02-GND | 50 | 0.102mm | | 10% |
| L01-Top Layer | L02-GND | 100 | 0.101mm | 0.203mm | 10% |
| L06-Bottom Layer | L05-GND | 50 | 0.102mm | | 10% |
| L06-Bottom Layer | L05-GND | 100 | 0.101mm | 0.203mm | 10% |

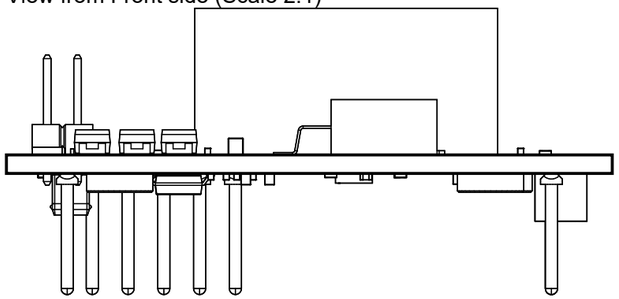
TABLE 2: SINGLE ENDED CONTROLLED IMPEDANCE

| Trace layer | Reference layers | Target Impedance | Wide Trace Width | Target Tolerance |
|---|---|---|---|---|
| L01-Top Layer | L02-GND | 50 | 0.102mm | 10% |
| L06-Bottom Layer | L05-GND | 50 | 0.102mm | 10% |

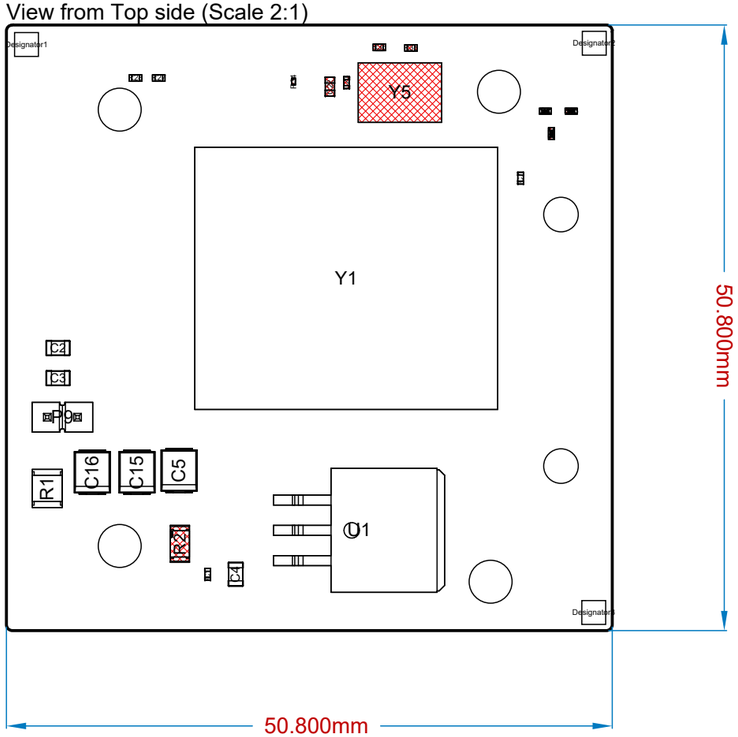
NOTES: UNITS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

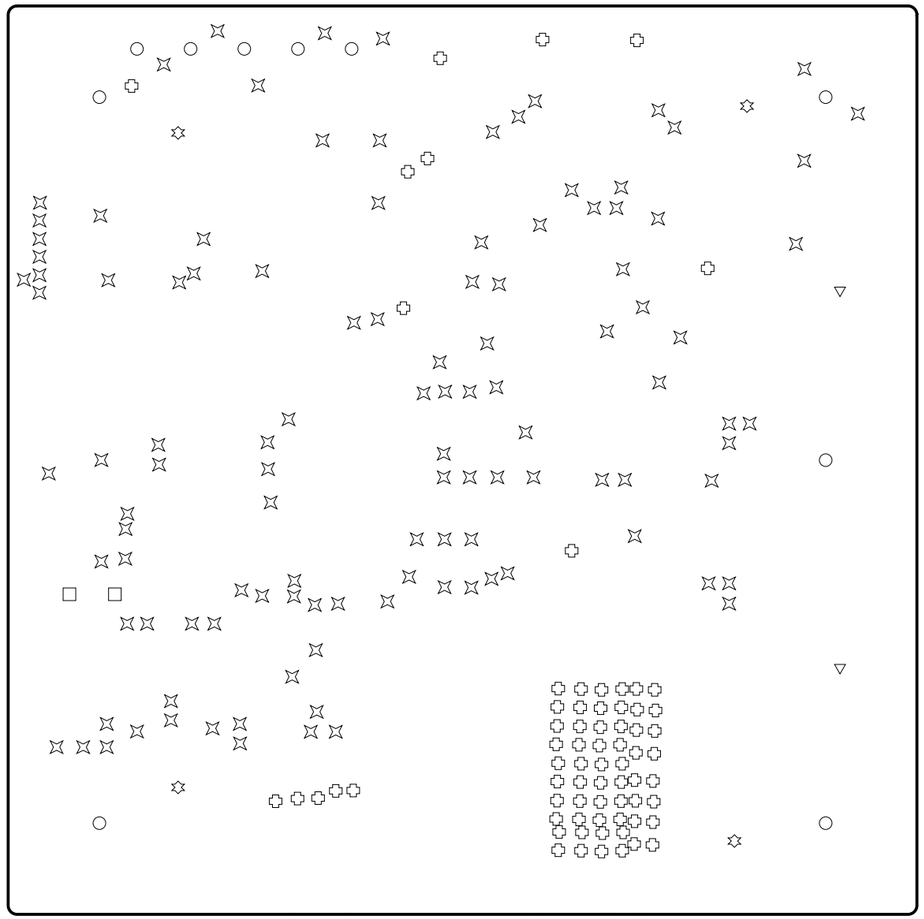
1. INTERPRET THIS DRAWING IN ACCORDANCE WITH IPC-D-325A.
2. BOARD FABRICATION AND QUALITY PER IPC-6012, CLASS 2, EXCEPT SPECIFIED HEREIN.
3. MUST COMPLY WITH EUROPEAN DIRECTIVE 2002/95/EC (RoHS).
4. DIMENSIONAL LIMITS APPLY AFTER PLATING OR COATING.
5. BOW AND TWIST MAXIMUM IS 0.75%.
6. MATERIAL: LAMINATE AND PREPREG SHALL BE IN ACCORDANCE WITH IPC-4101/21. 170 DEGREES CELSIUS MINIMUM Tg, UL 94V-0.
7. STACKUP SUMMARY:
   A. NUMBER OF COPPER LAYERS: 6
   B. BOARD THICKNESS SHALL BE 1.55mm +/- 10%
   C. COPPER: See Layer Stack
   D. DEFAULT TRACE/SPACE: 0.1mm/0.2mm
   E. CONDUCTOR WIDTH TOLERANCE = +/- 0.01mm
8. VIPPO (VIA IN PAD PLATED OVER) PER IPC-6012, CURRENT REVISION, CLASS 2, AS STATED IN NOTE 2.
   A. FILL AND CAP All 0.3mm VIA HOLES WITH COPPER.
   B. FILL AND CAP VIAS MUST BE PLANARIZED.
9. SURFACE FINISH/PLATING:
   A. BOARD SHALL BE IMMERSION GOLD PLATED (ENIG) ACCORDING TO IPC-4552. THICKNESS SHALL BE A MINIMUM OF 0.05µm GOLD OVER 3-6µm NICKEL.
10. SOLDERMASK WITH LIQUID PHOTO IMAGEABLE (LPI) PER IPC-SM-840C, CLASS T.
    COLOR: BLACK
11. SILKSCREEN PER SUPPLIED ARTWORK WITH ORGANIC, NON-CONDUCTIVE, EPOXY INK. SILKSCREEN MAY BE TRIMMED OFF ANY SOLDERABLE ENTITY.
    COLOR: WHITE
12. 100% BARE BOARD ELECTRICAL TEST TO BE DONE WITH REFERENCE TO SUPPLIED NETLIST.
13. LOCATE MANUFACTURER'S IDENTIFICATION AND LOT CODE ON PRIMARY SIDE FREE FROM ALL METAL ENTITY RENDERED IN SILKSCREEN.
14. DIFFERENTIAL CONTROLLED IMPEDANCE REQUIRED ON BOARD.
    SEE TABLE 1: DIFFERENTIAL CONTROLLED IMPEDANCE
    SEE TABLE 2: SINGLE ENDED CONTROLLED IMPEDANCE
15. DETAILS NOT SPECIFIED ARE AT MANUFACTURER'S OPTION BUT FINAL APPROVAL MUST BE OBTAINED FROM META.

View from Front side (Scale 2:1)



View from Top side (Scale 2:1)



Drill Drawing View (Scale 3:1)

Drill Table

| Symbol | Count | Hole Size | Plated | Drill Layer Pair | Via / Pad | Hole Tolerance |
|---|---|---|---|---|---|---|
| ⛝ | 114 | 0.300mm | Plated | L01-Top Layer - L06-Bottom Layer | Via | +0.000mm/-0.300mm |
| ⛒ | 70 | 0.300mm | Plated | L01-Top Layer - L06-Bottom Layer | Via | |
| □ | 2 | 1.020mm | Plated | L01-Top Layer - L06-Bottom Layer | Pad | +/-0.076mm |
| ○ | 10 | 1.090mm | Plated | L01-Top Layer - L06-Bottom Layer | Pad | +/-0.076mm |
| ▽ | 2 | 3.000mm | Non-Plated | L01-Top Layer - L06-Bottom Layer | Pad | +/-0.051mm |
| ✡ | 4 | 3.700mm | Plated | L01-Top Layer - L06-Bottom Layer | Pad | +/-0.075mm |
| | 202 Total | | | | | |