AX88279 USB 3.2 Gen1 to 2.5G Ethernet Application Design Note

Revision 1.00
October 29th, 2024

Revision History

Revision	Date	Description
V0.10	2023/02/24	Preliminary Release
V0.20	2023/03/20	Modified some description in Section 2.
V1.00	2024/10/29	Corrected some description in Section 7 & 8 & 13.

Content

Figures

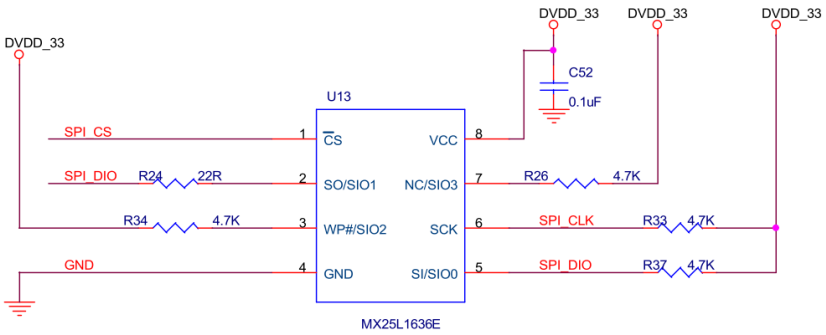
1. Introduction

The AX88279 USB 3.2 Gen1 to 100M/1G/2.5Gigabit Ethernet controller is a high performance and highly integrated ASIC which enables low cost, small form factor, and simple plug-and-play 2.5Gigabit Ethernet network connection capability for desktops, notebook PC's, Ultrabook's, docking stations, game consoles, digital-home appliances, and any embedded system using a standard USB port.

This Application Design Note provides important information about external component selection, schematic design and PCB design/layout for designing with ASIX Electronics' AX88279 USB 3.2 Gen1 to 2.5Gigabit Ethernet controller. ASIX Electronics highly recommends that user read through this Design Note before starting hardware design on schematic capture and PCB layout.

2. External SPI Flash Selection Considerations

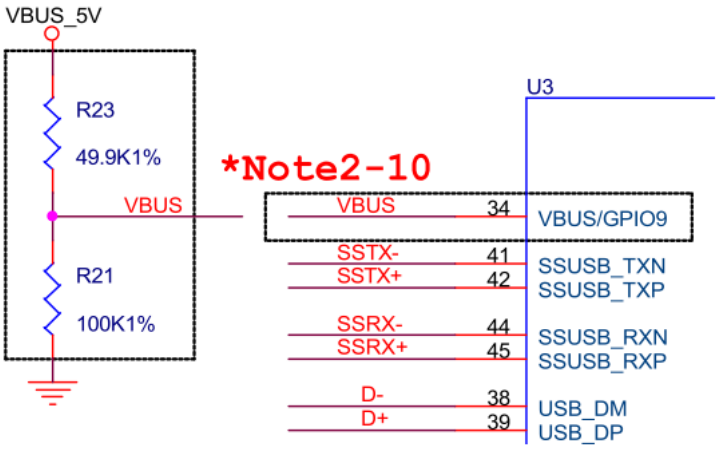
The following is the SPI Flash reference circuit of AX88279 USB 3.2 Gen1 to 2.5Gigabit Ethernet application.



Note:

1. The AX88279 supports external SPI flash, the Flash size must be supported to 8Mbit above.
2. SPI flash must be closed to AX88279, the path distance of SPI as short as possible.

3. VBUS pin Design Considerations



VBUS	I3/S	34	VBUS signal of USB. (GPIO9)

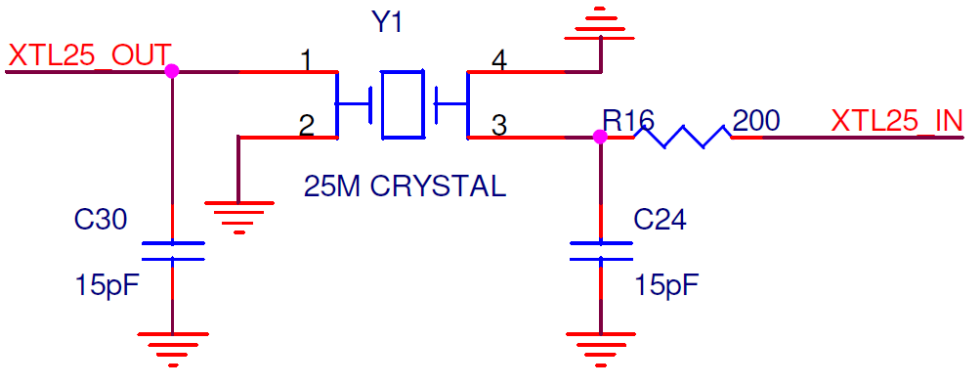
The AX88279 VBUS is a 3.3v pin input, the VBUS pin of AX88279 should be connected to the 3.3V level, which power source needs from the VBUS signal(5V) of USB connector, to judge the USB port is attached or not. AX88279 VBUS pin should be at low if AX88279 device is detach. e.g., If your application is connected to next layer of USB hub, the VBUS pin of AX88279 shall connect to VBUS pin of USB hub.

4. Crystal Selection Considerations

The following is the specification of NSK NXK25.000AE12F-KAB6-12 SMD 25Mhz crystal with CL 15pF and Drive Level 100uW, for AX88279 USB 3.2 Gen1 to 2.5G Ethernet application.

Parameter	Symbol	Typical Value
Nominal Frequency	Fo	25.000000MHz
Oscillation Mode		Fundamental
Frequency Tolerance (@25℃)		±20ppm
Frequency Stability (-40 to +105℃)		±30ppm
Equivalent Series Resistance	ESR	40 Ohm max.
Load Capacitance	CL	12pF
Drive Level		100uW
Operation Temperature Range		-40℃ ~ +105℃
Aging		±3ppm/year

The following is an example of the 25MHz crystal clock circuit.



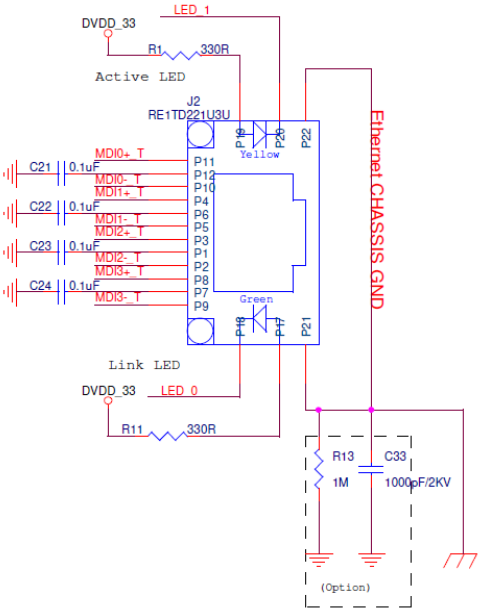
Note:

1. Please make sure the XTL25_IN 25MHz clock output signals are within 25MHz +- 30ppm. If the XTL25_IN 25Mhz clock output signals are out of the specification, please fine-tune the load capacitors (C24, C30) to meet the specification.

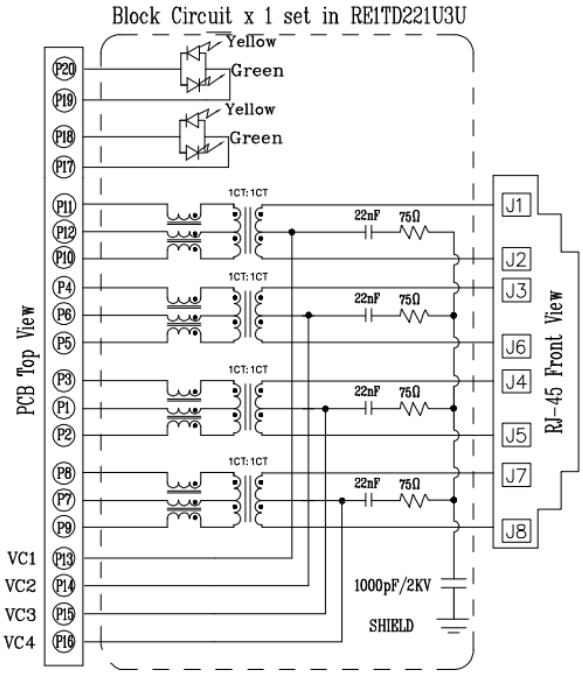
5. Ethernet Magnetics Selection Considerations

5-1 Single RJ-45 Connector (with integrated 2.5G Base-T magnetics)

The following is the reference Ethernet magnetics circuit (single RJ-45 connector integrated 2.5G Base-T magnetics with Turns Ratio 1CT:1CT) on AX88279 demo board.

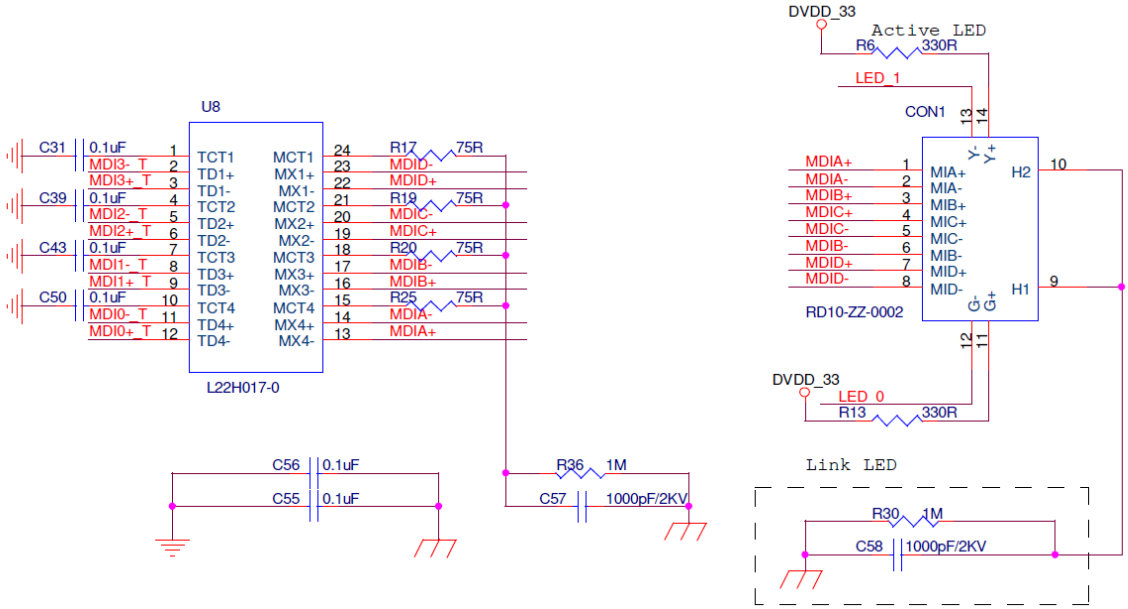


The following is an example (Bothhand RE1TD221U3U) of single RJ-45 connector (with integrated 2.5G Base-T magnetics).

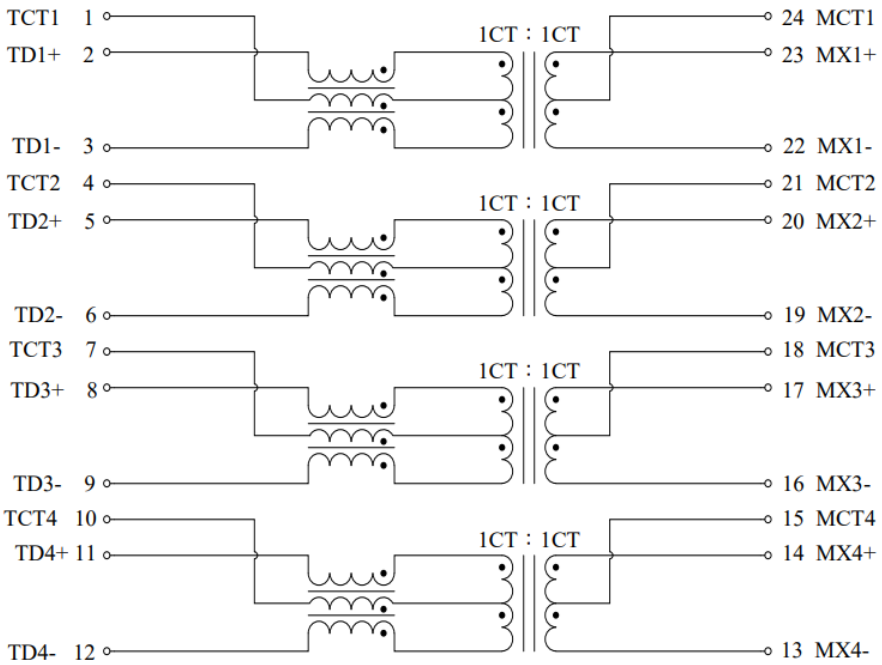


5-2 Separate 2.5G Base-T Magnetics and RJ-45 Connector

The following is an example reference circuit of separate 2.5G Base-T magnetics (Turns Ratio 1CT:1CT) and RJ-45 connector.



The following is an example (UDE L22H017-0) of 2.5G Base-T magnetics (Turns Ratio 1CT:1CT).



6. 4-Layer PCB Design

We strongly suggest customers to design AX88279 USB 3.2 Gen1 to 2.5G Ethernet controller on the printed circuit board (PCB) with at least 4 layers. The 4-layer PCB design can help reduce some potential EMI, thermal and signal integrity issues, etc.

The following is an example 4-Layer PCB design for an embedded system application that uses AX88279 USB 3.2 Gen1 to 2.5G Ethernet controller.

Layer 1	Component (Top)	Magnetics and major signals
Layer 2	Ground	Digital/analog ground planes
Layer 3	Power	Digital/analog power planes
Layer 4	Component (Bottom)	Magnetics and other signals

Figure 1. An Example of 4-Layer PCB Design

7. Power and Ground Planes Considerations

1. Digital GND and Analog GND can be placed together in one-piece so as to enlarge the GND, and thus helping dissipation of noises.

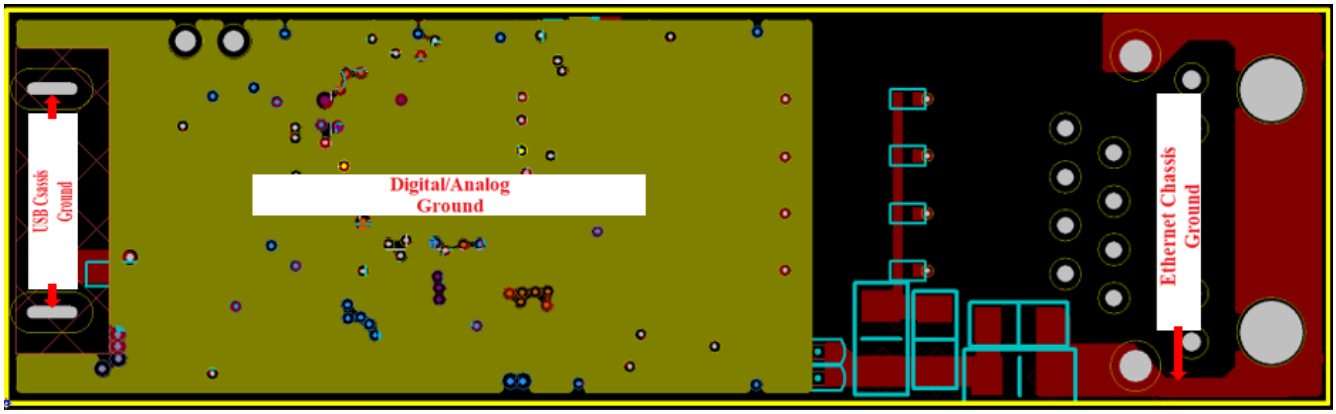
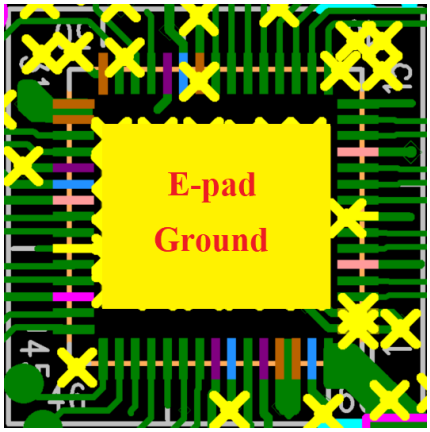


Figure 2. Typical Digital/Analog/Chassis Ground Planes

2. Connect AX88279 GNDK E-pad to digital ground plane to reduce AX88279 operating temperature.



3. The USB chassis ground and the digital ground should be isolated through a 1M Ohm resistor and a Ferrite Bead; the Ethernet chassis ground and the digital ground should be isolated through a 1000pF/2KV decoupling capacitor. And the gap between the chassis ground and digital ground must be wider than 80 mils.

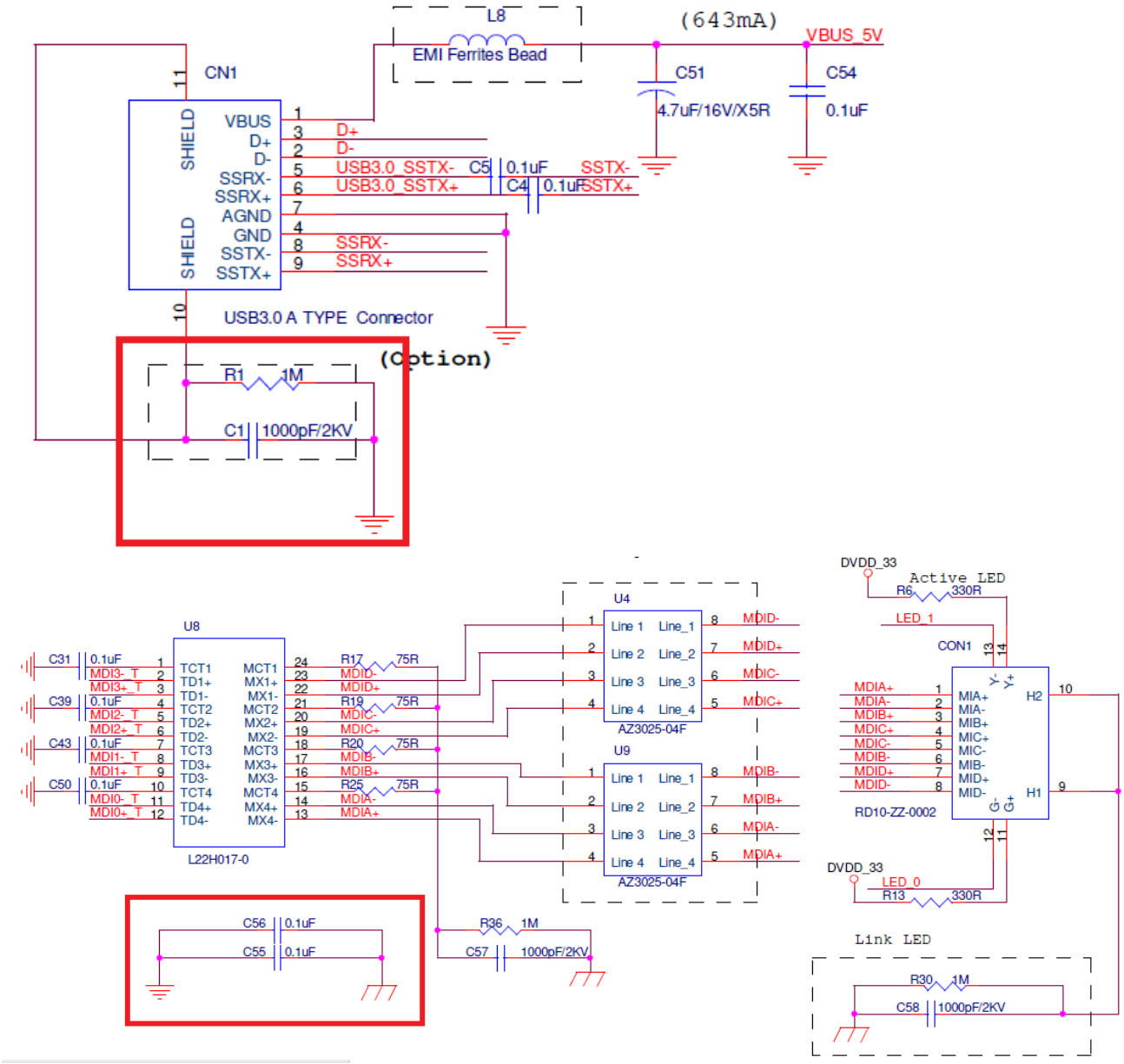


Figure 3. Typical Chassis/Digital/Chassis Ground Reference Circuit

4. All the digital and analog power planes for different voltage supplies should be handled separately with different blocks to supply power to IC chip and peripheral components.

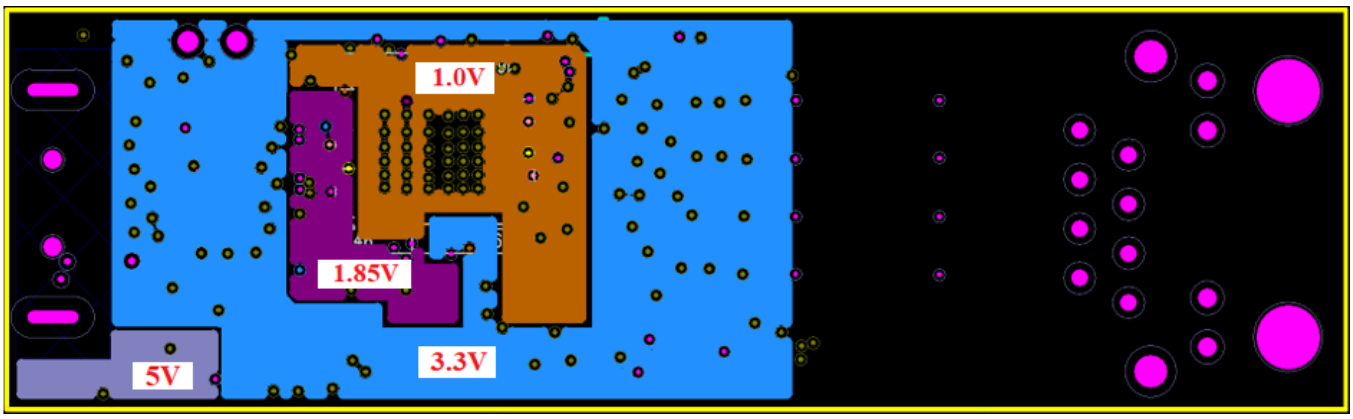
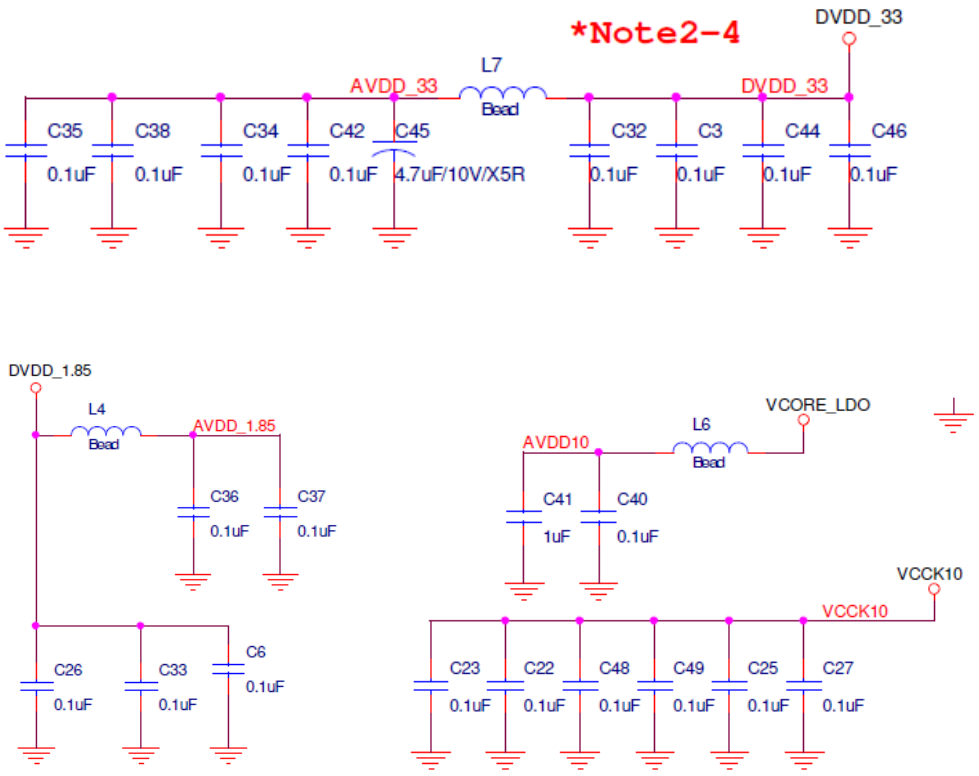


Figure 4. Typical Digital/Analog Power Planes

Note: The above figures are the Digital and Analog Power Planes diagram of an illustrative LAN board design. For exact layout pattern, ASIX Electronics provides AX88279 demo board PCB layout/Gerber files for customer reference.

5. The digital and analog power planes should be isolated with a Ferrite Bead to isolate the noise source, and all power planes should be implemented with a large compensating capacitor to provide a stable power source.



6. All power pins should be implemented with a decoupling capacitor, and the decoupling capacitor should be as close to the respective power pin of ASIX Ethernet controller as possible.

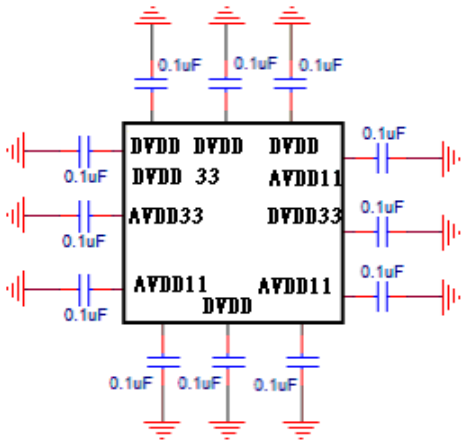
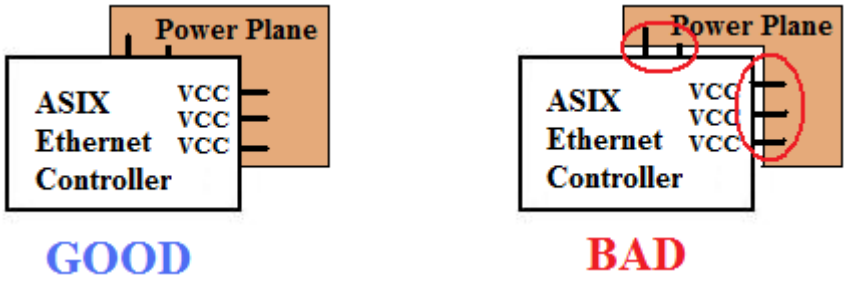


Figure 5. An Example of Power Pins and Decoupling Capacitors Circuits

7. Provide a power plane right underneath the ASIX Ethernet controller such that the VCC pins can be contacted to the power plane without going through thin traces.



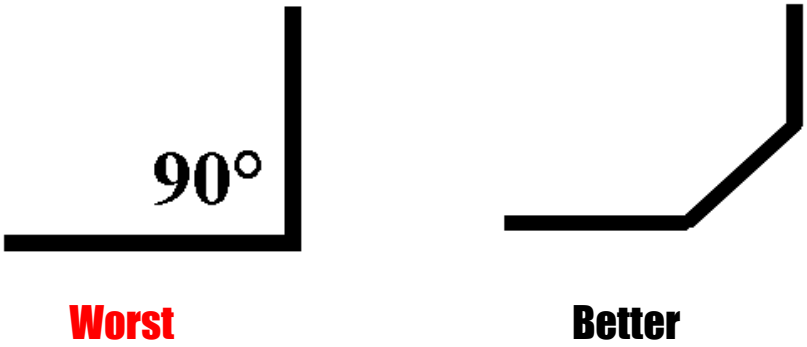
GOOD BAD

8. USB Layout Considerations

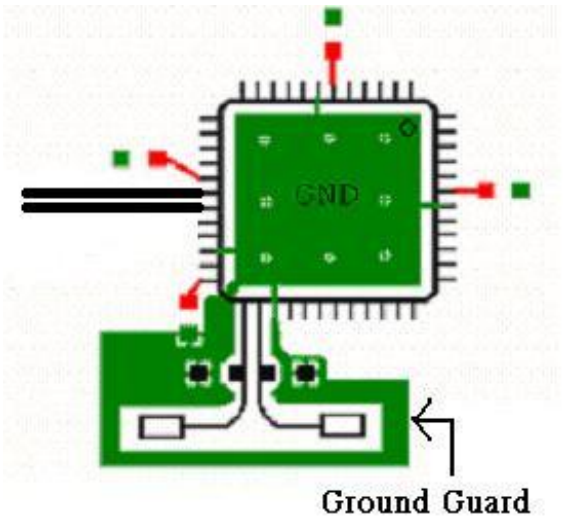
This section describes some general USB signal layout guideline for the differential signals of USB 3.2 Gen1/USB 2.0 interface and the USB connector.

8-1 USB Layout Notes

1. The USB differential signals should be routed with minimum trace length as short as possible.
2. The USB differential signals traces layout consideration should carefully avoid the nearby clock or noisy digital signals being routed too close to the signals.
3. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close to the AX88279 device as possible.
4. Match the lengths of the differential pair traces (i.e. SSTX±/SSRX±/D±). There should be less than 5 mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
5. AC coupling capacitors should be placed close to each other to minimize extra trace length.
6. Avoiding route the USB 3.2 Gen1 and USB 2.0 signals near the edge of PCB or power planes.
7. Avoiding any stubs and removing any routing that causes signal discontinuity and severe EMC noise issue.
8. Do not put any metal between all USB 3.2 Gen1 differential signal pair traces when using USB 3.2 Gen1 receptacle connector with pins stabbing the PCB.
9. To minimize the crosstalk issue, the routing of the signal traces between SSTX±/SSRX±/D± pairs should not be closed to each other.
10. The trace spacing between USB 3.2 Gen1 and USB 2.0 signals is 8 mils.
11. Route the differential pair traces parallel to one another and close together as much as possible. The traces should be symmetrical.
12. Different USB differential pairs should be isolated by proper wide ground traces.
13. Any 90-degree turn in trace routing should be accomplished with two 135-degree turns as shown in example below.

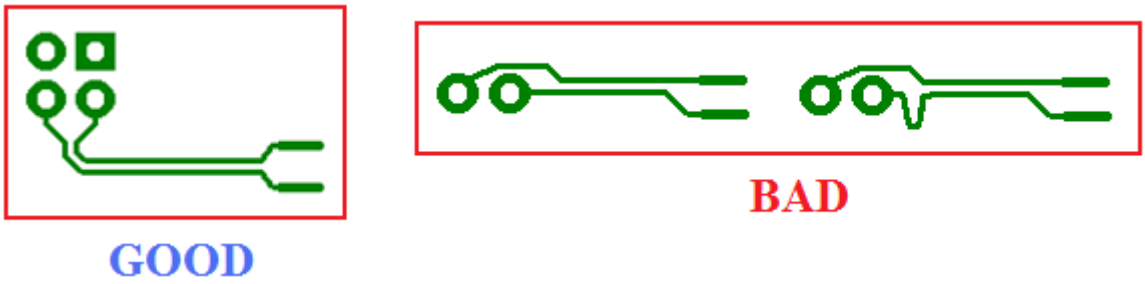


14. The X’tal (oscillator) traces shall be surrounded by GND to prevent interference to other signal wires. Better EMI effect can be attained by a one-piece GND underneath the IC furnished with PTH holes to enlarge the GND area.

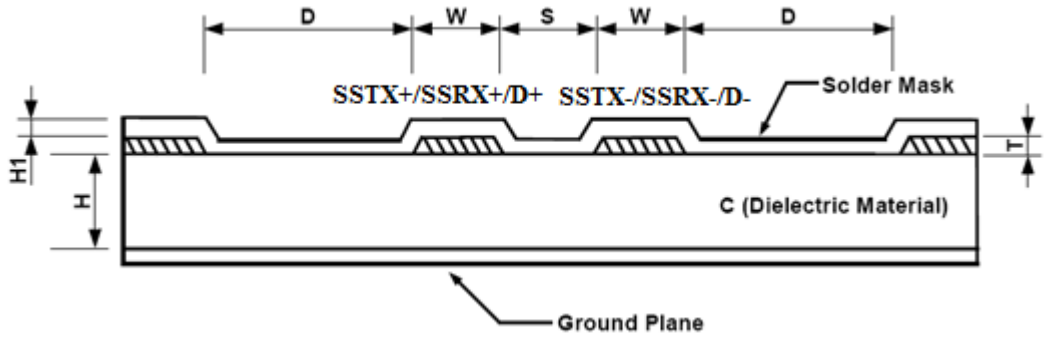


15. The X’tal traces shall be symmetrical and parallel in order to get better oscillation wave form and better EMI protection.

16. USB signal traces shall be placed parallel as below pictures.



8-2 PCB (FR4 material) and impedance



1. W = 8 mils
2. S (SSTX+/SSRX+/D+ to SSTX-/SSRX-/D-) = 8 mils
3. T = Thickness of the trace = 1 ounce copper
4. D (Ground Separation) ≥ 30 mils
5. H (Dielectric thickness, distance of trace from the ground plane. Board thickness) ≈ 63 mils. The H value is dependent on the PCB material and might need to be fined tune based on your real PCB material.
6. The ideal USB differential impedance between “SSTX+ & SSTX-”, “SSRX+ & SSRX-” and “D+ & D-“ traces should be 90 Ohm. The USB differential impedance between the SSTX+/SSTX-/SSRX+/SSRX-/D+/D- trace and GND should be 45 Ohm respectively. The designer can use the trace width of SSTX+/SSTX-/SSRX+/SSRX-/D+/D- traces to fine tune the USB differential impedance value (a wider trace has a smaller impedance value). If the PCB manufacturer provides TDR measurement, it helps control the PCB Impedance. You can fine tune the USB traces width with 90 Ohm impedance first and then fine tune the Ethernet traces width with 100 Ohm impedance.

8-3 USB Traces Routing for USB 3.2 Gen1 PHY and Connector

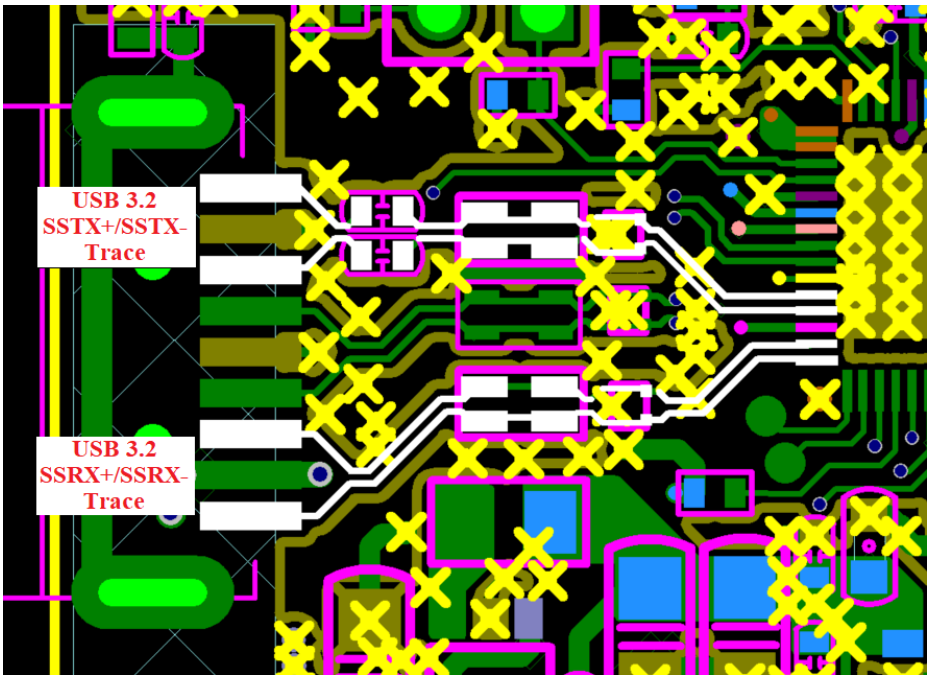


Figure 6. USB 3.2 Gen1 SSTX+-/SSRX+- Traces Routing (Top Level)

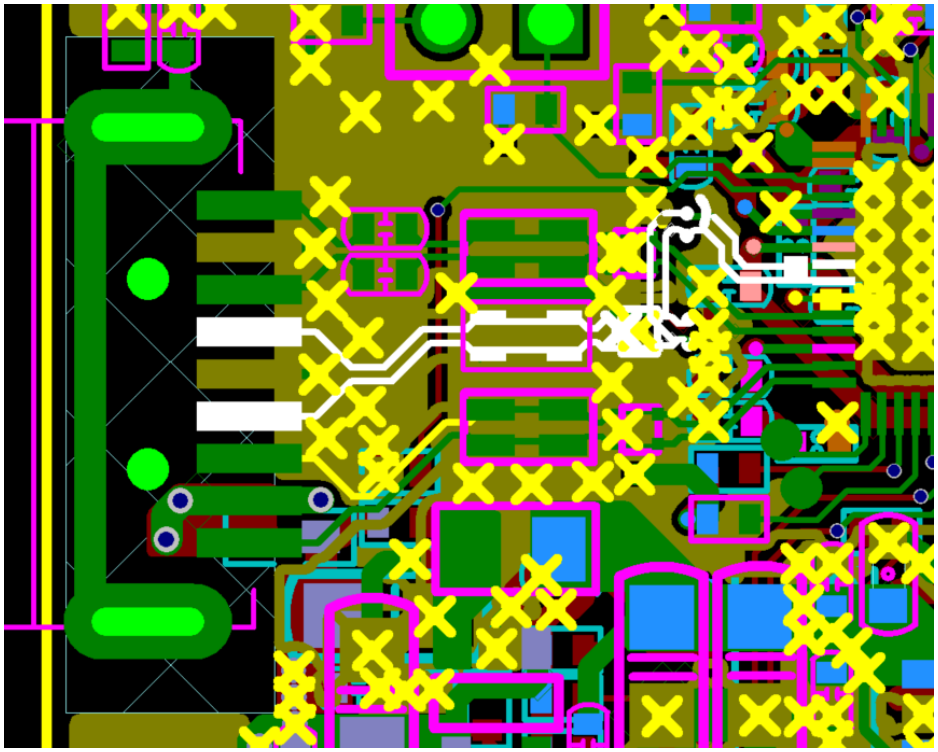


Figure 7. USB 2.0 D+/D- Traces Routing (Bottom Level)

9. Ethernet Magnetics Layout Considerations

This section describes some general 2.5G Ethernet layout considerations for the differential signals of the 2.5G Ethernet controller/PHY, the 2.5G Ethernet magnetics and the RJ-45 connector.

All trace routes from the 2.5G Ethernet controller/PHY, 2.5G Ethernet magnetics, RJ-45 connector should be as short as possible. It is an appropriate policy to have the same length for all differential pair signal traces. General speaking, reducing signal crosstalk, providing a solid ground plane, and decreasing parallel route should be considered.

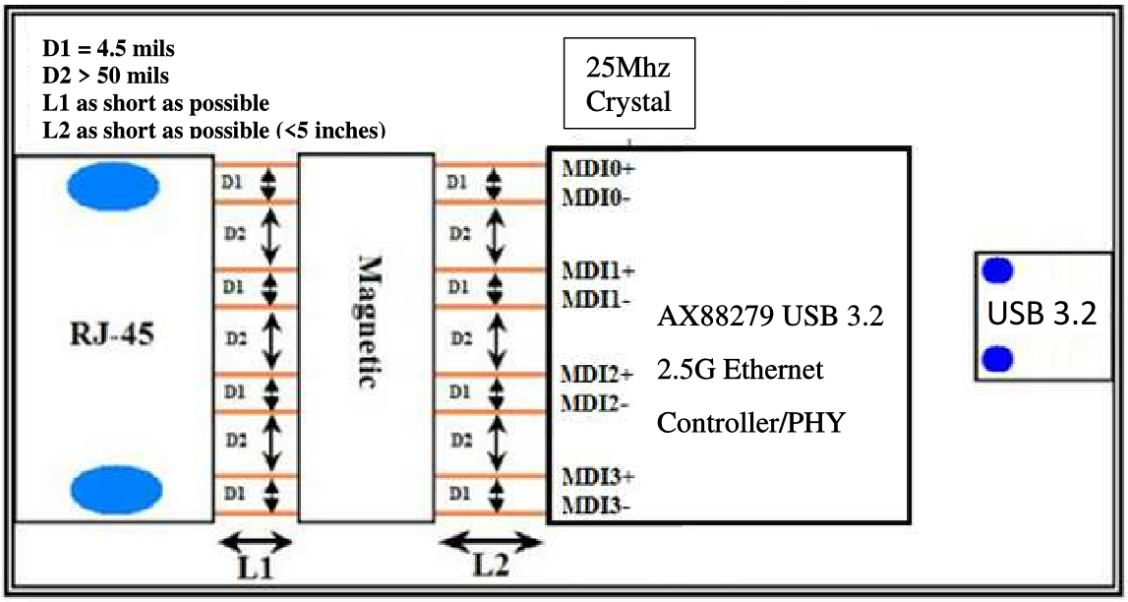
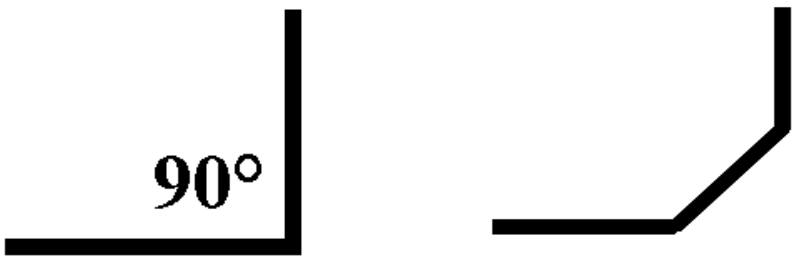


Figure 8. 2.5G Ethernet MDI0±, MDI1±, MDI2±, and MDI3± Differential Pairs Layout

1. The ideal Ethernet differential impedance between the "MDI0+ & MDI0-", "MDI1+ & MDI1-", "MDI2+ & MDI2-" and "MDI3+ & MDI3-" traces should be 100 Ohm. The Ethernet differential impedance between the MDI0+ (or MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-) trace and GND should be 50 Ohm respectively. The designer can use the trace width of MDI0+/MDI0-/MDI1+/MDI1-/MDI2+/ MDI2-/MDI3+/MDI3- traces to fine tune the Ethernet differential impedance value (a wider trace has a smaller impedance value). If the PCB manufacturer provides TDR measurement, it helps control the PCB Impedance
2. The crystal/oscillator clock source and the switching noises from digital signals should be kept away from the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs. Moreover, the crystal/oscillator may be sensitive to wander capacitances and noise from other signals; it is better to deploy the crystal far away from I/O ports, high frequency signal traces, magnetics, board edges, and so on.

3. The Ethernet magnetics should be placed as close to the RJ-45 connector as possible.
4. The 2.5G Ethernet PHY should be placed as close as possible to the magnetics. If there are some limitations on the PCB layout, the trace length from the 2.5G Ethernet PHY to the magnetics should not be longer than 5 inches. The designer should double check it by running full network functionality testing.
5. The MDI0±, MDI1±, MDI2±, and MDI3± differential pairs should be routed as close as possible. The trace spacing D1 between "MDI0+ & MDI0-", "MDI1+ & MDI1-", "MDI2+ & MDI2-" and "MDI3+ & MDI3-" pairs should be in 4.5 mils. The trace width minimum is 5 mils and should be adjusted accordingly to yield the required trace impedance.
6. Keep the trace length difference between MDI0+ and MDI0- (or between MDI1+ and MDI1-, MDI2+ and MDI2-, MDI3+ and MDI3-) pair within 200 mils.
7. The spacing D2 should be larger than 50 mils. If the PCB layout is really difficult to meet this requirement, the D2 spacing should be as larger as possible.
8. Route the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs as straight as possible and keep them in parallel for differential pairs.
9. Route the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs running symmetric, equal length and close whenever possible.
10. Different Ethernet differential pairs should be isolated by proper wide ground traces and keep 5 mils spacing.
11. Avoid using vias on the traces of the MDI0±, MDI1±, MDI2±, and MDI3± differential pairs. If the PCB layout really needs to use vias on the differential pairs, please match the vias to keep the differential pairs balanced.
12. The power plane and digital ground plane should not be placed under the magnetics and RJ-45 connector.
13. Avoid routing the signal trace with right angle, instead, the signal trace should be routed with multiple 135° angles.



Worst Better

10. QFN Package PCB Layout Considerations

This section describes some PCB layout considerations for QFN (**Q**uad **F**lat **N**o leads) package.

The QFN package is designed to provide superior thermal performance through an exposed thermal pad (E-pad) on the bottom surface of the package. This provides an extremely low thermal resistance path between the die and the exterior of the package. This package can be easily mounted using standard PCB assembly techniques and can be removed and replaced using standard repair procedures.

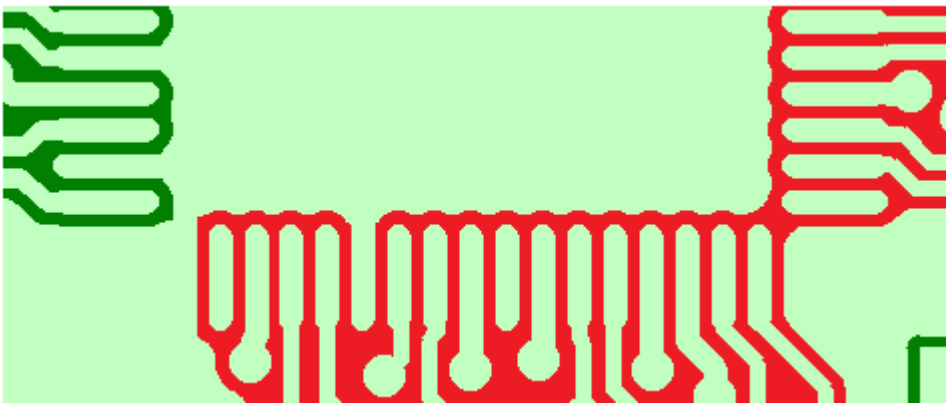
10-1 Solder Masking Design Considerations

The pads on PCB are either Solder Mask Defined (SMD) or Non-Solder Mask Defined (NSMD).

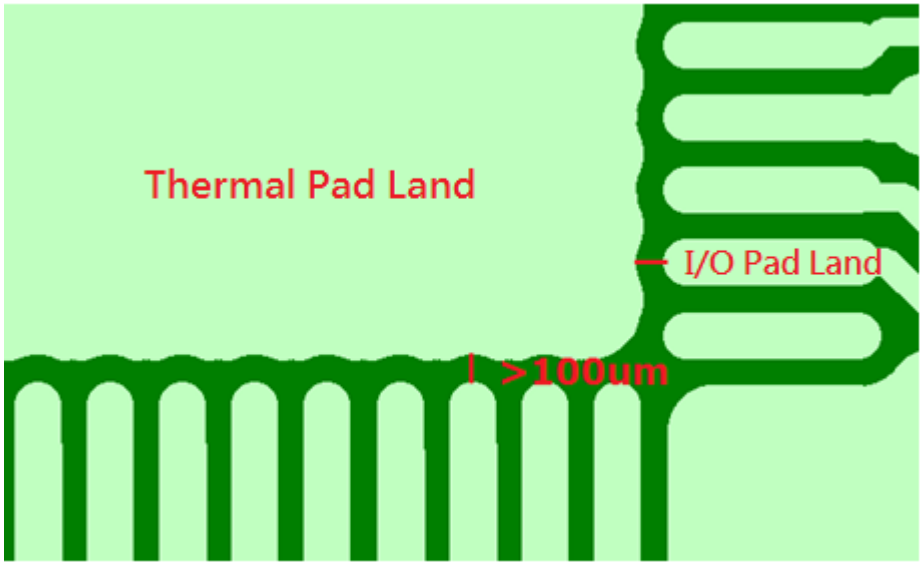
1. Solder Mask Defined (SMD): Solder mask openings smaller than the metal pads.
2. Non-Solder Mask Defined (NSMD): Solder mask openings larger than the metal pads.

The SMD pads are recommended for the single-row QFN package with a center thermal pad such as AX88279 QFN package. The NSMD pads are recommended for multi-row QFN package since the copper etching process has tighter control than the solder masking process and improves the reliability of solder joints.

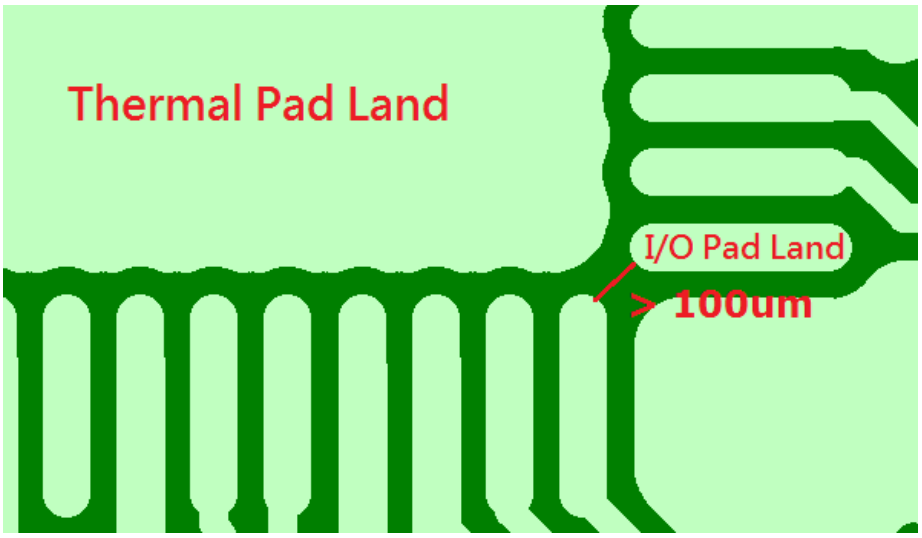
Typically, each land pad on PCB should have its own solder mask opening with a web between the adjacent pads. However, for a 0.4mm pitch width part with 0.23mm I/O land pad width, the PCB space may not be available for a proper solder mask web between the adjacent pads. In practice, designers can use one big solder mask opening for all the pads on one side of the QFN package as below red color areas.



For QFN package design, the exposed thermal pad size might be near the maximum available size for that package so the gap between the thermal pad land and I/O pads land may be small. Please keep the gap between the thermal pad land and I/O pads land to be larger than 100µm on all four sides to increase the solder mask web between the thermal pad and I/O pads lands.



Please keep the solder mask opening gap between the two adjacent I/O pad lands at four corners of the QFN package to be larger than 100µm.



10-2 Stencil Design Considerations

To avoid possible excessive solder paste to overflow to the pins, you can consider implementing the thermal pad land through cross-hatching Stencil opening lands.

The recommended wide and height of each Stencil opening land is 1.8 ~ 2.0 mm, and the recommended spacing between two Stencil opening lands is 0.3 mm.

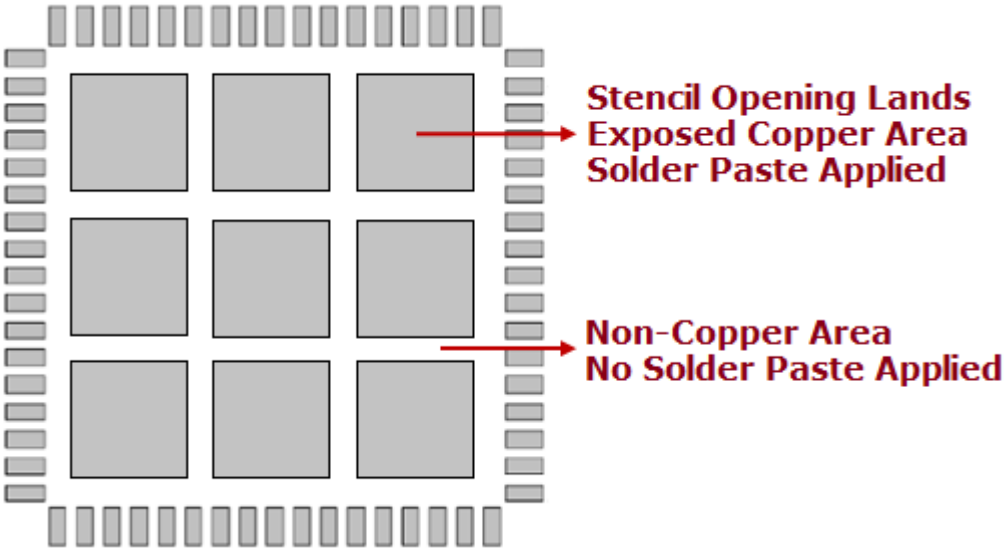


Figure 9. Thermal Pad Cross-Hatching Stencil Opening Lands

10-3 Thermal Vias Design Considerations

The thermal vias are designed to effectively transfer the heat from the E-pad of QFN package IC die to the top copper layer of the PCB to the inner or bottom copper layers to provide superior thermal dissipation performance.

The recommended thermal via diameter is 0.3 mm or less, and the recommended spacing between two adjacent thermal vias is 1.0 ~ 1.2 mm.

The thermal vias should be well connected to the internal ground plane through an exposed copper ring around each thermal via. The exposed copper ring is not required on the exposed thermal pad land since the copper of the thermal pad land is already exposed.

In practice, designers might need to adjust the thermal vias location to meet the possible PCB layout requirements such as good power planes layout considerations.

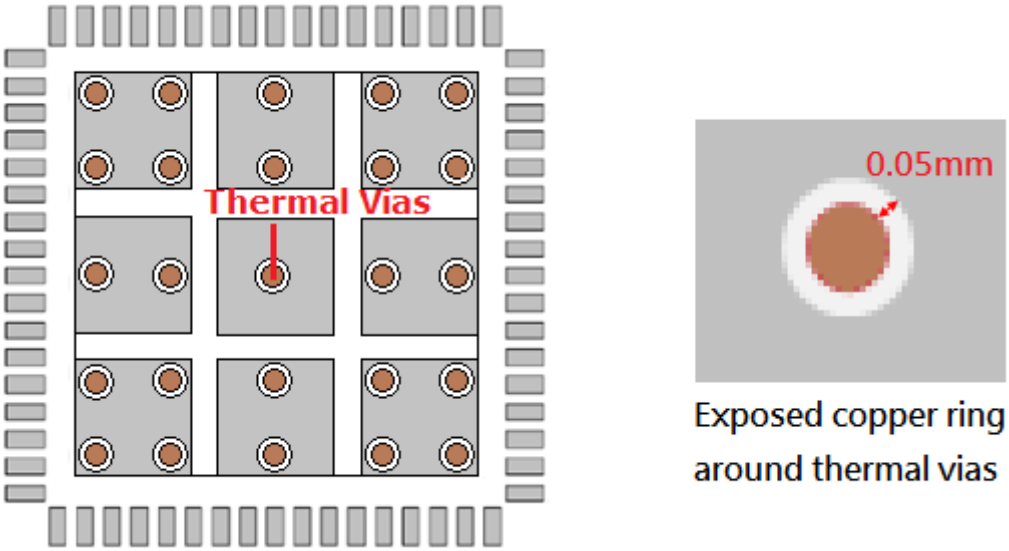


Figure 10. Thermal Vias and Exposed Copper Ring

10-4 Copper Area Design Considerations

The top/inner/bottom copper areas of PCB board act as heat sinks for the QFN package PCB layout design. The top copper areas should be covered with solder mask leaving only the solder mask defined thermal pad exposed. The top copper areas should be made as large as possible.

The inner and bottom layer copper planes can be connected to the exposed thermal pad through thermal vias and should be made as large as possible. The thermal pad is usually tied to the ground copper planes of PCB board so designers might need to double check the electrical correctness when connecting the copper planes to the thermal pad.

11. Thermal Considerations

This section describes some information about how to reduce the operating temperature on the USB 3.2 Gen1 to 2.5G Ethernet applications.

11-1 Improve the Cooling Plane

There are some major heat sources on the AX88279 USB 3.2 Gen1 to 2.5G Ethernet applications included AX88279 and external voltage regulators.

You can connect the AX88279 VCC/GND pins and the GNDK E-pad pin with wide traces to the respective power/ground planes to increase the cooling effect and reduce AX88279 operating temperatures.

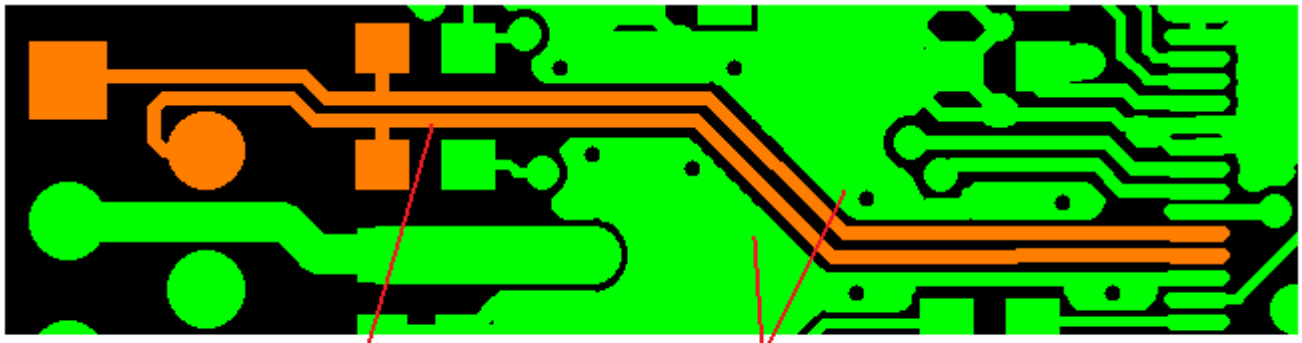
You can also add cooling planes on the external voltage regulators to reduce the operating temperature of the external voltage regulators.

11-2 Improve the Air Convection

If AX88279 is implemented on embedded system, you can place AX88279 at the location with good air convection and stay away from the high-operating-temperature IC such as voltage regulators or MCU to reduce AX88279 operating temperature.

12. EMI Considerations

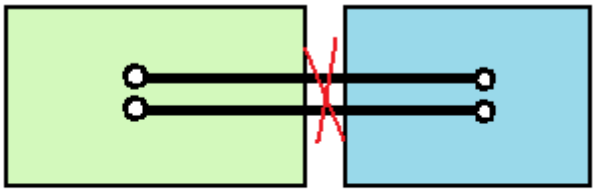
1. The high frequency signals traces such as Ethernet differential signals, clock signals, etc. shall be surrounded by GND to prevent interference to other signal wires. Better EMI effect can be attained by a one-piece GND underneath the IC furnished with PTH holes to enlarge the GND area.



2. The chosen connector must be shielded so that EMI integrity of the design is not compromised. The shield must be electrically connected to chassis ground to extend the chassis barrier for high frequency emissions. If an unshielded connector were used, the EMI would pass through the nylon material of the connector. The shield will also prevent less external EMI from entering the chassis.

3. To reduce electromagnetic emissions and susceptibility, it is imperative that traces from the transceiver to the magnetics sand from the magnetics to the RJ-45 be routed as differential pairs. The objective is to close the loop area formed by the two conductors. The radiated field from the loop or the voltage picked up by the loop by external fields is governed by the field strength and the area formed by the two conductors. Reasonable board design uses 5~10 mils trace widths separated by 10 mils. Transmit differential pairs should be routed adjacent to a power plane.

4. DON'T CROSS ANY SIGNAL TRACES OVER ANY REFERENCE PLANE CUTS. This might cause some unpredictable EMI problems.



5. Designer can consider implementing the choke components on the 2.5G differential signals traces to avoid the possible EMI issues if necessary.

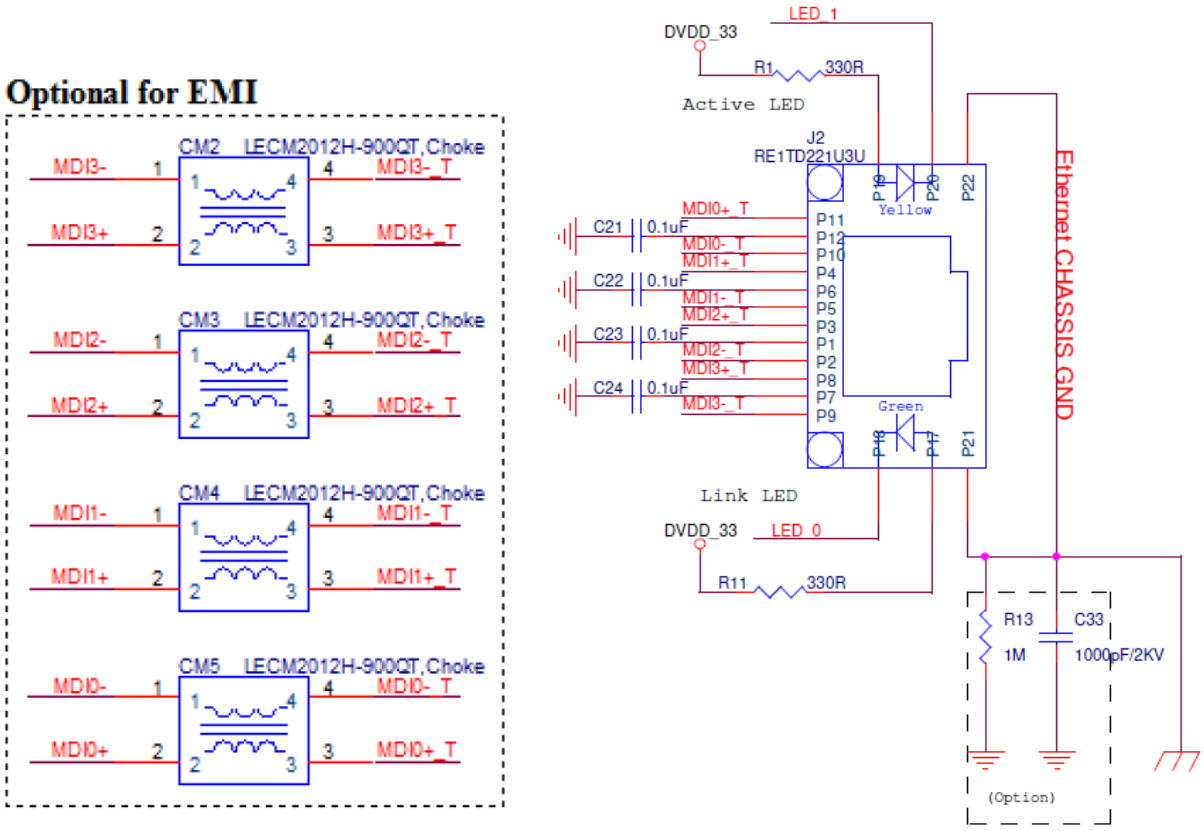


Figure 11. EMI Consideration Reference Circuit (Optional)

13. ESD Considerations

This section describes some information about the ESD design guideline. Users can refer to the following circuit to avoid the ESD issue.

It is necessary to install 1M Ohm and 1000pF capacitor (2KV or 3KV) to isolate the chassis ground and digital ground as below figure and give the gap with a proper distance (at least 80 mils) for better ESD protection. If possible, directly connect the RJ-45 Connector with fully shielded and choose a RJ-45 Connector that provides a low impedance path to ground for improved noise immunity performance.

Note: The following figure is just an example of the magnetics circuit for the ESD considerations. Please refer to AX88279 reference schematic for the detailed Ethernet magnetics circuit and refer to the preferred TVS diode part reference circuit to implement the ESD protection circuit.

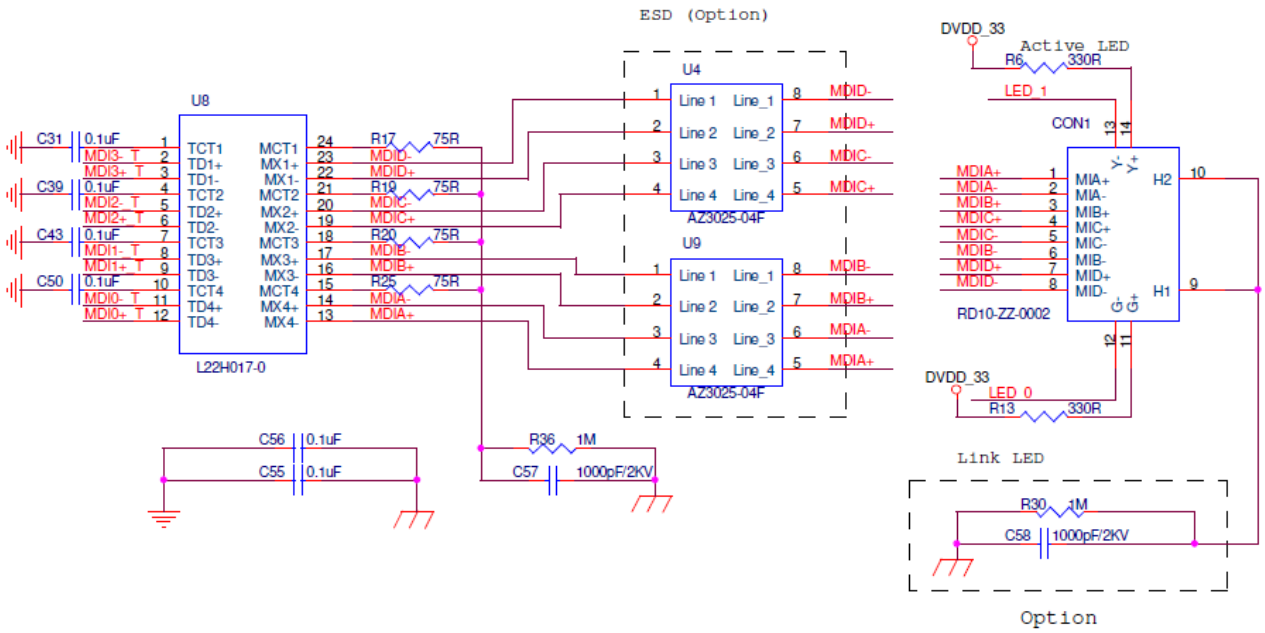


Figure 12. Ethernet ESD Considerations Reference Circuit

The fatal discharge may generate from a charged Ethernet cable, or out from outside devices such as PoE, or a human body, etc. Ethernet ICs become vulnerable to damage from Electrostatic Discharge (ESD) within those unpredictable factors. Protecting Ethernet interfaces from cable discharges can create a challenge for board designers. Be sure a good protective circuit must effectively fasten a transient to a safe voltage, and must present an acceptable capacitive load on high-speed differential transmission lines as well.

Below are a sample circuit for ESD protection. Please refer to the ESD Protection Diode datasheet for detailed ESD protection circuit.

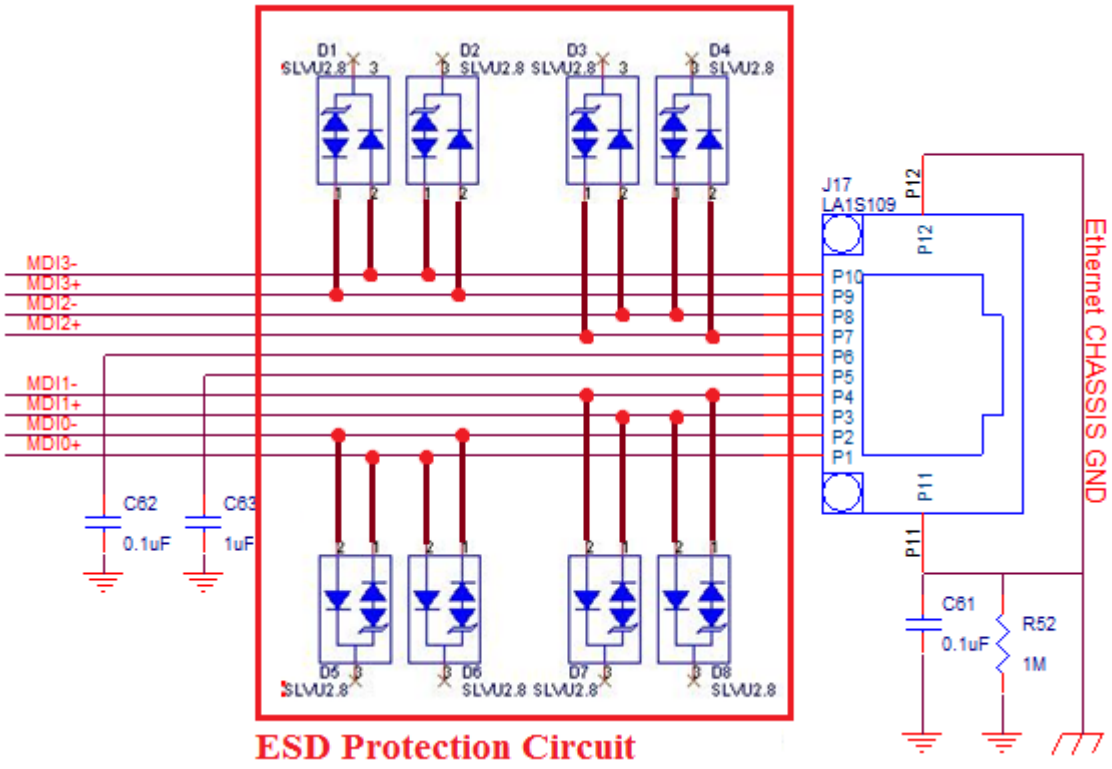


Figure 13. A Sample ESD Protection Circuit for Single RJ-45 with Integrated Magnetics (Optional)

14. AX88279 with USB HUB Design Considerations

If your application is connected to next layer of USB hub, the AX88279 VBUS pin will be controlled by the Power Enable signal of USB hub for judging USB Host is attach or detach, the AX88279 VBUS pin should be at low if AX88279 device is detach.

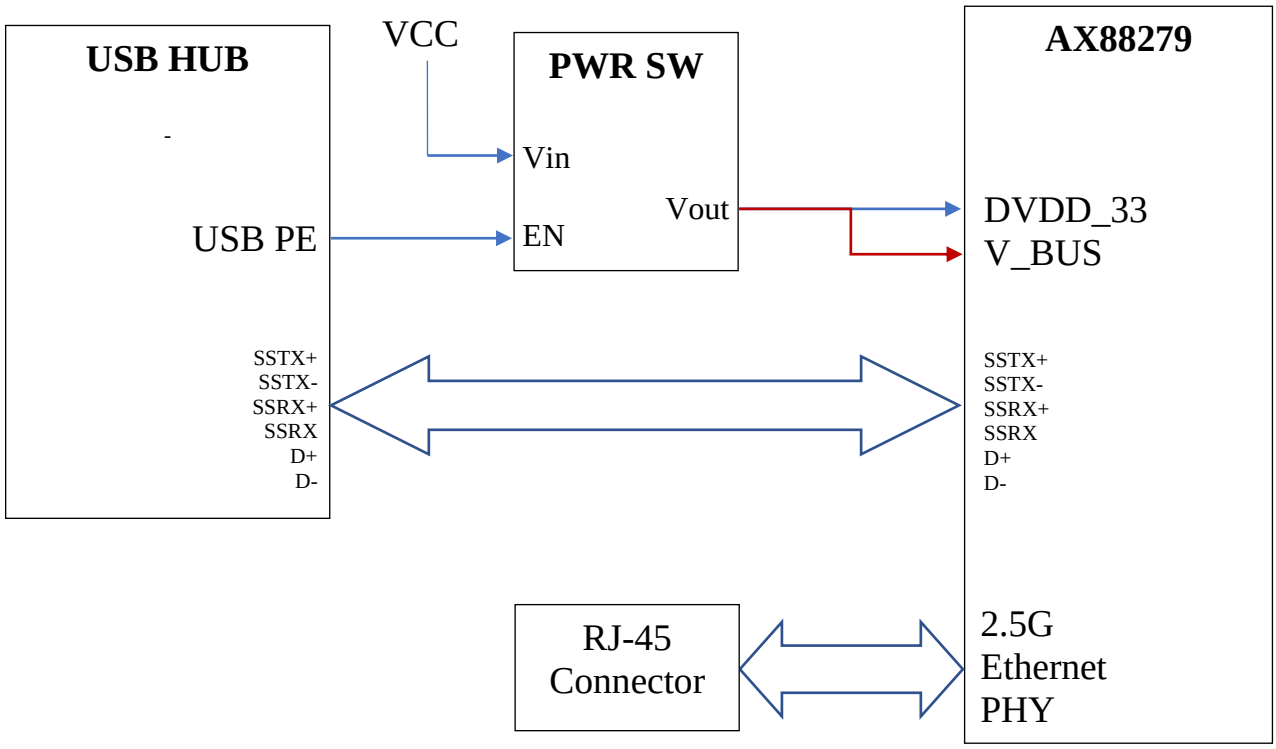


Figure 14. AX88279 with USB HUB Reference Block Diagram

ASIX Electronics Corporation

4F, No.8, Hsin Ann RD., Hsinchu Science Park,
Hsinchu, Taiwan, R.O.C.

TEL: +886-3-5799500
FAX: +886-3-5799558

Email: support@asix.com.tw
Web: https://www.asix.com.tw