Features

Document No: AX88279/V1.00/08/15/23

- **Single chip USB 3.2 Gen 1 to 2.5G Ethernet Controller with Integrated 100M/1G/2.5G Ethernet PHY**
- **USB Device Controller**
  - Integrates on-chip USB Type-C 3.2 Gen1 PHY and controller compliant to USB Spec 3.2 Gen 1, 2.0 and 1.1
  - Supports all USB 3.2 Gen 1 power saving modes (U0, U1, U2, and U3)
  - Supports USB Super/High/Full Speed modes with Bus-power or Self-power device
- **2.5G Ethernet Controller**
  - Integrates 100M/1G/2.5G Ethernet MAC/PHY, compliant to IEEE 802.3, 802.3u, 802.3ab and 802.3bz
  - Supports CDC-NCM, CDC-ECM
  - Supports IEEE 802.3az (Energy Efficient Ethernet, EEE)
  - Supports AUTO-MDIX, flow control (IEEE 802.3 Annex.31B)
  - Supports IPv4/IPv6 Packet Checksum Offload Engine (COE)
  - Supports TCP Large Send Offload V1/V2
  - Supports up to 9K Jumbo Frame
  - Supports IEEE 802.1Q VLAN tagging and 4096 VLAN ID filtering; received VLAN tag (4 bytes) can be stripped off or preserved
  - Supports IEEE 802.1P Layer 2 Priority Encoding and Decoding
  - Supports manageability L2 filter
  - Supports TCO filter, L3/L4 IP/Port filter
  - Supports Second DA RX filter with bit mask
- **Precision Time Protocol (PTP)**
  - Supports IEEE 1588v2 and 802.1AS
  - Supports Ordinary and Boundary clock
  - Supports 1-step and 2-step Clock Synchronization
  - Supports IEEE802.3, UDP/IPv4, and UDP/IPv6 Protocol Encapsulations
- **Wake-on-LAN Functions**
  - Supports suspend mode and remote wakeup via link-change, Magic Packet, Microsoft wakeup frame and external wakeup pin
  - Supports Bonjour Wake-on-Demand
  - Supports Wakeup Packet Indication
  - Supports Microsoft Modern Standby
- **Advanced Power Management Features**
  - Supports power management offload (ARP & NS)
  - Supports ECMA-393 ProxZzzy® for sleeping hosts
- **Supports Windows 11/10/8.x, Linux/Android /Chrome OS, Nintendo Switch in-box drivers, and macOS/Linux native CDC-NCM driver for driverless, Plug & Play**
- **Supports embedded eFuse for die identifier and customized USB ID and Ethernet MAC address**
- **Supports SPI Flash for firmware customization**
- **Single 25 MHz crystal clock source**
- **Integrates on-chip power-on reset circuit**
- **60-pin QFN, 7x7 mm package**
- **Operating Temperature Range: 0 to +70°C**

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Target Applications

- Notebook/Laptop Onboard LAN
- USB Ethernet Dongle for Ultrabook /Table/Smart Phone/etc.
- Docking Station, POS/PDA Cradle
- IP STB, Smart Camera, Smart TV Box
- Game Console
- 5G/LTE Router/Gateway

Typical Applications Diagram

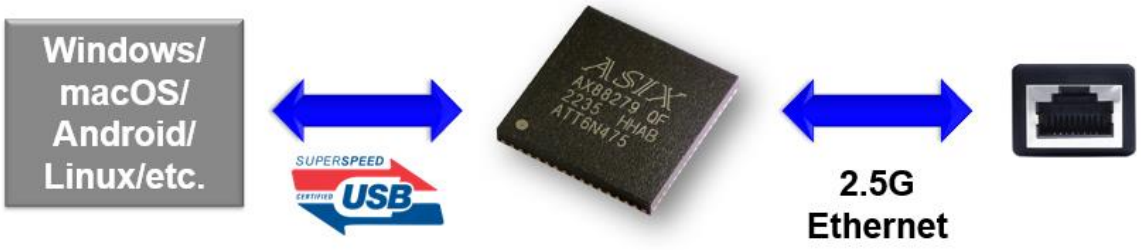

Figure 0-1: AX88279 Typical Applications Diagram

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1 Introduction

1.1 General Description

The AX88279 USB 3.2 Gen1 to 100M/1G/2.5Gigabit Ethernet controller is a high performance and highly integrated ASIC which enables low cost, small form factor, and simple plug-and-play 2.5Gigabit Ethernet network connection capability for desktops, notebook PC's, Ultrabook's, docking stations, game consoles, digital-home appliances, and any embedded system using a standard USB port.

The AX88279 features a USB interface to communicate with a USB Host Controller and is compliant with USB specification V3.2 Gen1, V2.0, and V1.1. It implements a 100M/1G/2.5Gigabit Ethernet LAN function based on IEEE802.3, IEEE802.3u, IEEE802.3ab and IEEE802.3bz standards with embedded SRAMs for packet buffering. And, it also integrates an on-chip 100M/1G/2.5Gigabit EEE-compliant Ethernet PHY to simplify system design.

1.2 Block Diagram

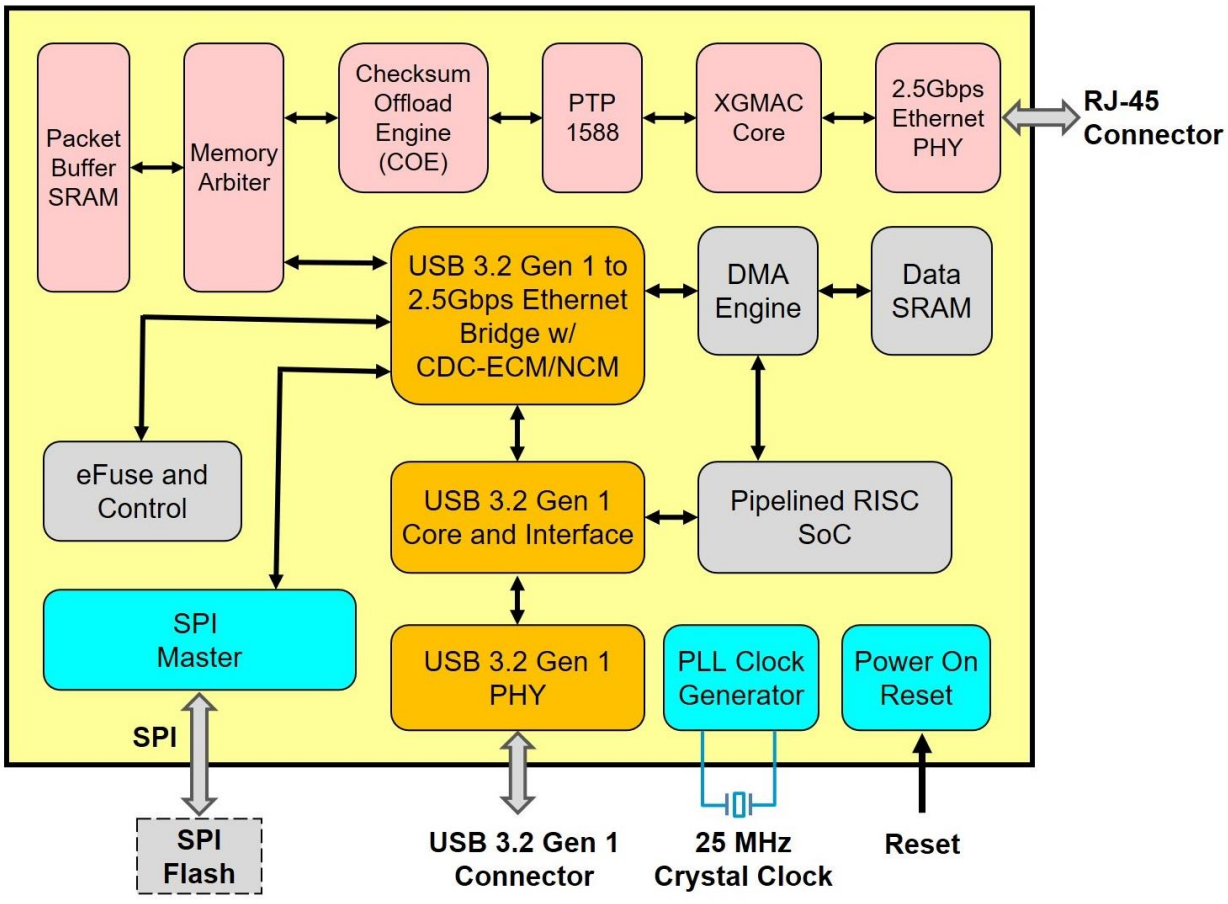


Figure 1-1: AX88279 Block Diagram

1.3 Pinout Diagram

AX88279 is housed in a 60-pin E-PAD QFN package.

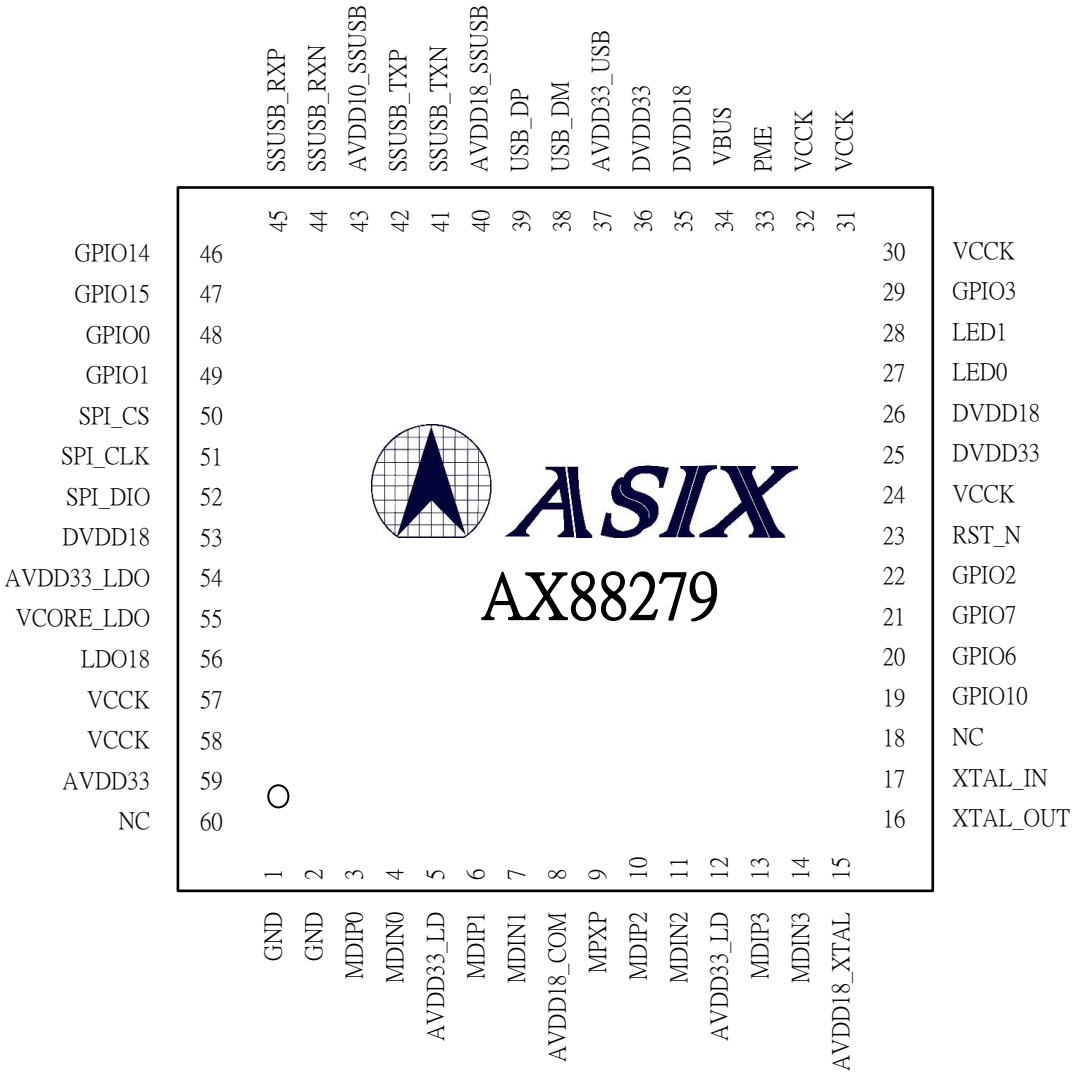


Figure 1-2: AX88279 Pinout Diagram

1.4 Signal Description

Following abbreviations are used in "Type" column of below pin description tables. Note that some I/O pins with multiple signal definitions on the same pin may have different attributes in "Type" column for different signal definition.

AB Analog Bi-directional I/O
AI Analog Input
AO Analog Output
I18 Input, 1.85V
O18 Output, 1.85V
B3 Bi-directional I/O, 3.3V
I3 Input, 3.3V
O3 Output, 3.3V
PU Internal Pull-Up (75K)
PD Internal Pull-Down (75K)
P Power/Ground pin
S Schmitt Trigger
T Tri-state
4m 4mA driving strength
8m 8mA driving strength

1.4.1 USB Interface

Pin Name	Type	Pin No	Pin Description
USB_DP	AB	39	USB 2.0 data differential pair positive pin.
USB_DM	AB	38	USB 2.0 data differential pair negative pin.
SSUSB_TXN	AO	41	USB 3.2 Gen 1 TX- differential pair.
SSUSB_TXP	AO	42	USB 3.2 Gen 1 TX+ differential pair.
SSUSB_RXN	AI	44	USB 3.2 Gen 1 RX- differential pair.
SSUSB_RXP	AI	45	USB 3.2 Gen 1 RX+ differential pair.

Table 1-1: USB Interface Pin Description

1.4.2 Clock

Pin Name	Type	Pin No	Pin Description
XTAL_IN	I18	17	25Mhz crystal or oscillator clock input.
XTAL_OUT	O18	16	25Mhz crystal clock output.

Table 1-2: Clock Pin Description

1.4.3 GPHY MDI

Pin Name	Type	Pin No	Pin Description
MDIP0	AB	3	MDI pair 0 positive pin
MDIN0	AB	4	MDI pair 0 negative pin
MDIP1	AB	6	MDI pair 1 positive pin
MDIN1	AB	7	MDI pair 1 negative pin
MDIP2	AB	10	MDI pair 2 positive pin
MDIN2	AB	11	MDI pair 2 negative pin
MDIP3	AB	13	MDI pair 3 positive pin
MDIN3	AB	14	MDI pair 3 negative pin

Table 1-3: 2.5G PHY MDI Pin Description

1.4.4 Misc. Pin

Pin Name	Type	Pin No	Pin Description
MPXP	AB	9	External Reference Resistor (24 KΩ, 1%) Connect resistor to Analog GND.
VBUS	I3/S	34	VBUS signal of USB. (GPIO9)
RST_N	I3/S/PU	23	Reset signal. Active low
SPI_CS	B3/S	50	SPI Chip Select pin for external SPI flash
SPI_CLK	B3/S	51	SPI Clock pin for external SPI flash
SPI_DIO	B3/S	52	SPI Digital I/O pin for external SPI flash
PME*	B3/S/PU	33	PME pin for power management, always pull up this pin. (GPIO8)
GPIO0	B3/S	48	General Purpose I/O 0
GPIO1	B3/S	49	General Purpose I/O 1
GPIO2	B3/S	22	General Purpose I/O 2
GPIO3**	B3/S	29	General Purpose I/O 3 This pin needs to be pulled up with an external resister to DVDD33
GPIO6	B3/S	20	General Purpose I/O 6
GPIO7	B3/S	21	General Purpose I/O 7
GPIO10	B3/S	19	General Purpose I/O 10. This pin needs to be pulled up with an external resister to DVDD33.
GPIO14	B3/S	46	General Purpose I/O 14
GPIO15	B3/S	47	General Purpose I/O 15
LED0	B3	27	Programmable LED0 indication (GPIO5)
LED1	B3	28	Programmable LED1 indication (GPIO4)
NC	B3	18, 60	No Connection Pin (Keep floating on the PCB)

*: The default is an external wakeup pin. Active low. PME or USB3.0 LED pin needs to set by tool.
**: It can be set LED2 indication by tool.

Table 1-4: Misc. Pin Description

1.4.5 Power and Ground Pin

Pin Name	Type	Pin No	Pin Description
AVDD33_USB	P	37	3.3V Analog Power Input of USB.
AVDD18_SSUSB	P	40	1.85V Analog Power Input of SS USB.
AVDD10_SSUSB	P	43	1.0V Analog Power Input of SS USB.
DVDD33	P	25, 36	3.3V I/O Power.
DVDD18	P	26, 35, 53	1.85V I/O Power.
VCCK	P	24, 30, 31, 32, 57, 58	1.0V Digital Core Power.
AVDD33	P	59	3.3V Analog Power.
GND	P	1, 2	Ground for all Analog and Digital Power.
AVDD33_LDO	P	54	3.3V Analog Power for LDO.
LDO18	P	56	1.85V Power Output from LDO.
VCORE_LDO	P	55	1.0V Power Output from LDO.
AVDD18_XTAL	P	15	1.85V Analog Power for crystal pad.
AVDD33_LD	P	5, 12	3.3V Analog Power for Ethernet PHY.
AVDD18_COM	P	8	1.85V Analog Power for Ethernet PHY.
EPAD	P	--	Ground for all Analog and Digital Power.

Table 1-5: Power and Ground Pin Description

2 Function Description

2.1 Clocks/Resets

The AX88279 integrates internal oscillator circuits for 25 MHz (25MHz ± 50PPM at room temperature), respectively, which allow the chip to operate cost effectively with just one single external 25 MHz crystal.

The external 25 MHz crystal or oscillator, via pins XTAL_IN / XTAL_OUT, provides the reference clock to internal oscillation circuit to generate clock source for the embedded Ethernet PHY, embedded USB PHY, and base clock for ASIC use.

The AX88279 integrates an internal power-on-reset circuit, which can simplify the external reset circuitry on PCB design. The power-on-reset circuit generates a reset pulse to reset chip logic when power ramping up. The external hardware reset input pin, RST_N, is fed directly to the input of the power-on-reset circuit and can also be used as additional hardware reset source to reset the system logic. For more details on RST_N timing, please refer to the Reset timing section.

2.2 USB Core and Interfaces

The USB core and interfaces contains USB 3.2 Gen1/USB 2.0 transceiver interfaces (PIPE/UTMI) and USB 3.2 Gen1/USB 2.0 Device Controller.

The USB 3.2 Gen1/USB 2.0 transceiver (or PHY) processes USB 3.2 Gen1/2.0/1.1 Physical layer signals. And, The USB 3.2 Gen1/USB 2.0 Device Controller is interfacing with USB 3.2 Gen1/USB 2.0 transceiver by PIPE/UTMI buses and it processes packets of Link layer and protocol layer. Also, The USB 3.2 Gen1/USB 2.0 Device Controller contains Bulk IN and Bulk OUT buffers for handling Bulk transfer traffic and a FIFO for Interrupt IN transfers.

The USB core and interfaces are used to communicate with a USB host controller and is compliant with USB specification V3.2 Gen1, V2.0, and V1.1

2.3 100M/1G/2.5Gigabit Ethernet PHY

The 100M/1G/2.5Gigabit Ethernet PHY is compliant with 100Base-TX, 1000Base-T, and 2.5GBase-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT 5e UTP cable or CAT 6 UTP cable. It uses DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction (Auto-MDIX), polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented.

2.4 Energy Efficient Ethernet (EEE)

It supports IEEE 802.3az also known as Energy Efficient Ethernet (EEE). And also supports EEE specified a negotiation method to enable link partner to determine whether EEE is supported and to select the best set of parameters common to both devices. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled; however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

2.5 Checksum Offload Engine (COE)

The Checksum Offload Engine (COE) supports IPv4, IPv6, layer 4 (TCP, UDP, ICMP, ICMPv6 and IGMP) header processing functions and real time checksum calculation in hardware

The COE supports the following features in layer 3:

- IP header parsing, including IPv4 and IPv6
- IPv6 extension header and routing header type 0 supported
- IPv4 header checksum check and generation (There is no checksum field in IPv6 header)
- Detecting on RX direction for IP packets with error header checksum

The COE supports the following features in layer 4:

- TCP and UDP checksum check and generation for non-fragmented packet
- TCP Large Send Offload V2
- ICMP, ICMPv6 and IGMP message checksum check and generation for non-fragmented packet.

2.6 USB to Ethernet Bridge

The USB to Ethernet bridge block is responsible for converting Ethernet MAC frame into USB packets or vice-versa. This block supports proprietary burst transfer mechanism (US Patent Approval) to offload software burden and to offer very high packet transfer throughput over USB bus.

This USB to Ethernet bridge block not only co-work with “eFuse and Control”, “SPI Loader I/F”, and General Purpose I/Os and LEDs, but also handle USB Control transfers of Endpoint 0.

2.7 PTP

IEEE 1588(PTP) is used for a precision clock synchronization protocol to synchronize the clocks among network. The standard also defines a Precision Time Protocol (PTP) and generalized precision time protocol (gPTP) designed to synchronize real-time clocks in a distributed system, which can achieve synchronization accuracy. Such high accuracy is especially beneficial for control applications that need synchronized clocks for operation. This is only used for saving PTP information, modify timestamp field and modify correction field. The PTP need the software and driver (ptp4l in Linux system) which to run algorithm.

2.8 eFuse

The AX88279 integrated an eFuse which is allowed user to program USB descriptions (PID, VID, Serial numbers… ect) and some device information (MAC address). And ASIX advance data structures allow user to program this information for multiple times.

2.9 General Purpose I/O and LED

There are 3 general-purpose I/O pins for SPI flash and 2 LED pins for LED indication.

3 SPI/eFuse Memory

3.1 SPI/eFuse Memory

AX88279 supports integrated eFuse for MAC address, USB descriptor and several user specified information. It also supports external SPI flash for firmware image. These non-violated memory supports advance data architecture for multiple times programming.

4 USB Configuration Structure

4.1 USB Configuration

The AX88279 supports 2 USB Configuration, 1 for AX88279 proprietary driver, 1 for CDC-ECM/NCM.

4.2 USB Interface

The AX88279 supports 1 interface.

4.3 USB Endpoints

The AX88279 supports following 4 endpoints:

Endpoint 0: Control endpoint. It is used for configuring the device. Please refer to the USB Standard Commands and USB Vendor Commands sections.
Endpoint 1: Interrupt endpoint. It is used for reporting network Link status. Please refer to the Interrupt Endpoint section.
Endpoint 2: Bulk IN endpoint. It is used for receiving Ethernet Packet.
Endpoint 3: Bulk OUT endpoint. It is used for transmitting Ethernet Packet.

5 Electrical Specifications

5.1 DC Characteristics

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
DVDD33 AVDD33_USB AVDD33_BUCK AVDD33_LD	3.3V Supply Voltage	-0.3	3.63	V
DVDD18 AVDD18_SSUSB AVDD18_XTAL AVDD18_COM	1.85V Supply Voltage	-0.3	1.98	V
VCCK AVDD10_SSUSB	1.0V Supply Voltage	-0.3	1.1	V
|ΔxVDDx|	Variations between different the power pins of the same domain	--	0.3	V
Vin	Input Voltage of 3.3V IO Pins	-0.3	3.6	V

Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.
2. The input and output negative voltage ratings may be exceeded if the input and output currents under ratings are observed.

5.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
DVDD33 AVDD33_USB AVDD33_BUCK AVDD33_LD	3.3V Supply Voltage.	3.14	3.3	3.46	V
DVDD18 AVDD18_SSUSB AVDD18_XTAL AVDD18_COM	1.85V Supply Voltage.	1.76	1.85	1.89	V
VCCK AVDD10_SSUSB	1.0V Supply Voltage.	0.95	1.0	1.05	V
Tj	Operating junction temperature	0	25	125	℃
Ta	Operating ambient temperature	0	-	70	℃
T_{STG}	Storage temperature	-65	-	150	℃

5.1.3 Electrostatic Discharge and Latchup Performance

Symbol	Parameter	Conditions	Max	Units
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JEDEC JS-001-2017	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JEDEC JESD22-C101	500	V
LU	Static latchup class	T_A = +25 °C conforming to JEDEC EIA/JESD78 Trigger Current: 200mA Over Voltage: 1.5Vcc max	Pass	

5.1.4 DC Characteristics of 3.3V I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DVDD33	Power supply of 3.3V I/O.	3.3V I/O	3.14	3.3	3.46	V
Vil	Input low voltage.	LVTTL	-	-	0.8	V
Vih	Input high voltage.		2.0	-	-	V
Vt-	Schmitt trigger negative going threshold voltage.	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage.	Iol = 4 ~ 8mA	-	-	0.4	V
Voh	Output high voltage.	Ioh = 4 ~ 8mA	DVDD33 -0.4	-	-	V
Vopu (1)	Output pull-up voltage for 5V tolerant IO	With internal pull-up resistor	DVDD33 – 0.9	-	-	V
Rpu	Input pull-up resistance.		40	75	190	KΩ
Rpd	Input pull-down resistance.		40	75	190	KΩ
Iin	Input leakage current.	Vin = 3.3 or 0V	-	±6	-	μA
	Input leakage current with pull-up resistance.	Vin = 0 V	-	-45	-	μA
	Input leakage current with pull-down resistance.	Vin = DVDD33	-	45	-	μA

Note: This parameter indicates that the pull-up resistor for the I/O pins cannot reach DVDD33 DC level even without DC loading current.

5.2 Power Consumption

Symbol	Description	Conditions	Typ	Unit
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 2.5Gbps full duplex mode and USB Super Speed mode	710	mA
I_{VDD18}	Current Consumption of 1.85V		96.5	mA
I_{VDD33}	Current Consumption of 3.3V		201.6	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 1Gbps full duplex mode and USB Super Speed mode	66	mA
I_{VDD18}	Current Consumption of 1.85V		86.75	mA
I_{VDD33}	Current Consumption of 3.3V		198.3	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 100Mbps full duplex mode and USB Super Speed mode	40.5	mA
I_{VDD18}	Current Consumption of 1.85V		86.7	mA
I_{VDD33}	Current Consumption of 3.3V		181.5	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 100Mbps half duplex mode and USB Super Speed mode	40.3	mA
I_{VDD18}	Current Consumption of 1.85V		86.7	mA
I_{VDD33}	Current Consumption of 3.3V		181.4	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 2.5Gbps full duplex mode and USB High Speed mode	697.5	mA
I_{VDD18}	Current Consumption of 1.85V		90.5	mA
I_{VDD33}	Current Consumption of 3.3V		166.5	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 1Gbps full duplex mode and USB High Speed mode	58.5	mA
I_{VDD18}	Current Consumption of 1.85V		86.3	mA
I_{VDD33}	Current Consumption of 3.3V		150.35	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 100Mbps full duplex mode and USB High Speed mode	39.98	mA
I_{VDD18}	Current Consumption of 1.85V		73.7	mA
I_{VDD33}	Current Consumption of 3.3V		133.8	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 100Mbps half duplex mode and USB High Speed mode	39.83	mA
I_{VDD18}	Current Consumption of 1.85V		73.7	mA
I_{VDD33}	Current Consumption of 3.3V		133.7	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 2.5Gbps full duplex mode and USB Full Speed mode	697.5	mA
I_{VDD18}	Current Consumption of 1.85V		78.5	mA
I_{VDD33}	Current Consumption of 3.3V		155.1	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 1Gbps full duplex mode and USB Full Speed mode	57.9	mA
I_{VDD18}	Current Consumption of 1.85V		69.43	mA
I_{VDD33}	Current Consumption of 3.3V		146.6	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 100Mbps full duplex mode and USB Full Speed mode	39.05	mA
I_{VDD18}	Current Consumption of 1.85V		69	mA
I_{VDD33}	Current Consumption of 3.3V		130.3	mA
I_{VDD10}	Current Consumption of 1.0V	Operating at Ethernet 100Mbps half duplex mode and USB Full Speed mode	39.5	mA
I_{VDD18}	Current Consumption of 1.85V		69	mA
I_{VDD33}	Current Consumption of 3.3V		129.5	mA
I_{VDD10}	Current Consumption of 1.0V	Ethernet Unlink and USB Super Speed mode	315	mA
I_{VDD18}	Current Consumption of 1.85V		90	mA
I_{VDD33}	Current Consumption of 3.3V		156	mA
I_{VDD10}	Current Consumption of 1.0V	USB Suspend and Ethernet is 2.5Gbps: enable Remote WakeUp and disable WOLLP (WOL Low Power)	700	mA
I_{VDD18}	Current Consumption of 1.85V		73.8	mA
I_{VDD33}	Current Consumption of 3.3V		142.5	mA
I_{VDD10}	Current Consumption of 1.0V	USB Suspend and Ethernet is 1Gbps: enable Remote WakeUp and disable WOLLP (WOL Low Power)	58.1	mA
I_{VDD18}	Current Consumption of 1.85V		64.9	mA
I_{VDD33}	Current Consumption of 3.3V		131.5	mA
I_{VDD10}	Current Consumption of 1.0V	USB Suspend and enable Remote WakeUp and enable WOLLP to 100Mbps	39.5	mA
I_{VDD18}	Current Consumption of 1.85V		65.1	mA
I_{VDD33}	Current Consumption of 3.3V		120	mA
I_{VDD10}	Current Consumption of 1.0V	Suspend and disable Remote WakeUp	0	mA
I_{VDD18}	Current Consumption of 1.85V		0.68	mA
I_{VDD33}	Current Consumption of 3.3V		1.9	mA
System				
I_{SYSTEM}	VBUS of 5.0V (Includes all regulators)	Operating at Ethernet 2.5Gbps full duplex mode and USB Super Speed mode with full loading	397	mA
		Operating at Ethernet 1Gbps full duplex mode and USB Super Speed mode with full loading	174.5	
		Operating at Ethernet 100Mbps full duplex mode and USB Super Speed mode with full loading	141	
$I_{SYSTEM\ (Suspend)}$	VBUS of 5.0V (Includes all regulators)	Power consumption of AX88279 Suspend and disabled Remote WakeUp.	1.93	mA

Note: Above current value are typical values measured on AX88279 EVB.

Table 5-1: AX88279 Power Consumption

Symbol	Description	Condition	Min	Typ	Max	Unit
Θ_{JC}	Thermal resistance of junction to case		-	12.42	-	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still Air	-	20.47	-	°C/W
Θ_{JB}	Thermal resistance of junction to board		-	3.79	-	°C/W
Ψ_{JT}	Junction to Top of the Package Characterization Parameter		-	1.51	-	°C/W

Note: Above parameters based on JEDEC51-7 system with 4 layers FR4 PCB size: 76x114.3mm.

Table 5-2: Thermal Characteristics

5.3 Power–up Sequence

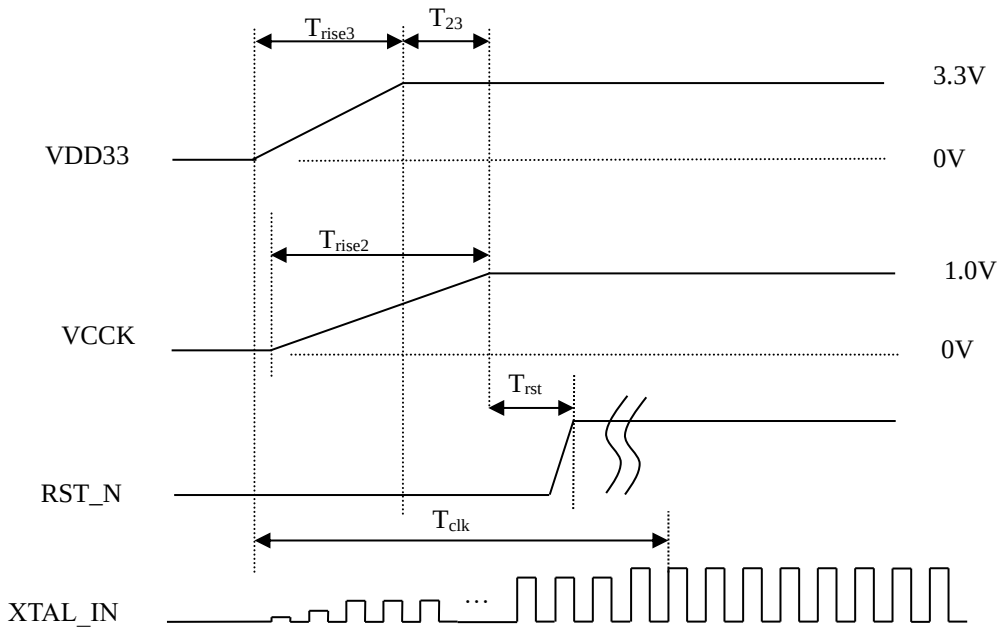


Figure 5-1: Power-up Sequence Timing Diagram

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{rise3}	3.3V power supply rise time.	From 0V to 3.3V.	-	800	-	us
T_{rise2}	VCCK (1.0V) power supply rise time.	From 0V to 1.0V.	-	5	-	ms
T_{23}	Interval between VDD33 and VCCK stable			4.2		ms
T_{rst}	RST_N asserted low level interval.	From VCCK rising to 1.0V to RST_N going high.	-	4	-	ms
T_{clk}	25MHz crystal oscillator start-up time.	From DVDD33 rising to 3.3V to clock stable of 25MHz crystal oscillator.	-	-	5	ms

Note: The above typical timing data is measured from AX88279 EVB.

Table 5-3: Power-up Sequence Timing Table

5.4 AC Timing Characteristics

5.4.1 SPI Timing

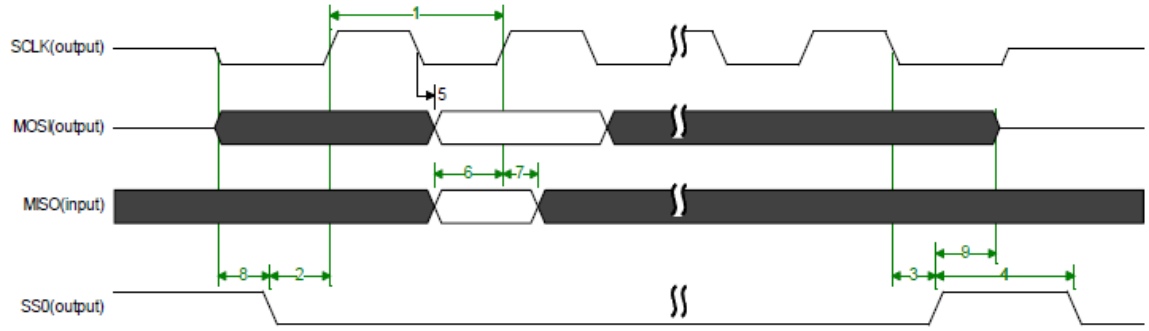


Figure 5-2: SPI Timing

Symbol	Parameter	Min	Typ	Max	Units
1	SCLK clock frequency	-	Fsys_clk (SPIBRR + 1) * 2		MHz
2	Setup time of SS to the first SCLK edge	-	0.5 * Tsclk	-	ns
3	Hold time of SS after the last SCLK edge	-	0.5 * Tsclk	-	ns
4	Minimum idle time between transfers (minimum SS high time)	-	((32 * SPIDT + 6) * Tsys_clk) + (0.5 * Tsclk)	-	ns
5	MOSI data valid time, after SCLK edge	-		1.53	ns
6	MISO data setup time before SCLK edge	5.98		-	ns
7	MISO data hold time after SCLK edge	0		-	ns
8, 9	Bus drive time before SS assertion and after SS de-assertion	-		0.5 * Tsclk	ns

Note 1: Fclk = 1/Tclk, where Tclk = ((SCL_HP + SCL_LP) * Tsys_clk).
Tsys_clk is 20MHz or 80MHz.

Table 5-4: SPI Timing Table

5.4.2 Clock Timing

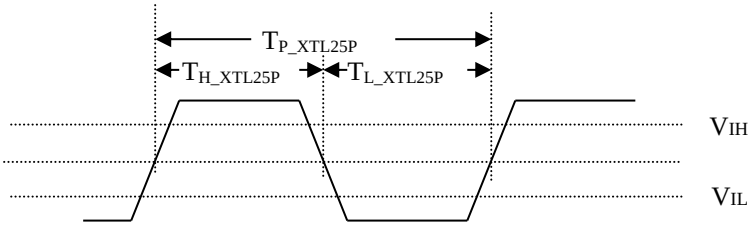
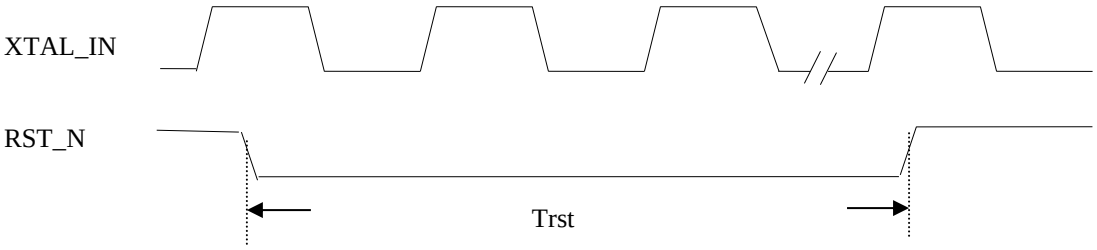


Figure 5-3: Clock Timing Diagram

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XTL25P}	XTAL clock cycle time		-	40.0	-	ns
T_{H_XTL25P}	XTAL clock high time		-	20.0	-	ns
T_{L_XTL25P}	XTAL clock low time		-	20.0	-	ns

Table 5-5: Clock Timing Table

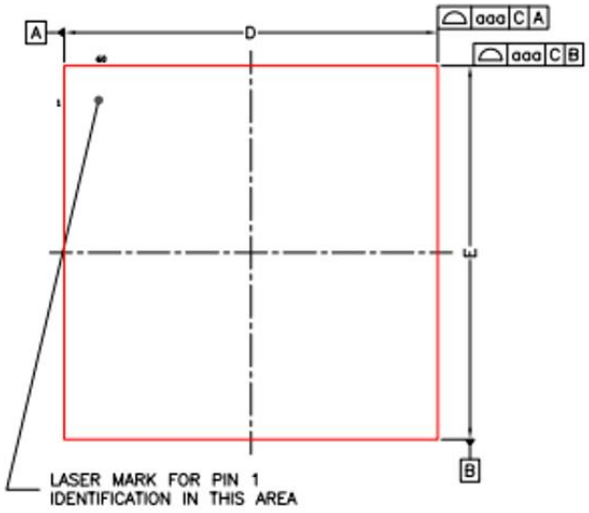
5.4.3 Reset Timing



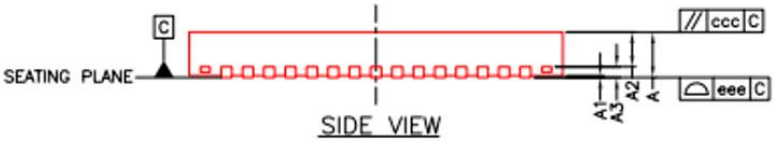
Symbol	Description	Min	Typ	Max	Unit
Trst	Reset pulse width after XTAL_IN is running	200	-	-	XTAL_IN clock cycle

Table 5-6: Reset Timing Table

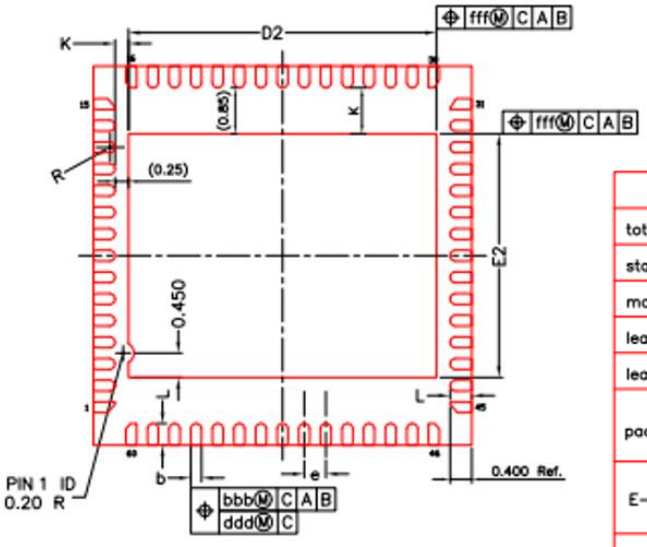
6 Package Information



TOP VIEW



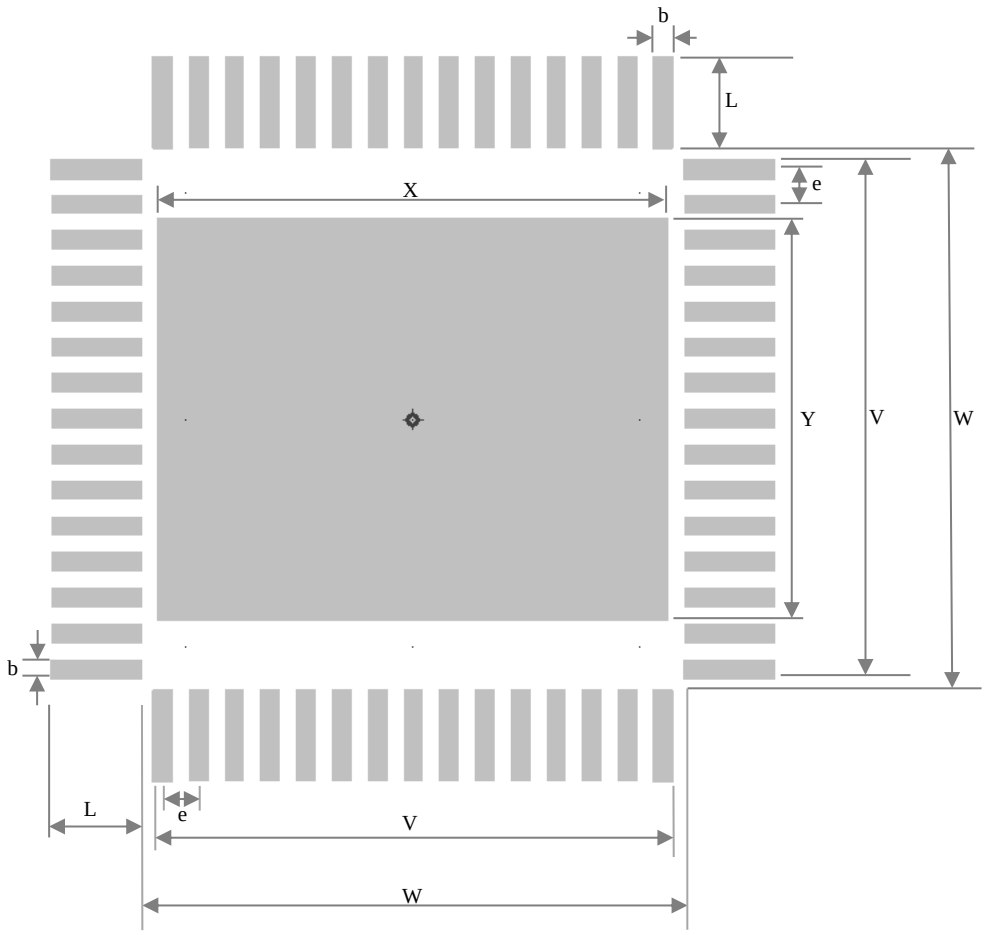
SIDE VIEW



BOTTOM VIEW

Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.80	0.85	0.90
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.60	0.65	0.70
leadframe thickness		A3		0.20 REF.	
lead width		b	0.15	0.20	0.25
package size	X	D	6.90	7.00	7.10
	Y	E	6.90	7.00	7.10
E-PAD size	X	D2	5.60	5.70	5.80
	Y	E2	4.40	4.50	4.60
lead length		L	0.30	0.40	0.50
lead pitch		e		0.40 bsc	
lead arc		R	0.075	---	---
Lead to E-PAD tolerance		K	0.20	---	---
Package profile of a surface		aaa		0.10	
Lead position		bbb		0.07	
Paralleliam		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

Recommended PCB Footprint for 60-pin QFN 7x7 package



Symbol	Description	Typical Dimension
e	Lead pitch	0.40 mm
b	Pad width	0.20 mm
L	Pad length	1.10 mm
X	-	5.80 mm
Y	-	4.60 mm
V	-	5.80 mm
W	-	6.00 mm

7 Ordering Information

Part Number	Description
AX88279QF	60-pin QFN lead Free package, Commercial temperature range: 0 to 70°C.

8 Revision History

Revision	Date	Comments
V0.10	2023/02/23	Preliminary release.
V0.20	2023/07/13	1.Updated power consumptions in section 5.2. 2. Added Recommended PCB Footprint for 60-pin QFN 7x7 package in Section 6
V1.00	2023/08/15	Updated some description in Table 1-4

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