Digital Computer Design Laboratory

#Poject2 Register File and Instruction Execution

1. In this project a register file shown in Figure-2 is a 16-register × 32-bit three-ported register file built from a three-ported memory. The register file has two read ports (A1/RD1 and A2/RD2) and one write port (A3/WD3). The 4-bit addresses, A1, A2, and A3, can each access all $2^4 = 16$ registers. Two registers can be read and one register written **simultaneously**.

   Create *register.sv* with behavioral design and test your design with *register_testbench.sv* .

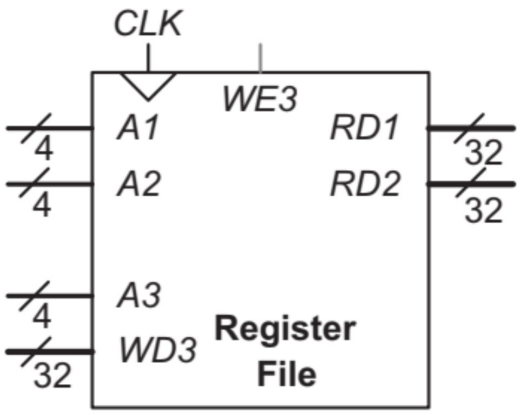

Figure-2

2. You will be creating a structural instruction separation and execution. An instruction has two-bit size instruction, four-bit size write register address, four-bit size read register address and another four-bit size second read register address as an input.

2 bit	4 bit	4 bit	4 bit
Ins.	REG_{WRT}	REG_1	REG_2

Your design should separate each instruction into the instruction and addresses. These values will be used as input to registerFile and ALU modules. The output of the ALU should be written into the register addressed by REG_{WRT}

Create *instruction.sv* with structural design and test your design with *register_instruction.sv* .

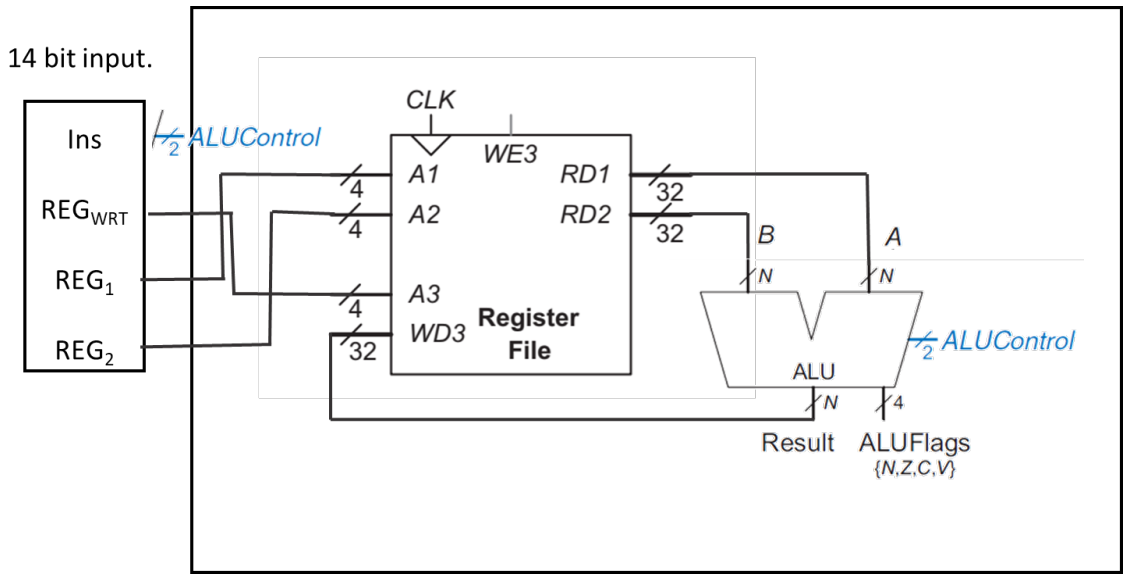

Figure-2