TU Delft
Analogue CMOS Design I — EE4520

Homework 2

Sjoerd Terlouw
5852455

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Abstract

Design of a discrete-time fully differential folded-cascode amplifier according to specifications in a feedback situation with a closed-loop gain of 8 times. The amplifier uses ideal gain-boosting and ideal common-mode feedback and is biased by the previous designed biasing block.

1 Table of Results

Table 1: Table of Results with personal specifications

	Design item	Unit	Specification	Achieved
1	Design Number		34	
2	SNR	$[dB]$	83.65	83.679
3	A_{settle}	$[dB]$	57	57
4	T_{settle}	$[\mu s]$	2.41	2.413
5	BW_{cl} from open-loop AC simulations	$[MHz]$		0.316
6	BW_{cl} from closed-loop AC simulations	$[MHz]$		0.316
7	Time-constant τ_{cl} from closed-loop AC simulations	$[\mu s]$		0.503
8	T_{40dB} (time to reach an accuracy of 40 dB)	$[\mu s]$		1.303
9	$T_{48.69dB}$ (time to reach an accuracy of 48.69 dB)	$[\mu s]$		1.813
10	Time-constant τ_{cl} from transient simulation	$[\mu s]$		0.510
11	Power dissipation[a]	$[\mu W]$	Lowest possible	213.208
12	$I(V_{dd})$[a]	$[\mu A]$	Lowest possible	118.449
13	Total integrated noise	$[\mu V_{rms}]$	55.74	55.553
14	Input step voltage	$[mV]$	150	150
15	Output step voltage	$[V]$	1.2	1.2
16	C_{in}	$[pF]$		32.360
17	C_{fb}	$[pF]$		4.045
18	C_{load}	$[pF]$		32.360
19	C_{CM}	$[pF]$		4.045
20	R_{big}	$[G\Omega]$	Big	1
21	C_{big}	$[uF]$	Big	1
22	Bonus points on FoM_{dB}	$[dB]$	0	0
23	$FoM_{lin} = 2\pi PT_{8.6dB}/SNR_{lin}^2$	$[aJ]$	≤ 3.98	2.929
24	$FoM_{dB} = -10\log_{10}(FoM_{lin})$	$[dB]$	≥ 174.0[b]	175.333

[a] Separate supply used for biasing

[b] Figure of Merit may exceed 176dB for good designs

Further specifications not in the table:

$$\begin{cases} C_{CM} = C_{fb} = C_{in}/8 \\ C_{load} = C_{in} \\ A_{add} = 100\ [\,] \end{cases} \tag{1}$$

Parameters for transient simulation:

$$\begin{cases} V_o = 1.2\ [V_{pd}] \\ V_i = 1.2/A_{cl}\ [V_{pd}] \\ \max V_o = 0.8485\ [V_{rms}] \end{cases} \tag{2}$$

And for biasing these relations should be fixed:

$$\begin{cases} I_{b,ncas} = r_n I_{b,main} \\ I_{b,pcas} = r_p I_{b,main} \\ C_{\text{decoupling}} = \sim 1\mu F \quad \text{(on all bias lines)} \end{cases} \tag{3}$$

And the fingers due to current specifications

$$\begin{cases} MN_{1,2}: & m = 4 \cdot S_A \\ MN_{5,6} = MN_{7,8}: & m = 4 \cdot S_A \\ MP_{1,3}: & m = 4 \cdot S_A r_{mp} \\ MP_{2,4}: & m = 2 \cdot S_A r_{mp} \\ MN_{3,4}: & m = 2 \cdot S_A \quad \text{(suggestion)} \end{cases} \tag{4}$$

2 Schematic with node voltages

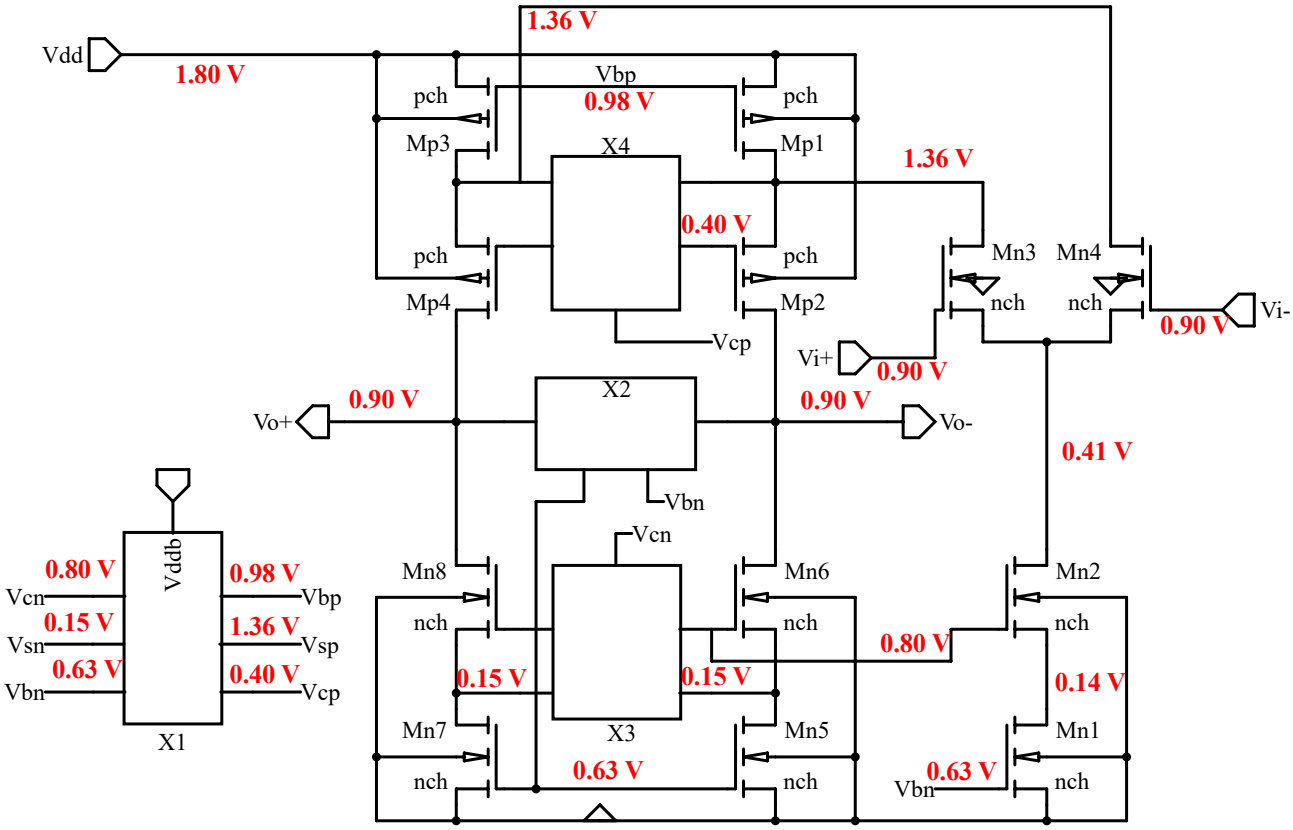

Figure 1: Opamp circuit with voltages from the operating point simulation

An easy overview of the voltages over the transistors and their operating region can be found in Table 2.

3 Schematic with branch currents

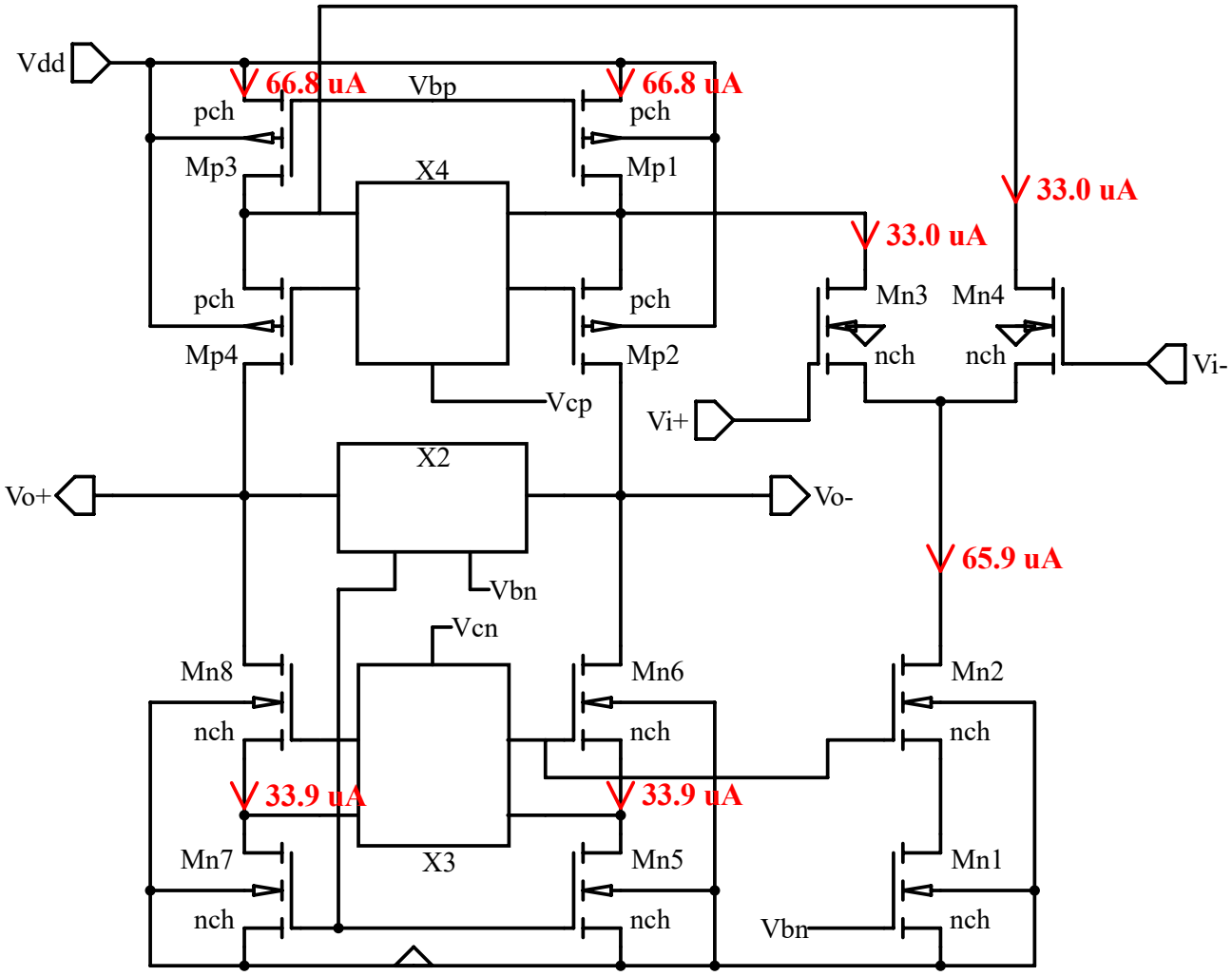

Figure 2: Opamp circuit with currents from the operating point simulation

As predicted by the equations in section 1, the current divides about equally over the two branches.

4 Bode-Diagram of A and $A\beta$

Plot of the amplifier gain A and the loop gain $A\beta$ versus $1Hz < f < 100GHz$, with the gain- and phase margin, unity-gain frequency f_{unity}, β and the time-constant of the closed-loop system indicated in the plot
Also explain the difference between loading the β-network with the OpAmp input or not while making sure the opamp is in the same state it normally is (inputs biased around CM-level, output biased around the CM-level and all currents identical to the normal situation)

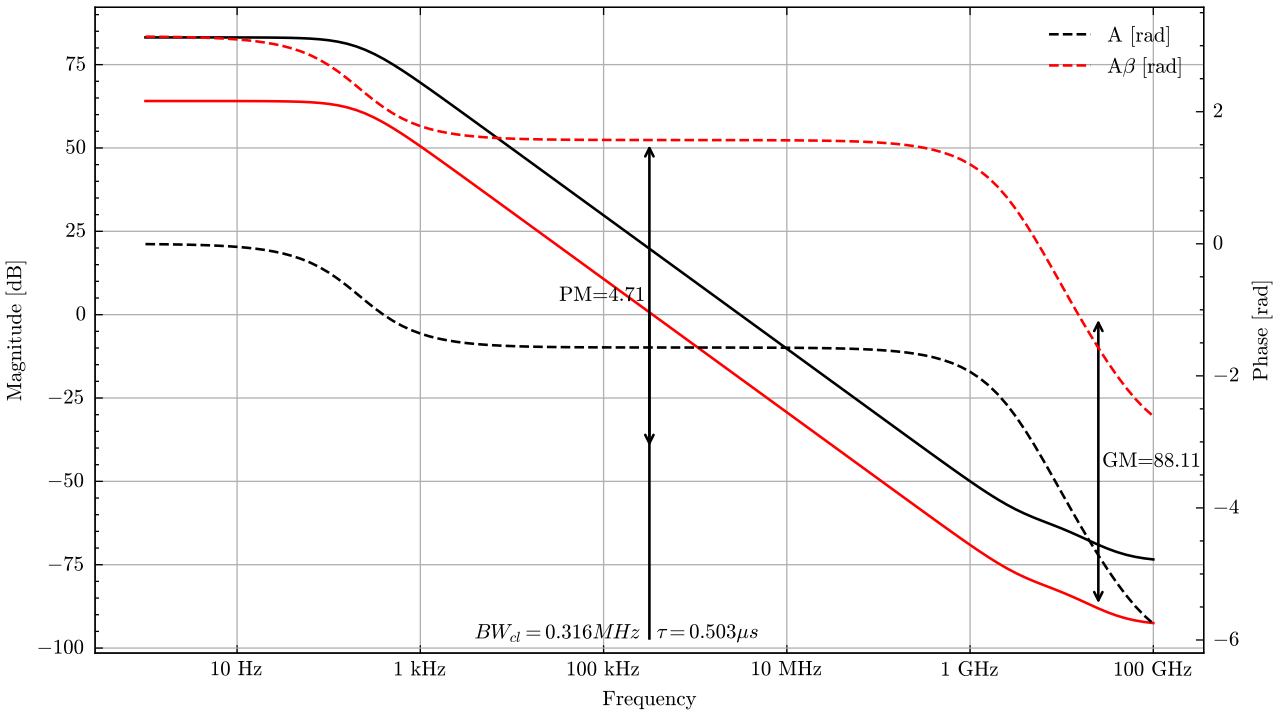

Figure 3: Bode diagram of A and $A\beta$ unloaded

These high phase and gain margins means the system is very stable and there will not be any ringing in the output or virtual ground, which is exactly what can be seen in Appendix A and section 6.

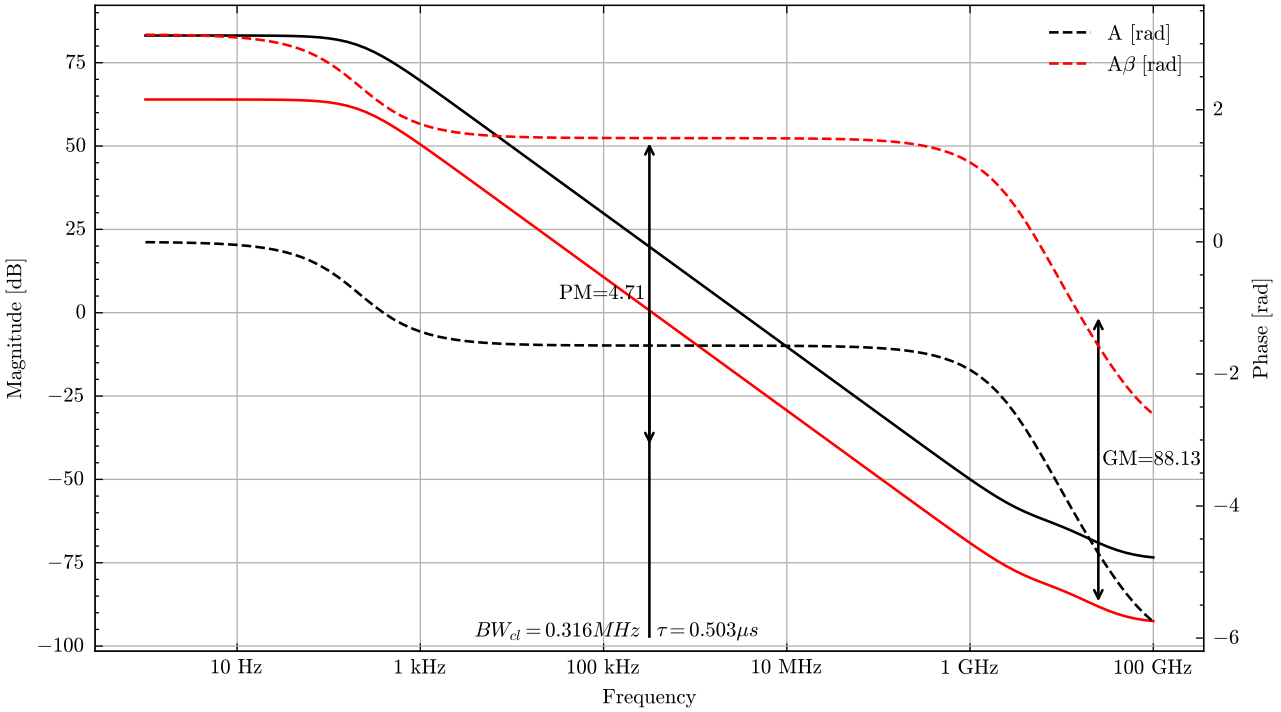

Figure 4: Bode diagram of A and $A\beta$ loaded

Loading the β-network with a copy of the amplifier adds a Miller capacitor to the feedback network to ground. This will obviously therefore not change DC and only have some influence at higher frequencies. The (not-Miller) input capacitance is given by $C_g = WLC_{ox}/3$ in parallel (approximating to only channel capacitance in the saturation region). This capacitance will be way smaller than any other capacitance in the circuit and will have little influence. In Table 2 the capacitance can be seen to be in the order of 10^{-14}. This is exactly what can be seen in the graphs; no relevant difference.

5 Bode-diagram of closed-loop gain

Plot the closed-loop gain versus $1Hz < f < 100GHz$ *showing an 8 times = 18.06 dB gain, with the -3dB bandwidth and closed-loop time-constant indicated*
Also compare the difference between the open- and closed-loop simulation

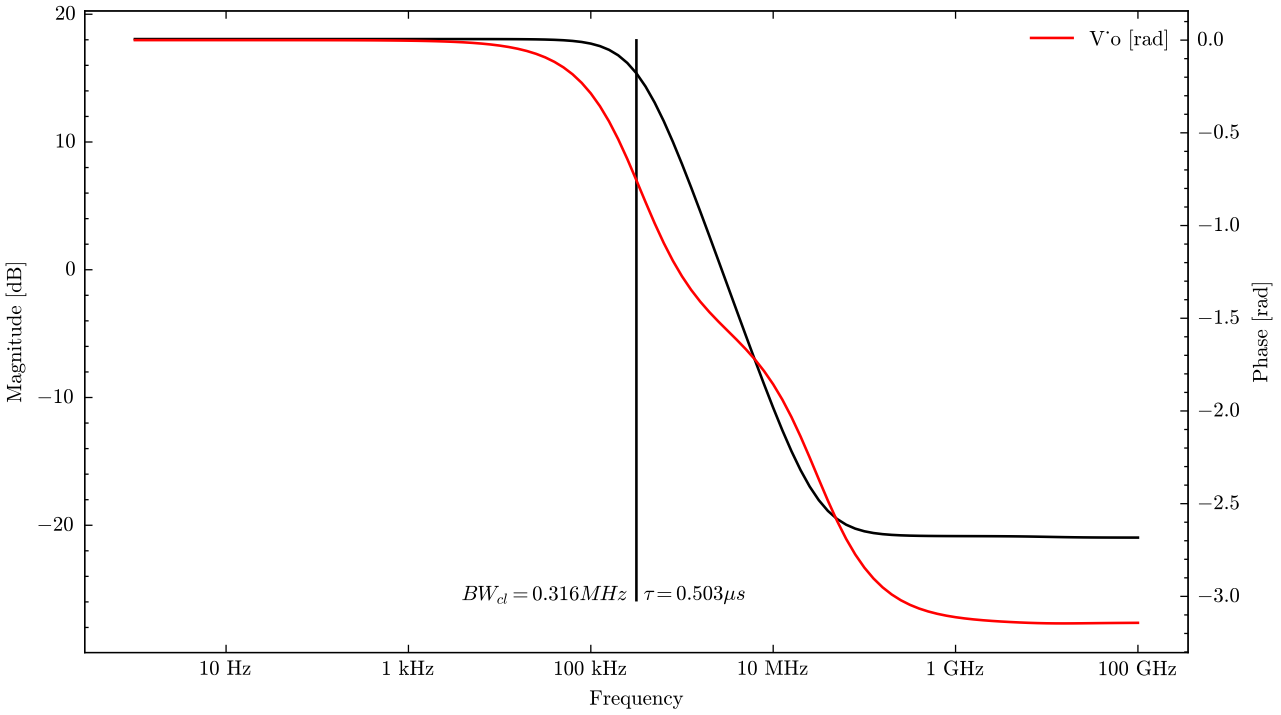

Figure 5: Closed loop ac simulation

As expected and also explained in the design section, the open-loop and closed-loop simulation are in line with each other in terms of bandwidth. You can also use $A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}(1 - \beta)$ to determine the closed loop gain from the open loop gain and feedback factor. That is shown in the next figure.
From this figure, it is clear that there still is a difference between the two simulations, despite the bandwidth being equal. The reason for this is that the first pole is counted double. That is the pole due to the load capacitance, which is not included in the previous equation.

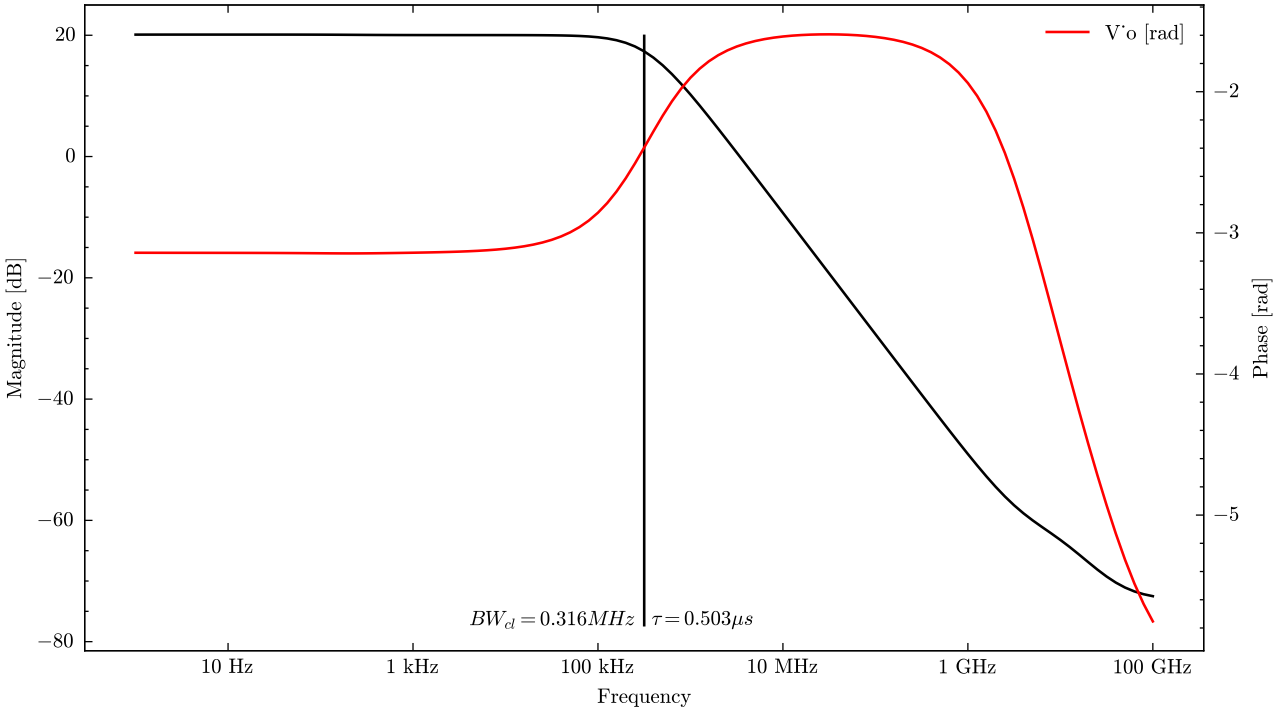

Figure 6: The closed loop gain obtained from the open loop gain using $A_{CL} = \dfrac{A_{OL}}{1 + A_{OL}\beta}(1 - \beta)$

6 Plot of settling behavior

Plot the settling accuracy versus time without over-designing according to the following equation:

$$Accuracy\,[dB] = 20\log_{10}\left(\frac{1.2\,[V]}{|V_{virtual\_ground}| + 1n}\right) \tag{5}$$

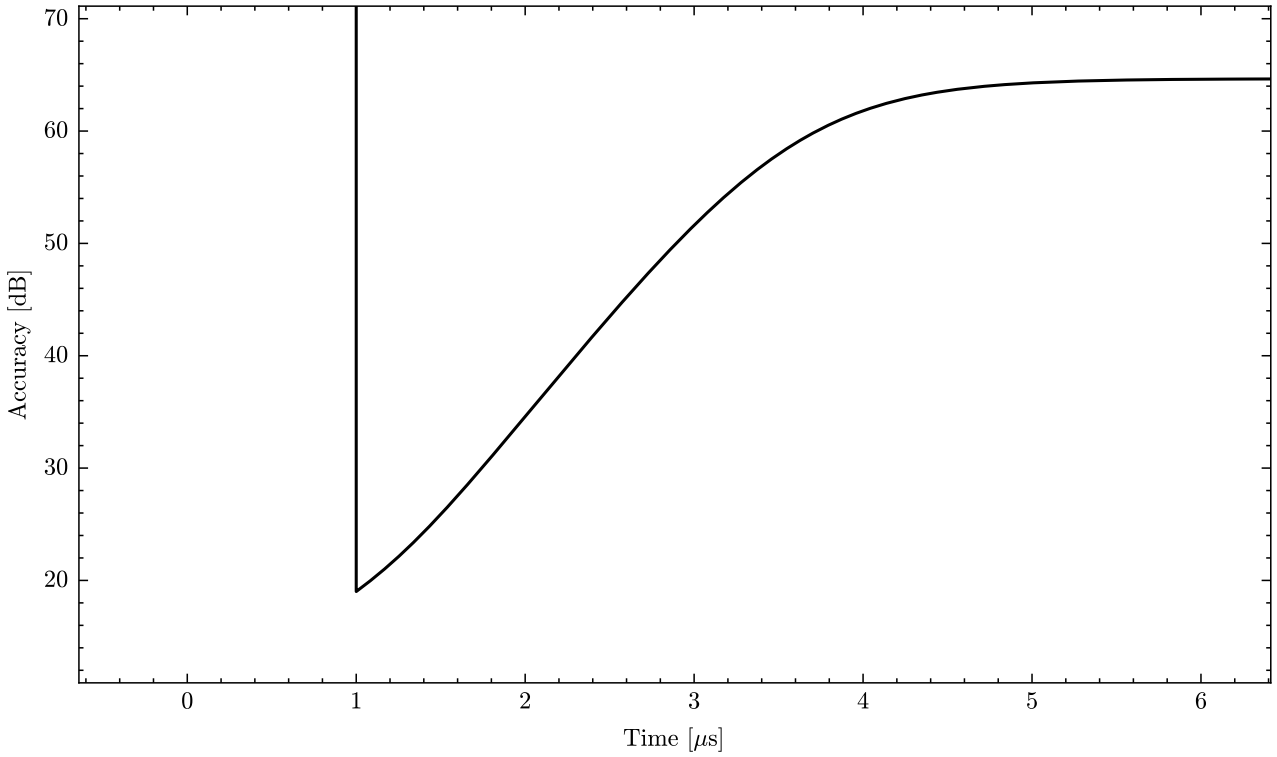

Figure 7: Settling accuracy without annotations

Annotations and analysis can be found in the next section.

7 Plot of settling behavior (annotated)

Determine $T_{settle}, T_{40dB}, T_{48.69dB}$ to calculate the closed-loop settling constant τ_{cl} and closed-loop bandwidth BW_{cl} (and compare them to section 4 and 5)
The plot and annotations differ $1\mu s$, since this is subtracted from the annotations due to the $1\mu s$ delay of the input step function (see Appendix A)

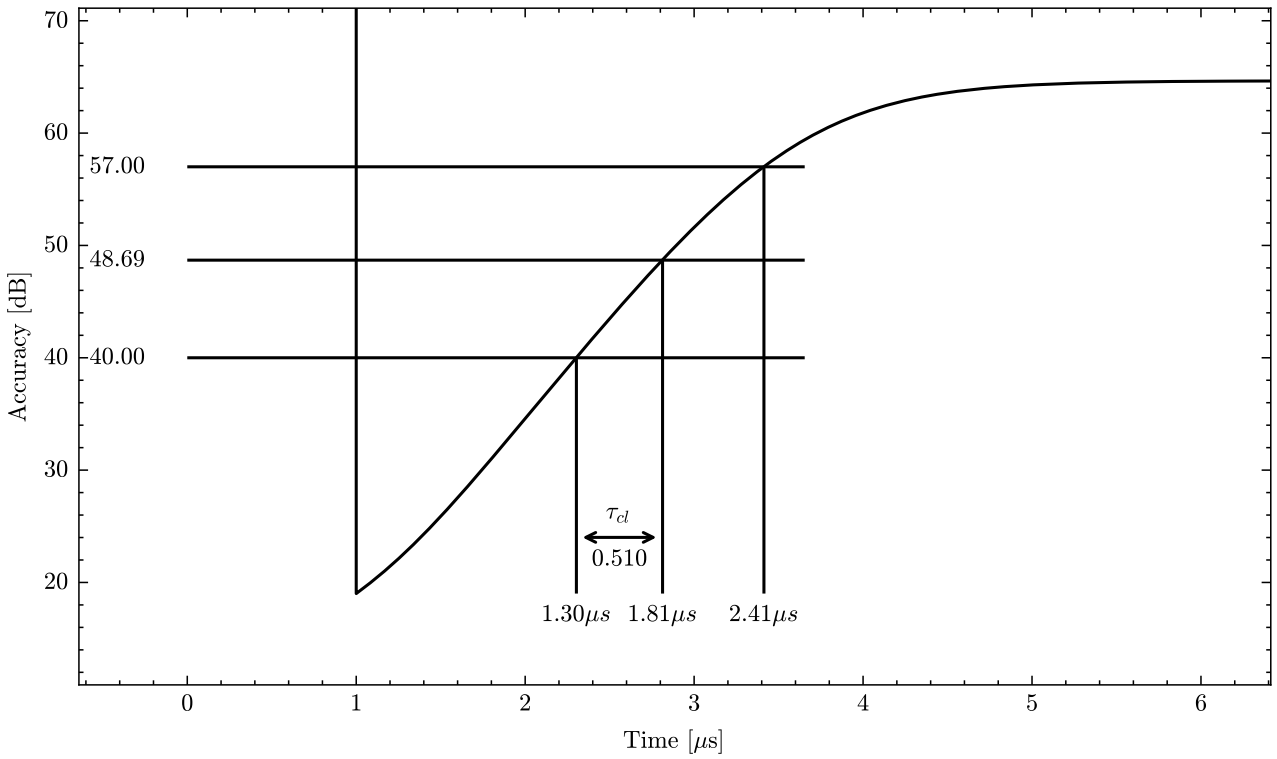

Figure 8: Settling accuracy with annotations

The time constant of the settling behaviour and AC analysis differ slightly. This is due the the fact that the settling behaviour is more realistic. The AC analysis uses a small-signal model and does not actually give insight in the entire behaviour. As also mentioned in the assignment, you can clearly see the slewing of the graph due to it not being a straight line.

8 Plot of noise density

Plot the noise and integrate over $10kHz < f < 100GHz$ *(different from AC), which is the lower end of the dynamic range or SNR*

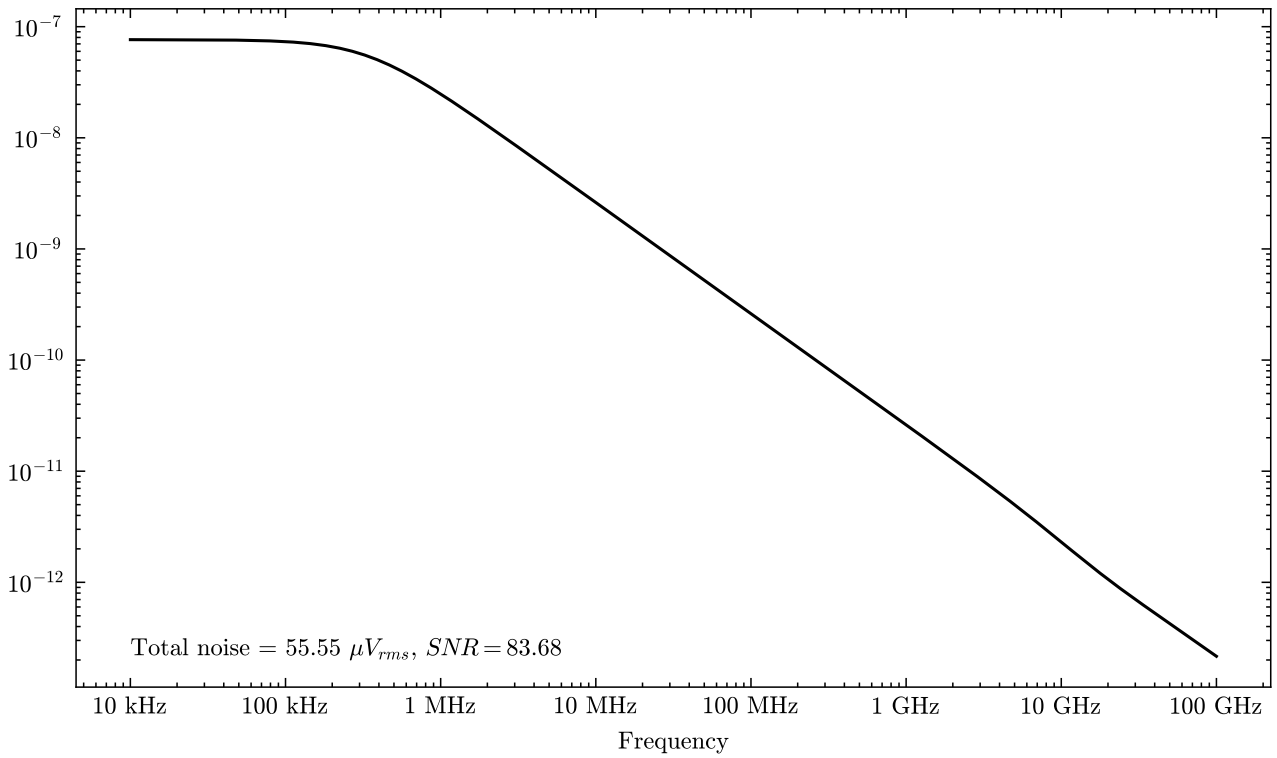

Figure 9: Closed loop noise analysis

This plot is done without $1/f$-noise of the transistors and therefore results in white noise, which is filtered mainly by the load capacitance. You can see therefore that the cutoff frequency in the noise plot is similar as the cutoff frequency in the closed loop AC analysis for example.

9 Design process

Explain arrival at final biasing and sizing and reasoning behind design steps
Also show how the open loop gain A, loop gain Aβ, closed-loop gain bandwidth B_{cl} and settling-curve are linked

9.1 Initial start

First up, for easy processing and analysis, a parameterized Python file was coupled to LaTeX and LTSpice such that this entire document can be automatically generated with all graphs, annotations and other values by only changing the variables S_a, R_{34}, R_{mp}, I_{bmain} and C_{in}. For testing to see if this works, the only requirement is that all transistors are in saturation. This is the case if the pMOS and nMOS transistors in the opamp are of similar size to the transistor in the biasing circuit. After this works, the actual theoretical analysis can start.

9.2 Theoretical analysis

Ideally, the feedback network is given by:

$$\beta = \frac{Z_{in}}{Z_{in} + Z_{fb}} = \frac{1}{9} = -19.08dB \tag{6}$$

Power can be determined to be approximately 250 μW to achieve high enough FoM with τ, SNR according to requirements and is almost entirely determined by twice the current going into MP_3, so

$$\begin{cases} P \approx 4m \cdot S_a R_{mp} (V_{GTp3})^2 \\ V_{GTp3} \approx 10\sqrt{\frac{I_{bmain}}{S_{ab}}} \end{cases} \rightarrow P \approx 0.4 S_a R_{mp} I_{bmain}/S_{ab} \approx 250\mu W \tag{7}$$

The DC gain is given by:

$$\frac{V_o}{V_i} = \frac{A g_b g_f}{\frac{A g_b}{r_b} - \left(\frac{1}{A g_c r_c r_d + r_c + r_d} + \frac{1}{r_b}\right)\left(A g_b + \frac{1}{r_f} + \frac{1}{r_b} + \frac{1}{r_a}\right)}^{1} \tag{8}$$

It's difficult to determine the exact values for r_o and g_m due to secondary effects, but it is known that $r_o \propto 1/W$ and $g_m \propto W$ which makes A_0 independent on most variables. The main thing to look at is the speed of settling. This is approximately given by:

$$f_{-3dB} \propto R_o C_L \tag{9}$$

Here is the load capacitance not only the load capacitance that can be seen in the closed loop circuit, but also the capacitance in the CMFB, which are both proportional to the input capacitance. The output impedance is mainly determined by S_a and $S_{ab}, {I_{bmain}}^2$.
SNR is mainly influenced by the output capacitance, which should be as small as possible while getting the correct SNR since a large capacitance ruins the speed. It is therefore convenient to use R_{34}, R_{mp} and S_{ab} to reduce noise, although these parameters have not that much influence.

9.3 Simulation

Very short and simplified: started with a capacitance that is a bit too low for a correct SNR, since other parameters are better to change to increase SNR without changing settling. From there, swept S_a and S_{ab} over reasonable ranges and found correct settling speed with minimal current. From there increased R_{34} significantly to reduce noise, increase settling speed and reduce current (up to a point). Reduced R_{mp} to decrease current and noise at the cost of slightly increasing settling time. Then repeated this a few times to get optimal values. From there used the parameterized python file to generate this document for several correct values and tuned everything a bit to increase the FoM. At the end, used Scikit-Optimize for a really tiny range around the ideal found inputs to get the last few 0.01dB.[3]. Final values are in subsection A.1.

9.4 Settling-curve, bode plots

Open loop gain is the gain of the amplifier itself A, which combined with β forms the closed loop gain $A_{CL} = \frac{A}{1 + A\beta}(1 - \beta)$, so the pole of the closed gain (=-3dB frequency = bandwidth) is given by $1 + A\beta = 0$, or when $A\beta = 0dB$. The settling curve starts at $1/\beta = 19.08dB$ and increases approximately 8.6dB/τ until A.

[1]Transistors: a = 1,3. b=2,4. c=6,8. d=7,5. e=2,1. f=3,4
[2]Changing I_{bmain} and S_{ab} with the same scaling has exactly the same result and therefore only one has to be considered
[3]Not terribly effective since the interface between Python and LTSpice is quite slow

A Transient analysis

This section is as a convenient check for myself, just as the table of the next section

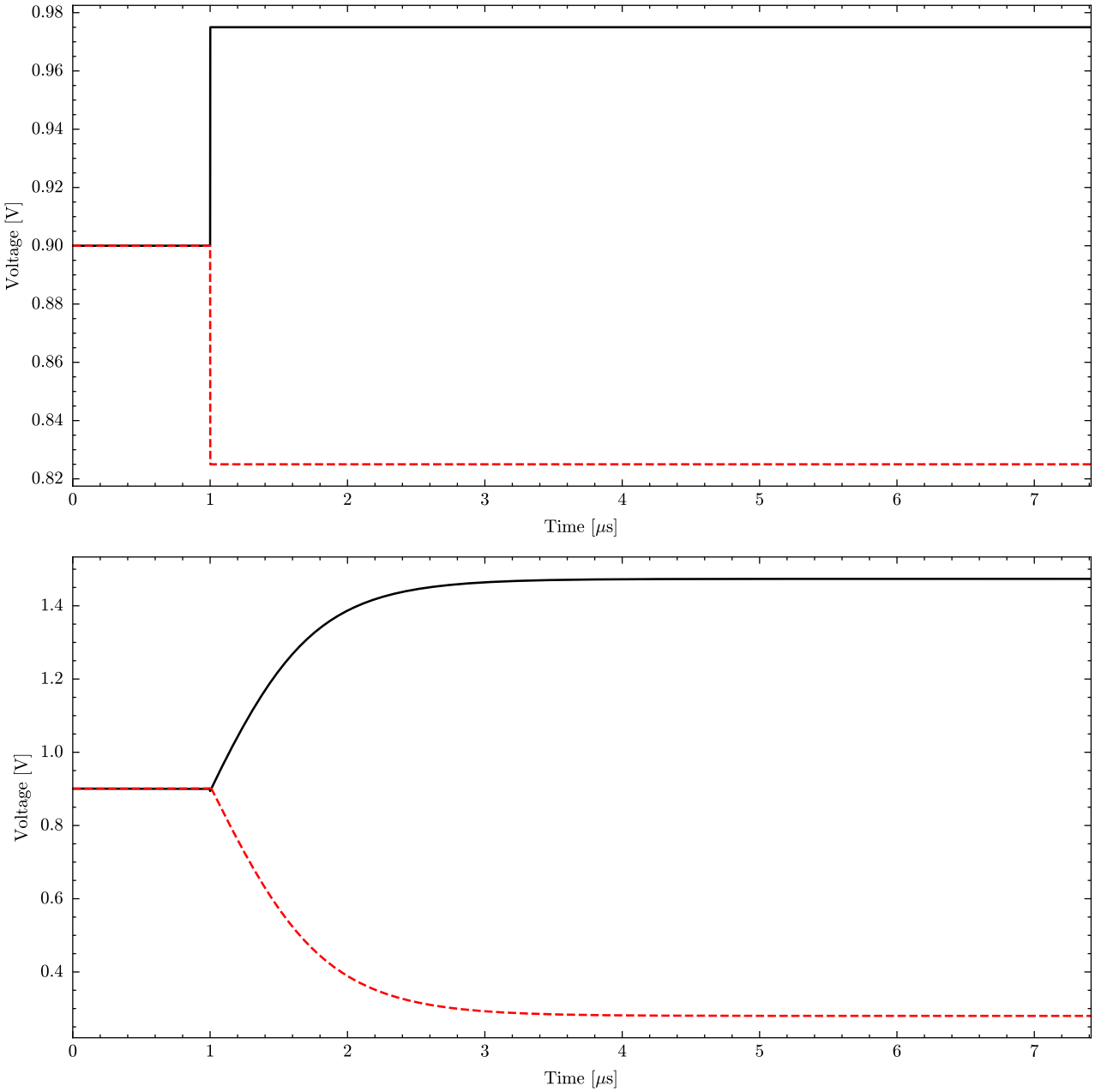

Figure 10: Ordinary transient analysis for the step input

A.1 Final values

$$\begin{cases} S_a = 0.986 \\ R_{34} = 95.0 \\ R_{mp} = 0.907 \\ I_{bmain} = 572.1\mu A \\ C_{in} = 32.36pF \\ S_{ab} = 16.907 \end{cases} \tag{10}$$

B Operating points

	m:x1:n1	m:x1:n2	m:x1:n3	m:x1:n4	m:x1:n5	m:x1:n6	m:x1:n7	m:x1:n8	m:x1:p1	m:x1:p2
$\|V_{Th}\|$	0.53	0.57	0.63	0.63	0.53	0.57	0.53	0.57	0.49	0.63
$\|V_{GS}\|$	0.63	0.66	0.49	0.49	0.63	0.65	0.63	0.65	0.82	0.96
$\|V_{DS} + V_{Th}\|$	0.67	0.83	1.58	1.58	0.68	1.31	0.68	1.31	0.94	1.09
$\|V_{GT} - V_{Th}\|$	0.11	0.10	-0.14	-0.14	0.11	0.08	0.11	0.08	0.32	0.33
Saturation?	True	True	False	False	True	True	True	True	True	True
Model:	x1:nch.9	x1:nch.9	x1:nch.9	x1:nch.9	x1:nch.9	x1:nch.9	x1:nch.9	x1:nch.9	x1:pch.9	x1:pch.9
Id:	65.90	65.90	33.00	33.00	33.90	33.90	33.90	33.90	-66.80	-33.90
Vgs:	6.33e-01	6.62e-01	4.93e-01	4.93e-01	6.34e-01	6.50e-01	6.34e-01	6.50e-01	-8.17e-01	-9.58e-01
Vds:	1.43e-01	2.64e-01	9.50e-01	9.50e-01	1.55e-01	7.46e-01	1.55e-01	7.46e-01	-4.43e-01	-4.57e-01
Vbs:	0.00e+00	-1.43e-01	-4.07e-01	-4.07e-01	0.00e+00	-1.55e-01	0.00e+00	-1.55e-01	0.00e+00	4.43e-01
Vth:	5.26e-01	5.67e-01	6.30e-01	6.30e-01	5.26e-01	5.69e-01	5.26e-01	5.69e-01	-4.94e-01	-6.30e-01
Vdsat:	1.17e-01	1.12e-01	4.61e-02	4.61e-02	1.17e-01	1.06e-01	1.17e-01	1.06e-01	-2.65e-01	-2.80e-01
Gm:	6.87e-04	7.56e-04	7.79e-04	7.79e-04	3.55e-04	4.06e-04	3.55e-04	4.06e-04	3.35e-04	1.67e-04
Gds:	1.25e-04	4.65e-05	1.70e-05	1.70e-05	5.48e-05	1.03e-05	5.48e-05	1.03e-05	2.86e-05	1.46e-05
Gmb	2.05e-04	2.04e-04	1.79e-04	1.79e-04	1.06e-04	1.07e-04	1.06e-04	1.07e-04	1.15e-04	4.85e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.31e-15	1.31e-15	3.12e-14	3.12e-14	6.57e-16	6.57e-16	6.57e-16	6.57e-16	1.29e-15	6.46e-16
Cgdov:	1.31e-15	1.31e-15	3.12e-14	3.12e-14	6.57e-16	6.57e-16	6.57e-16	6.57e-16	1.29e-15	6.46e-16
Cgbov:	1.26e-16	1.26e-16	2.98e-15	2.98e-15	6.28e-17	6.28e-17	6.28e-17	6.28e-17	1.66e-16	8.32e-17
dQgdVgb:	7.04e-15	6.91e-15	9.89e-14	9.89e-14	3.52e-15	3.40e-15	3.52e-15	3.40e-15	6.79e-15	3.38e-15
dQgdVdb:	-1.37e-15	-1.31e-15	-3.12e-14	-3.12e-14	-6.79e-16	-6.52e-16	-6.79e-16	-6.52e-16	-1.29e-15	-6.42e-16
dQgdVsb:	-4.90e-15	-4.80e-15	-3.27e-14	-3.27e-14	-2.45e-15	-2.33e-15	-2.45e-15	-2.33e-15	-5.14e-15	-2.58e-15
dQddVgb:	-1.50e-15	-1.35e-15	-3.12e-14	-3.12e-14	-7.34e-16	-6.59e-16	-7.34e-16	-6.59e-16	-1.32e-15	-6.60e-16
dQddVdb:	1.50e-15	1.34e-15	3.12e-14	3.12e-14	7.30e-16	6.57e-16	7.30e-16	6.57e-16	1.32e-15	6.60e-16
dQddVsb:	5.89e-17	2.80e-17	1.04e-18	1.04e-18	2.83e-17	2.04e-18	2.83e-17	2.04e-18	1.02e-17	4.31e-18
dQbdVgb:	-9.54e-16	-9.86e-16	-3.50e-14	-3.50e-14	-4.81e-16	-5.03e-16	-4.81e-16	-5.03e-16	-1.00e-15	-4.81e-16
dQbdVdb:	-5.59e-17	-5.38e-18	1.22e-18	1.22e-18	-2.23e-17	8.95e-19	-2.23e-17	8.95e-19	-8.58e-18	-3.96e-18
dQbdVsb:	-8.12e-16	-7.06e-16	-2.55e-16	-2.55e-16	-4.06e-16	-3.40e-16	-4.06e-16	-3.40e-16	-4.35e-16	-1.26e-16

Table 2: Voltages from the second operating point simulation

Transistors $n3$ and $n4$ are in subthreshold since this is a more efficient region to operate in.

	m:x1:p3	m:x1:p4	m:x1:x1:n1	m:x1:x1:n2	m:x1:x1:n3	m:x1:x1:p1	m:x1:x1:p2	m:x1:x1:p3
$\|V_{Th}\|$	0.49	0.63	0.53	0.57	0.53	0.49	0.63	0.49
$\|V_{GS}\|$	0.82	0.96	0.63	0.66	0.81	0.82	0.96	1.40
$\|V_{DS} + V_{Th}\|$	0.94	1.09	0.68	1.05	1.33	0.93	1.01	1.89
$\|V_{GT} - V_{Th}\|$	0.32	0.33	0.11	0.09	0.28	0.32	0.33	0.91
Saturation?	True	True	True	True	True	True	True	True
Model:	x1:pch.9	x1:pch.9	x1:x1:nch.9	x1:x1:nch.9	x1:x1:nch.9	x1:x1:pch.9	x1:x1:pch.9	x1:x1:pch.9
Id:	-66.80	-33.90	572.00	572.00	2750.00	-572.00	-572.00	-3550.00
Vgs:	-8.17e-01	-9.58e-01	6.33e-01	6.55e-01	8.05e-01	-8.17e-01	-9.62e-01	-1.40e+00
Vds:	-4.43e-01	-4.57e-01	1.50e-01	4.83e-01	8.05e-01	-4.39e-01	-3.78e-01	-1.40e+00
Vbs:	0.00e+00	4.43e-01	0.00e+00	-1.50e-01	0.00e+00	0.00e+00	4.39e-01	0.00e+00
Vth:	-4.94e-01	-6.30e-01	5.26e-01	5.68e-01	5.25e-01	-4.94e-01	-6.29e-01	-4.90e-01
Vdsat:	-2.65e-01	-2.80e-01	1.17e-01	1.09e-01	1.97e-01	-2.65e-01	-2.83e-01	-5.80e-01
Gm:	3.35e-04	1.67e-04	5.99e-03	6.79e-03	1.35e-02	2.87e-03	2.72e-03	5.80e-03
Gds:	2.86e-05	1.46e-05	9.85e-04	2.25e-04	4.88e-04	2.48e-04	3.41e-04	3.59e-04
Gmb	1.15e-04	4.85e-05	1.79e-03	1.82e-03	3.94e-03	9.86e-04	7.96e-04	2.03e-03
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.29e-15	6.46e-16	1.13e-14	1.13e-14	1.13e-14	1.11e-14	1.11e-14	1.11e-14
Cgdov:	1.29e-15	6.46e-16	1.13e-14	1.13e-14	1.13e-14	1.11e-14	1.11e-14	1.11e-14
Cgbov:	1.66e-16	8.32e-17	1.08e-15	1.08e-15	1.08e-15	1.43e-15	1.43e-15	1.43e-15
dQgdVgb:	6.79e-15	3.38e-15	6.03e-14	5.87e-14	6.25e-14	5.82e-14	5.81e-14	5.97e-14
dQgdVdb:	-1.29e-15	-6.42e-16	-1.17e-14	-1.12e-14	-1.12e-14	-1.11e-14	-1.11e-14	-1.10e-14
dQgdVsb:	-5.14e-15	-2.58e-15	-4.20e-14	-4.05e-14	-4.52e-14	-4.41e-14	-4.42e-14	-4.64e-14
dQddVgb:	-1.32e-15	-6.60e-16	-1.27e-14	-1.14e-14	-1.13e-14	-1.13e-14	-1.15e-14	-1.11e-14
dQddVdb:	1.32e-15	6.60e-16	1.26e-14	1.13e-14	1.13e-14	1.13e-14	1.16e-14	1.11e-14
dQddVsb:	1.02e-17	4.31e-18	4.95e-16	8.12e-17	3.92e-17	8.84e-17	6.79e-17	1.32e-17
dQbdVgb:	-1.00e-15	-4.81e-16	-8.22e-15	-8.58e-15	-8.69e-15	-8.57e-15	-8.19e-15	-8.90e-15
dQbdVdb:	-8.58e-18	-3.96e-18	-4.18e-16	8.57e-18	4.00e-18	-7.64e-17	-1.56e-16	1.02e-18
dQbdVsb:	-4.35e-16	-1.26e-16	-6.96e-15	-5.91e-15	-6.56e-15	-3.73e-15	-2.16e-15	-2.78e-15

Table 3: Voltages from the second operating point simulation

C Simulation

Symbol and Python files not included

C.1 Biasing circuit

```
Version 4
SHEET 1 3816 872
WIRE 1984 -160 1200 -160
WIRE 1200 -96 1200 -160
WIRE 1984 -96 1984 -160
WIRE 1984 -96 1200 -96
WIRE 1200 -32 1200 -96
WIRE 1984 -32 1984 -96
WIRE 1984 -32 1200 -32
WIRE 1344 16 1280 16
WIRE 1376 16 1344 16
WIRE 1504 16 1376 16
WIRE 1632 16 1504 16
WIRE 1696 16 1632 16
WIRE 1824 16 1696 16
WIRE 1872 16 1824 16
WIRE 1904 16 1872 16
WIRE 1776 32 1744 32
WIRE 1280 64 1280 16
WIRE 1632 64 1632 16
WIRE 1696 64 1632 64
WIRE 1824 64 1824 16
WIRE 1776 80 1776 32
WIRE 1872 80 1776 80
WIRE 1904 80 1872 80
WIRE 1696 144 1696 112
WIRE 1760 144 1696 144
WIRE 1824 144 1824 128
WIRE 1824 144 1760 144
WIRE 1904 144 1824 144
WIRE 1344 176 1344 16
WIRE 1696 176 1696 144
WIRE 1408 192 1392 192
WIRE 1424 192 1408 192
WIRE 1776 192 1744 192
WIRE 1280 224 1280 64
WIRE 1344 224 1280 224
WIRE 1632 224 1632 64
WIRE 1696 224 1632 224
WIRE 1776 224 1776 192
WIRE 1856 224 1776 224
WIRE 1904 224 1856 224
WIRE 1344 288 1344 272
WIRE 1408 288 1408 192
WIRE 1408 288 1344 288
WIRE 1696 288 1696 272
WIRE 1696 288 1584 288
WIRE 1344 320 1344 288
WIRE 1504 320 1504 16
WIRE 1696 320 1696 288
WIRE 1504 432 1504 400
```

```
WIRE 1504 432 1440 432
WIRE 1696 432 1696 400
WIRE 1696 432 1600 432
WIRE 1504 448 1504 432
WIRE 1696 448 1696 432
WIRE 1568 496 1504 496
WIRE 1760 496 1696 496
WIRE 1808 496 1792 496
WIRE 1888 496 1808 496
WIRE 1904 496 1888 496
WIRE 1440 528 1440 432
WIRE 1440 528 1424 528
WIRE 1456 528 1440 528
WIRE 1760 528 1760 496
WIRE 1824 528 1760 528
WIRE 1888 528 1888 496
WIRE 1696 576 1696 544
WIRE 1808 576 1696 576
WIRE 1888 576 1808 576
WIRE 1904 576 1888 576
WIRE 1696 608 1696 576
WIRE 1760 608 1760 528
WIRE 1824 608 1760 608
WIRE 1888 608 1888 576
WIRE 1344 624 1344 400
WIRE 1344 624 1296 624
WIRE 1600 640 1600 432
WIRE 1296 656 1296 624
WIRE 1760 656 1760 608
WIRE 1760 656 1696 656
WIRE 1808 656 1792 656
WIRE 1888 656 1808 656
WIRE 1904 656 1888 656
WIRE 1600 688 1600 640
WIRE 1648 688 1600 688
WIRE 1760 688 1760 656
WIRE 1824 688 1760 688
WIRE 1888 688 1888 656
WIRE 1344 704 1344 624
WIRE 1504 704 1504 544
WIRE 1504 704 1344 704
WIRE 1568 704 1568 496
WIRE 1568 704 1504 704
WIRE 1696 704 1568 704
WIRE 1760 704 1760 688
WIRE 1760 704 1696 704
WIRE 1200 720 1200 −32
WIRE 1984 720 1984 −32
WIRE 1984 720 1200 720
FLAG 1376 16 vdd
FLAG 1760 144 Vsp
FLAG 1776 192 Vcp
FLAG 1776 32 Vbp
FLAG 1600 640 Vbn
FLAG 1808 656 Vbn
FLAG 1808 576 Vsn
FLAG 1808 496 Vcn
```

```
FLAG 1296 656 0
FLAG 1648 528 Vcn
FLAG 1424 528 Vcn
FLAG 1424 192 Vcp
FLAG 1584 288 Vbp
FLAG 1904 80 Vbp
IOPIN 1904 80 Out
FLAG 1904 144 Vsp
IOPIN 1904 144 Out
FLAG 1904 224 Vcp
IOPIN 1904 224 Out
FLAG 1904 496 Vcn
IOPIN 1904 496 Out
FLAG 1904 576 Vsn
IOPIN 1904 576 Out
FLAG 1904 656 Vbn
IOPIN 1904 656 Out
FLAG 1280 64 Vdd
IOPIN 1280 64 BiDir
FLAG 1856 288 vdd
DATAFLAG 1696 144 "round($*100)/100"
DATAFLAG 1792 80 "round($*100)/100"
SYMBOL nmos4 1648 448 R0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn2
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*2}
SYMBOL current 1696 320 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName Ibmain
SYMATTR Value {Ibmain}
SYMBOL current 1504 320 R0
WINDOW 0 -95 -2 Left 2
WINDOW 3 -114 79 Left 2
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName Ibncas
SYMATTR Value {Ibncas}
SYMBOL pmos4 1744 272 R180
WINDOW 0 53 24 Left 2
SYMATTR InstName Mp2
SYMATTR Value pch
SYMATTR Value2 l={L} w={W} m={Sa*Rmp*2}
SYMBOL pmos4 1744 112 R180
WINDOW 0 55 26 Left 2
SYMATTR InstName Mp1
SYMATTR Value pch
SYMATTR Value2 l={L} w={W} m={Sa*Rmp*2}
SYMBOL nmos4 1456 448 R0
SYMATTR InstName Mn3
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*2}
SYMBOL current 1344 320 R0
WINDOW 0 -114 3 Left 2
WINDOW 3 -126 73 Left 2
WINDOW 123 0 0 Left 0
```

```
WINDOW 39 0 0 Left 0
SYMATTR InstName Ibpcas
SYMATTR Value {Ibpcas}
SYMBOL pmos4 1392 272 R180
WINDOW 0 53 24 Left 2
SYMATTR InstName Mp3
SYMATTR Value pch
SYMATTR Value2 l={L} w={W} m={Sa*Rmp*2}
SYMBOL nmos4 1648 608 R0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn1
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*2}
SYMBOL cap 1856 16 R0
SYMATTR InstName C1
SYMATTR Value {Cbig}
SYMBOL cap 1808 64 R0
SYMATTR InstName C2
SYMATTR Value {Cbig}
SYMBOL cap 1840 224 R0
SYMATTR InstName C3
SYMATTR Value {Cbig}
SYMBOL cap 1824 544 R270
WINDOW 0 32 32 VTop 2
WINDOW 3 0 32 VBottom 2
SYMATTR InstName C4
SYMATTR Value {Cbig}
SYMBOL cap 1824 624 R270
WINDOW 0 32 32 VTop 2
WINDOW 3 0 32 VBottom 2
SYMATTR InstName C5
SYMATTR Value {Cbig}
SYMBOL cap 1824 704 R270
WINDOW 0 32 32 VTop 2
WINDOW 3 0 32 VBottom 2
SYMATTR InstName C6
SYMATTR Value {Cbig}
TEXT 1200 744 Left 2 !.lib 'C:\\Users\\terlo\\OneDrive\\Documenten\\LTspiceXVII
    \\lib\\cmp\\log018.l' TT
TEXT 1216 -176 Left 2 ;BIASING CIRCUIT
TEXT 1200 768 Left 2 !.params W=1u L=0.18u
TEXT 1208 -120 Left 2 !.param Ibmain=200u Rbn=4.8 Rbp=6.2
TEXT 1208 -56 Left 2 !.param Ibpcas = {Ibmain*Rbp} Ibncas = {Ibmain*Rbn}
TEXT 1680 -144 Left 2 !.param Cbig=1u
TEXT 1688 -120 Left 2 !.param Sa=0.4
TEXT 1680 -184 Left 2 !.param Rmp=4.85
```

C.2 Opamp

```
Version 4
SHEET 1 3816 880
WIRE 1456 -96 1440 -96
WIRE 2032 -96 1456 -96
WIRE 1296 -48 1040 -48
WIRE 1376 -48 1296 -48
WIRE 1696 -48 1376 -48
WIRE 1776 -48 1696 -48
WIRE 1376 -32 1376 -48
```

WIRE 1696 −32 1696 −48
WIRE 1536 −16 1424 −16
WIRE 1648 −16 1536 −16
WIRE 1296 16 1296 −48
WIRE 1376 16 1296 16
WIRE 1776 16 1776 −48
WIRE 1776 16 1696 16
WIRE 1376 80 1376 64
WIRE 1440 80 1440 −96
WIRE 1440 80 1376 80
WIRE 1696 80 1696 64
WIRE 1696 80 1632 80
WIRE 1824 80 1696 80
WIRE 1904 80 1824 80
WIRE 1376 128 1376 80
WIRE 1696 128 1696 80
WIRE 1904 128 1904 80
WIRE 2032 128 2032 −96
WIRE 1440 144 1424 144
WIRE 1648 144 1632 144
WIRE 1296 176 1296 16
WIRE 1376 176 1296 176
WIRE 1776 176 1776 16
WIRE 1776 176 1696 176
WIRE 928 208 880 208
WIRE 1136 208 1088 208
WIRE 2144 208 2080 208
WIRE 1632 240 1536 240
WIRE 1904 240 1904 224
WIRE 1968 240 1904 240
WIRE 2032 240 2032 224
WIRE 2032 240 1968 240
WIRE 928 256 880 256
WIRE 1136 256 1088 256
WIRE 1856 256 1856 208
WIRE 1856 256 1792 256
WIRE 1968 272 1968 240
WIRE 928 304 880 304
WIRE 1136 304 1088 304
WIRE 1376 320 1376 224
WIRE 1376 320 1264 320
WIRE 1424 320 1376 320
WIRE 1696 320 1696 224
WIRE 1696 320 1648 320
WIRE 1808 320 1696 320
WIRE 1504 400 1456 400
WIRE 1584 400 1568 400
WIRE 1552 432 1536 432
WIRE 1376 448 1376 320
WIRE 1696 448 1696 320
WIRE 1968 448 1968 272
WIRE 1376 496 1296 496
WIRE 1776 496 1696 496
WIRE 2048 496 1968 496
WIRE 1440 528 1440 496
WIRE 1440 528 1424 528
WIRE 1648 528 1632 528

```
WIRE 1920 528 1872 528
WIRE 1840 560 1824 560
WIRE 1872 560 1872 528
WIRE 1872 560 1840 560
WIRE 1376 592 1376 544
WIRE 1408 592 1376 592
WIRE 1440 592 1408 592
WIRE 1648 592 1632 592
WIRE 1696 592 1696 544
WIRE 1696 592 1648 592
WIRE 1376 608 1376 592
WIRE 1696 608 1696 592
WIRE 1968 608 1968 544
WIRE 1296 656 1296 496
WIRE 1376 656 1296 656
WIRE 1776 656 1776 496
WIRE 1776 656 1696 656
WIRE 2048 656 2048 496
WIRE 2048 656 1968 656
WIRE 1456 688 1456 400
WIRE 1456 688 1424 688
WIRE 1648 688 1456 688
WIRE 1920 688 1856 688
WIRE 1296 720 1296 656
WIRE 1376 720 1376 704
WIRE 1376 720 1296 720
WIRE 1520 720 1376 720
WIRE 1696 720 1696 704
WIRE 1696 720 1520 720
WIRE 1776 720 1776 656
WIRE 1776 720 1696 720
WIRE 1968 720 1968 704
WIRE 1968 720 1776 720
WIRE 2048 720 2048 656
WIRE 2048 720 1968 720
FLAG 1040 −48 Vdd
IOPIN 1040 −48 In
FLAG 2032 176 0
FLAG 1904 176 0
FLAG 1792 256 Vi+
IOPIN 1792 256 In
FLAG 2144 208 Vi−
IOPIN 2144 208 In
FLAG 1008 112 Vddb
IOPIN 1008 112 In
FLAG 1520 720 0
FLAG 880 304 Vbn
FLAG 1584 400 Vbn
FLAG 880 208 Vcn
FLAG 1552 432 Vcn
FLAG 880 256 Vsn
FLAG 1136 208 Vbp
FLAG 1264 320 Vo+
IOPIN 1264 320 Out
FLAG 1808 320 Vo−
IOPIN 1808 320 Out
FLAG 1856 688 Vbn
```

```
FLAG 1536 -16 Vbp
FLAG 1136 304 Vcp
FLAG 1632 240 Vcp
FLAG 1136 256 Vsp
FLAG 1968 272 Vsi
FLAG 1968 544 Vssi
FLAG 1456 688 Vbcm
FLAG 1824 80 Vpmr
FLAG 1632 144 Vpg
FLAG 1408 592 Vnml
FLAG 1648 592 Vnmr
FLAG 1456 -96 Vpml
FLAG 1840 560 Vcn
DATAFLAG 1216 -48 "round($*100)/100"
DATAFLAG 1104 208 "round($*100)/100"
DATAFLAG 1104 256 "round($*100)/100"
DATAFLAG 1104 304 "round($*100)/100"
DATAFLAG 912 304 "round($*100)/100"
DATAFLAG 912 256 "round($*100)/100"
DATAFLAG 912 208 "round($*100)/100"
DATAFLAG 1328 320 "round($*100)/100"
DATAFLAG 1760 320 "round($*100)/100"
DATAFLAG 2032 32 "round($*100)/100"
DATAFLAG 1904 80 "round($*100)/100"
DATAFLAG 1872 528 "round($*100)/100"
DATAFLAG 1552 688 "round($*100)/100"
DATAFLAG 1536 432 "round($*100)/100"
DATAFLAG 1568 400 "round($*100)/100"
DATAFLAG 1968 336 "round($*100)/100"
DATAFLAG 2112 208 "round($*100)/100"
DATAFLAG 1888 688 "round($*100)/100"
DATAFLAG 1824 256 "round($*100)/100"
DATAFLAG 1968 576 "round($*100)/100"
DATAFLAG 1440 496 "round($*100)/100"
DATAFLAG 1408 80 "round($*100)/100"
DATAFLAG 1616 -16 "round($*100)/100"
DATAFLAG 1600 240 "round($*100)/100"
DATAFLAG 1440 144 "round($*100)/100"
SYMBOL pmos4 1648 224 M180
WINDOW 0 53 24 Left 2
SYMATTR InstName Mp2
SYMATTR Value pch
SYMATTR Value2 l={L} w={W} m={Sa*Rmp*2}
SYMBOL nmos4 1648 448 R0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn6
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*2}
SYMBOL pmos4 1424 224 R180
WINDOW 0 53 24 Left 2
SYMATTR InstName Mp4
SYMATTR Value pch
SYMATTR Value2 l={L} w={W} m={Sa*Rmp*2}
SYMBOL Biasing_circuit 752 384 R90
WINDOW 39 11 -256 VBottom 2
SYMATTR SpiceLine Rbn={Rbn} Rbp={Rbp} Ibmain={Ibmain} Sa = {Sa_b} Rmp = {Rmp}
SYMATTR InstName X1
```

```
SYMBOL gain_boosting_nmos 1536 560 R0
SYMATTR InstName X3
SYMBOL gain_boosting_pmos 1536 112 R0
SYMATTR InstName X4
SYMBOL CMFB 1520 320 R0
WINDOW 39 17 8 Bottom 2
SYMATTR SpiceLine Cin={Cin}
SYMATTR InstName X2
SYMBOL pmos4 1424 64 R180
WINDOW 0 53 24 Left 2
SYMATTR InstName Mp3
SYMATTR Value pch
SYMATTR Value2 l={L} w={W} m={4*Sa*Rmp}
SYMBOL pmos4 1648 64 M180
WINDOW 0 53 24 Left 2
SYMATTR InstName Mp1
SYMATTR Value pch
SYMATTR Value2 l={L} w={W} m={4*Sa*Rmp}
SYMBOL nmos4 1424 448 M0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn8
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*2}
SYMBOL nmos4 1648 608 R0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn5
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*2}
SYMBOL nmos4 1424 608 M0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn7
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*2}
SYMBOL nmos4 1920 608 R0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn1
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={4*Sa}
SYMBOL nmos4 1920 448 R0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn2
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={4*Sa}
SYMBOL nmos4 1856 128 R0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn3
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*R34}
SYMBOL nmos4 2080 128 M0
WINDOW 0 57 21 Left 2
SYMATTR InstName Mn4
SYMATTR Value nch
SYMATTR Value2 l={L} w={W} m={Sa*R34}
TEXT 968 -248 Left 2 !.lib 'C:\\Users\\terlo\\OneDrive\\Documenten\\LTspiceXVII
    \\lib\\cmp\\log018.l' TT
TEXT 968 -224 Left 2 !.params W=1u L=0.18u
TEXT 968 -280 Left 2 !.param Rbn=4.8 Rbp=6.2
```

```
TEXT 968 -200 Left 2 !.param Sa=1 Rmp=1 R34=2.5 Sa_b=0.4 Cin=10p
TEXT 968 -176 Left 2 !.param Ibmain=200u
```

C.3 CMFB

```
Version 4
SHEET 1 880 680
WIRE -32 192 -80 192
WIRE 0 192 -32 192
WIRE 160 192 80 192
WIRE 240 192 160 192
WIRE 352 192 320 192
WIRE 400 192 352 192
WIRE -32 224 -32 192
WIRE 160 224 160 192
WIRE 352 224 352 192
WIRE -32 320 -32 288
WIRE 160 320 160 304
WIRE 160 320 -32 320
WIRE 352 320 352 288
WIRE 352 320 160 320
WIRE 160 352 160 320
WIRE 336 352 288 352
FLAG -80 192 Vo+
IOPIN -80 192 Out
FLAG 160 352 Vbcm
IOPIN 160 352 In
FLAG 288 352 Vbn
IOPIN 288 352 In
FLAG 400 192 Vo-
IOPIN 400 192 Out
DATAFLAG 160 192 "round($*1000)/1000"
DATAFLAG -32 192 "round($*1000)/1000"
DATAFLAG 352 192 "round($*1000)/1000"
DATAFLAG 80 320 "round($*1000)/1000"
DATAFLAG 336 352 "round($*1000)/1000"
SYMBOL res 96 176 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName R1
SYMATTR Value {Rbig}
SYMBOL cap -48 224 R0
SYMATTR InstName C1
SYMATTR Value {CCM}
SYMBOL bv 160 208 R0
SYMATTR InstName B1
SYMATTR Value V=0.9-V(Vbn)
SYMBOL res 336 176 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName R2
SYMATTR Value {Rbig}
SYMBOL cap 336 224 R0
SYMATTR InstName C2
SYMATTR Value {CCM}
TEXT 72 128 Left 2 !.param Cin=10n Rbig=1G CCM={Cin/8}
```

C.4 Gain-boosting

```
Version 4
SHEET 1 1104 680
WIRE 128 -112 128 -160
WIRE 224 -96 160 -96
WIRE -80 32 -128 32
WIRE 128 32 128 -32
WIRE 128 32 0 32
WIRE 256 32 128 32
WIRE 464 32 336 32
WIRE 96 176 -16 176
WIRE 304 176 160 176
FLAG 128 -160 0
FLAG 224 -96 Vcn
IOPIN 224 -96 In
FLAG -16 176 Vg
IOPIN -16 176 In
FLAG 304 176 Vn
IOPIN 304 176 In
FLAG -128 32 Vo-
IOPIN -128 32 Out
FLAG 464 32 Vo+
IOPIN 464 32 Out
DATAFLAG -96 32 "round($*1000)/1000"
DATAFLAG 64 176 "round($*1000)/1000"
DATAFLAG 128 32 "round($*1000)/1000"
DATAFLAG 224 176 "round($*1000)/1000"
SYMBOL bv 16 32 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName B1
SYMATTR Value V={Aadd}*(V(Vg)-V(Vn))/2
SYMBOL bv 352 32 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName B2
SYMATTR Value V={Aadd}*(V(Vg)-V(Vn))/2
SYMBOL bv 128 -16 R180
WINDOW 0 24 96 Left 2
WINDOW 3 24 16 Left 2
SYMATTR InstName B3
SYMATTR Value V=V(Vcn)
TEXT 352 -40 Left 2 !.param Aadd=100
```

```
Version 4
SHEET 1 880 680
WIRE 128 48 16 48
WIRE 336 48 208 48
WIRE -32 192 -80 192
WIRE 176 192 48 192
WIRE 304 192 176 192
WIRE 432 192 384 192
WIRE 176 256 176 192
WIRE 384 320 320 320
WIRE 176 384 176 336
FLAG 176 384 0
```

```
FLAG 384 320 Vcp
IOPIN 384 320 In
FLAG 16 48 Vg
IOPIN 16 48 In
FLAG 336 48 Vp
IOPIN 336 48 In
FLAG -80 192 Vo-
IOPIN -80 192 Out
FLAG 432 192 Vo+
IOPIN 432 192 Out
DATAFLAG 272 48 "round($*1000)/1000"
DATAFLAG 80 48 "round($*1000)/1000"
DATAFLAG 128 192 "round($*1000)/1000"
DATAFLAG 400 192 "round($*1000)/1000"
DATAFLAG -64 192 "round($*1000)/1000"
SYMBOL bv 64 192 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName B1
SYMATTR Value V={Aadd}*(V(Vg)-V(Vp))/2
SYMBOL bv 400 192 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName B2
SYMATTR Value V={Aadd}*(V(Vg)-V(Vp))/2
SYMBOL bv 176 240 R0
SYMATTR InstName B3
SYMATTR Value V=V(Vcp)
TEXT 80 -72 Left 2 !.param Aadd=100
```

C.5 Closed loop

```
Version 4
SHEET 1 1268 800
WIRE 128 -96 96 -96
WIRE 208 -96 192 -96
WIRE 96 -48 96 -96
WIRE 96 -48 32 -48
WIRE 208 -48 208 -96
WIRE 336 -48 208 -48
WIRE 96 0 96 -48
WIRE 112 0 96 0
WIRE 208 0 208 -48
WIRE 208 0 192 0
WIRE 160 96 160 80
WIRE -176 160 -208 160
WIRE -96 160 -112 160
WIRE 160 192 160 176
WIRE -448 208 -512 208
WIRE -208 208 -208 160
WIRE -208 208 -368 208
WIRE -96 208 -96 160
WIRE -48 208 -96 208
WIRE -208 256 -208 208
WIRE -192 256 -208 256
WIRE -96 256 -96 208
WIRE -96 256 -112 256
WIRE 768 256 672 256
```

```
WIRE −48 272 −48 208
WIRE 32 272 32 −48
WIRE 32 272 −48 272
WIRE 80 272 32 272
WIRE 336 272 336 −48
WIRE 336 272 288 272
WIRE 432 272 432 240
WIRE 432 272 336 272
WIRE 480 272 432 272
WIRE 624 272 480 272
WIRE −512 288 −512 208
WIRE 32 320 −48 320
WIRE 80 320 32 320
WIRE −176 336 −208 336
WIRE −96 336 −112 336
WIRE 336 336 288 336
WIRE 432 336 336 336
WIRE 480 336 432 336
WIRE 624 336 624 320
WIRE 624 336 480 336
WIRE 432 368 432 336
WIRE −512 384 −512 288
WIRE −448 384 −512 384
WIRE −208 384 −208 336
WIRE −208 384 −368 384
WIRE −96 384 −96 336
WIRE −48 384 −48 320
WIRE −48 384 −96 384
WIRE 160 416 160 400
WIRE −208 432 −208 384
WIRE −192 432 −208 432
WIRE −96 432 −96 384
WIRE −96 432 −112 432
WIRE 160 512 160 496
WIRE 144 592 112 592
WIRE 224 592 208 592
WIRE 32 640 32 320
WIRE 112 640 112 592
WIRE 112 640 32 640
WIRE 224 640 224 592
WIRE 336 640 336 336
WIRE 336 640 224 640
WIRE 112 688 112 640
WIRE 128 688 112 688
WIRE 224 688 224 640
WIRE 224 688 208 688
FLAG 160 80 0
FLAG 160 512 0
FLAG 480 272 Vop
FLAG 480 336 Von
FLAG 432 176 0
FLAG 432 432 0
FLAG −592 288 0
FLAG −1056 432 0
FLAG −1056 352 Vi
FLAG 768 256 Vo
FLAG 672 336 0
```

```
DATAFLAG -336 208 "round($*100)/100"
DATAFLAG -272 384 "round($*100)/100"
DATAFLAG -32 320 "round($*100)/100"
DATAFLAG 0 272 "round($*100)/100"
DATAFLAG 304 272 "round($*100)/100"
DATAFLAG 368 336 "round($*100)/100"
SYMBOL op_amp 192 384 R0
WINDOW 39 79 391 Bottom 2
SYMATTR SpiceLine Rbn={Rbn} Rbp={Rbp} Sa={Sa} Rmp={Rmp} R34={R34} Ibmain = {
    Ibmain} Sa_b = {Sa_b} Cin={Cin}
SYMATTR InstName X1
SYMBOL voltage 160 192 R180
WINDOW 0 24 96 Left 2
WINDOW 3 24 16 Left 2
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName Vdd
SYMATTR Value 1.8
SYMBOL voltage 160 400 R0
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName Vddb
SYMATTR Value 1.8
SYMBOL cap -112 144 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName Cin1
SYMATTR Value {Cin}
SYMBOL res -96 240 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName Rin1
SYMATTR Value {Rin}
SYMBOL cap -112 320 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName Cin2
SYMATTR Value {Cin}
SYMBOL res -96 416 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName Rin2
SYMATTR Value {Rin}
SYMBOL cap 192 -112 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName Cfb1
SYMATTR Value {Cin/8}
SYMBOL res 208 -16 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName Rfb1
SYMATTR Value {Rin*8}
SYMBOL cap 208 576 R90
WINDOW 0 0 32 VBottom 2
WINDOW 3 32 32 VTop 2
SYMATTR InstName Cfb2
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SYMATTR Value {Cin/8}
SYMBOL res 224 672 R90
WINDOW 0 0 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName Rfb2
SYMATTR Value {Rin*8}
SYMBOL cap 416 176 R0
SYMATTR InstName Cload1
SYMATTR Value {Cin}
SYMBOL cap 416 368 R0
SYMATTR InstName Cload2
SYMATTR Value {Cin}
SYMBOL bv -352 208 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName B1
SYMATTR Value V=-V(Vi)/2
SYMBOL bv -352 384 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
SYMATTR InstName B2
SYMATTR Value V=V(Vi)/2
SYMBOL voltage -496 288 R90
WINDOW 0 -32 56 VBottom 2
WINDOW 3 32 56 VTop 2
WINDOW 123 0 0 Left 0
WINDOW 39 0 0 Left 0
SYMATTR InstName V1
SYMATTR Value 0.9
SYMBOL voltage -1056 336 R0
WINDOW 123 24 124 Left 2
WINDOW 39 0 0 Left 0
WINDOW 3 24 44 Left 2
SYMATTR Value2 AC 1
SYMATTR Value PULSE(0 150m 1u 100f 100f 10m 0 1)
SYMATTR InstName Vi
SYMBOL e 672 240 R0
SYMATTR InstName E1
SYMATTR Value 1
TEXT 208 -208 Left 2 !.param Rbn=4.8 Rbp=6.2
TEXT 208 -184 Left 2 !.param Cin=32.36p Ibmain=572.1u Rmp=0.907 Sa=0.988 Sa_b
    =16.907 R34=95
TEXT 208 -232 Left 2 !.lib 'C:\\Users\\terlo\\OneDrive\\Documenten\\LTspiceXVII
    \\lib\\cmp\\log018.l' TT
TEXT 208 -160 Left 2 !.param Rin=100G
TEXT -1288 -56 Left 2 !;tran 0 3.41u 1.001u 0.005u
TEXT -1288 -32 Left 2 ;20*log10(1.2/abs(V(n005,n001)))
TEXT -1288 -8 Left 2 !;ac dec 100 1 100G
TEXT -1288 -104 Left 2 !;noise V(Vo) Vi dec 10 10k 100G
TEXT -1288 -176 Left 2 !;meas TRAN A0 FIND 20*log10(1.2/abs(V(n005,n001))) AT 0u
TEXT -1288 -200 Left 2 !.meas TRAN A1 FIND 20*log10(1.2/abs(V(n005,n001))) AT
    2.405u
TEXT -1288 -152 Left 2 !.meas TRAN current FIND I(Vdd)*1e6 AT 2.405u
TEXT -1288 -128 Left 2 !;meas TRAN FoM PARAM min(0.4*pow(2.5,(abs(A0-19.3))) +
    0.1*pow(10,(abs(A1-57.3))) + abs(current),50Meg)
TEXT -1288 -224 Left 2 !;save I(Vdd) V(n005) V(n001)
TEXT -1288 40 Left 2 !;step dec param Sa 1 5000 5
```

```
TEXT -1288 64 Left 2 !;step dec param Sa_b 1 5000 5
TEXT -1288 112 Left 2 !;step dec param Ibmain 1u 1000u 5
TEXT -1288 16 Left 2 !;op
TEXT -1288 -80 Left 2 !;meas NOISE vorms INTEG V(onoise)*1e6 FROM 10k TO 100G
```