Embedded systems: Assignment 5

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Introduction

In this document I will show and explain my solutions to the tasks detailed in Assignment 5 of the course Embedded Systems 2018.

Assignment 5.1

See the below equations for my answer to task 1 of assignment 5. In case my solution is not clear some specifications: my cache is denoted by square brackets, its four different cache lines separated by commas. Each cache line in turn contains a set of values, which the line itself or a line above it must contain. An empty set means that there is no information about which values must be contained in the line or above, aside from the information contained in lines below it. My cache is filled from the left and entries age to the right.

$$
\begin{aligned}
1 &: [\{\}, \{\}, \{\}, \{\}] \\
2 &: [\{a\}, \{\}, \{\}, \{\}] \\
3 &: [\{a\}, \{\}, \{\}, \{\}] \\
4 &: [\{\}, \{a\}, \{\}, \{\}] \\
5 &: [\{d\}, \{\}, \{a\}, \{\}] \\
6 &: [\{d\}, \{\}, \{a\}, \{\}] \\
\text{out} &: [\{b\}, \{d\}, \{\}, \{a\}]
\end{aligned}
$$

Assignment 5.2

(a): Both task-set A and B are EDF schedulable, as for all tasks $D = T$ and the utilization for both sets is smaller than one: $U_A = \frac{13}{20} < 1$ and $U_B = \frac{69}{70} < 1$. This is assuming that context switches have no overhead, as discussed in the slides.

(b): For both task sets there are three tasks, so that $U_{\text{lub}} = 3(2^(1/3) - 1) \approx 0.78$. With this we can then see that $U_A \leq U_{\text{lub}}$ and that $U_B \nleq U_{\text{lub}}$, meaning that task-set A is RM schedulable while set B is not.