FPGA Implementation of a Digitally Controlled Oscillator for AD-PLLs (All digital Phase locked loops)

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INTRODUCTION

Precision clock generation is essential in high-speed digital systems, especially in applications such as RF communication, digital phase-locked loops (ADPLLs), and mixed-signal SoCs. A Digitally Controlled Oscillator (DCO) is a key component in these systems, allowing frequency tuning via digital inputs, which is critical for adaptive clocking, synchronization, and dynamic performance scaling.

From a hardware implementation perspective, designing a DCO on an FPGA presents unique opportunities and challenges. Unlike ASICs, FPGAs offer reconfigurability, rapid prototyping, and integration with digital control logic — making them ideal for validating DCO architectures in real-time systems. However, limitations such as lack of native analog components and the need for synthesizable, clock-driven logic require careful architectural choices. Instead of using behavioural delays, clocked pipeline structures are essential to emulate delay cells and achieve controllable oscillation behaviour.

This project focuses on designing and implementing a ring-type DCO on an FPGA using Verilog HDL, with tuneable coarse and fine frequency control. The design is adapted for synthesis using a 45nm technology model and is tested on a Basys3 FPGA board, demonstrating both functional correctness and practical feasibility of digital delay control in hardware.

LITERATURE SURVEY

Recent research on DCOs highlights the importance of robust supply noise compensation (SNC) to improve jitter performance and PVT (Process, Voltage, Temperature) tolerance. Techniques such as replica-based analog closed loops and self-biased SNC architectures have demonstrated excellent performance in GHz-range DCOs fabricated on advanced 28nm and 40nm CMOS processes [1][2].

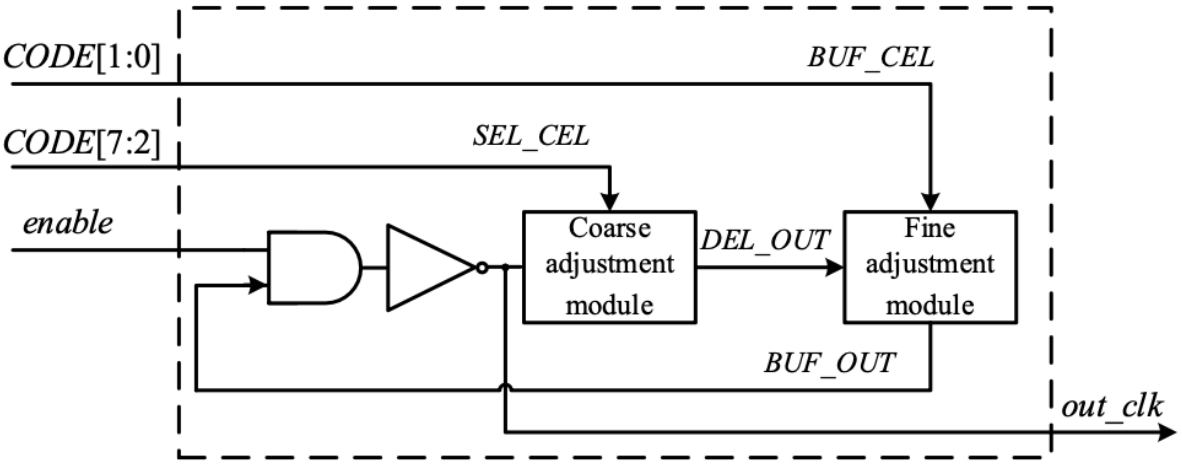
However, these implementations are predominantly on ASIC platforms. Limited work exists on implementing DCOs on FPGAs, where frequency control granularity is constrained by the system clock. A notable study on Xilinx Zynq 7035 showed a frequency range of 6–150 MHz [3], emphasizing the need for techniques that extend range and resolution on FPGA platforms. Fine control and discrete frequency steps are crucial to reduce phase noise in ADPLLs [4].

This project addresses the gap by designing a ring-type DCO with coarse and fine adjustment blocks and implementing it on a Xilinx Basys3 FPGA board.

PAPER TITLE	AUTHORS AND PUBLICATIONS	SUMMARY	INFERENCE
A Low-Jitter 8-GHz RO-Based ADPLL With PVT-Robust Replica-Based Analog Closed Loop for Supply Noise Compensation	Hyojun Kim , Student Member, IEEE, Woosong Jung , Student Member, IEEE, Kwandong Kim, Sungwoo Kim , Member, IEEE, Woo-Seok Choi , Member, IEEE, and Deog-Kyoon Jeong , Fellow, IEEE IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 57, NO. 6	One of the major challenges in the design of an RO-based PLL is to mitigate the degradation of jitter performance by supply noise. The loop filter of a PLL can be realized in a digital manner, obtaining immunity to the impact of supply noise. the noise contribution of the additional hardware for the technique is minimized so as not to degrade the phase noise of the output clock. The prototype ADPLL is fabricated in 40-nm CMOS technology, achieving a jitter-power figure of merit (FoM) of −241 dB without supply noise and a jitter reduction of −23.8 dB in the presence of a 20-mVrms white noise on the supply.	The technique does not extort the voltage headroom of the DCO nor does it add any circuit components in the delay cell of the RO, thereby allowing high-frequency oscillation.
A 1.05-to-3.2 GHz All-Digital PLL for DDR5 Registering Clock Driver With a Self-Biased Supply-Noise-Compensating Ring DCO	Yeonggeun Song , Student Member, IEEE, Han-Gon Ko , Member, IEEE, Changhyun Kim , Fellow, IEEE, and Deog-Kyoon Jeong , Fellow, IEEE IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 69, NO. 3	A registering clock driver (RCD) performs the role of buffering the command and address bus, chip selects, and clock between the host controller and the DRAMs in server memory modules. One of key challenges of designing the PLL in the RCD is responding to the sudden voltage droop due to workload transitions. By combining two cur-rent sources that have an opposite dependency on supply variations, the proposed AD-PLL provides constant current to a RO over a wide supply voltage range.	The AD-PLL for DDR5 RCD application with a self-biased SNC technique is presented. By combining two current sources that have opposite dependency on supply variations, the proposed AD-PLL improves a static voltage margin and offers robustness against supply fluctuation.
FPGA Implementation of Ring-Type Digitally	Zhihao Shen Nanjing University of Aeronautics and Astronautics, Ying Yang Nanjing	Generally, FPGA-based DCOs can be divided into the following two types: the cyclic phase accumulation DCO and	The CAM provides a large frequency adjustment range. The compensation

Controlled Oscillator	University of Aeronautics and Astronautics, Ying Zhang Nanjing University of Aeronautics, Yongxin Shan Nanjing University of Aeronautics and Astronautics, Xin Chen Nanjing University of Aeronautics Astronautics 2024 3rd International Symposium on Aerospace Engineering and Systems (ISAES)	the pulse addition and subtraction DCO. Logic gates in FPGA have inherent delay time. Different delay time of delay unit can be achieved by different number of logical gates, which provides an opportunity for the application of RO in FPGA. Based on this feature of FPGA. The innovative ring-DCO proposed in this paper is composed of a coarse adjustment module (CAM) and a fine adjustment module (FAM).	block in CAM can fix the irregular waveform. The FAM further reduces the adjustment step size by changing the number of low-delay buffers in oscillation loop. The ring-DCO can take up smaller area resources while obtaining a wide frequency range.
FPGA Based DCO With Fine Control Correlation Calibration Technique	Abdullah Almasoud Department of Electrical Engineering King Saud University, Mohammed Abbas Department of Electrical Engineering King Saud University, Abdullah Alghaihab Department of Electrical Engineering King Saud University, Mohammed Aboelola Department of Electrical Engineering King Saud University 2022 3rd International Conference on Electrical Engineering and Informatics	This work presents an FPGA based DCO implementation for use in ADPLL. It also presents the calibration technique which solves the non-monotonicity problem between the control code and the oscillation frequency. The issue is observed when implementing fine control of the DCO using ring oscillator (generator on delays) which is implemented with 4 carry4 blocks and 16 input multiplexer within the seven series Xilinx FPGAs for minimum controlled delay.	High frequency gate delay oscillators using carry4 elements for fine control FPGAs suffer from correlation issue. Calibration method must be used to correct for that. To further improve this process, additional steps are needed to compensate or the non-linearity between the control code and the output frequency.

DESIGN



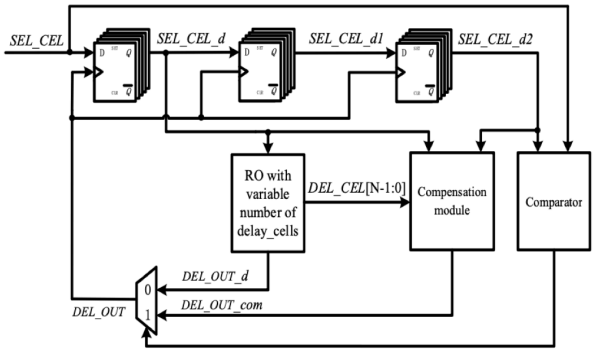


Fig. 4 Structure of the CAM

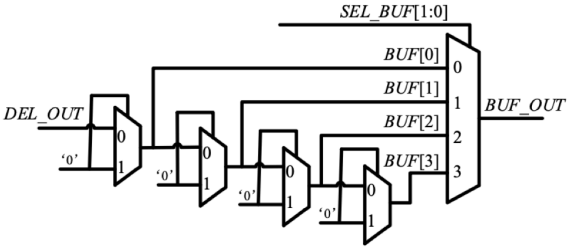


Fig. 8 Structure of FAM

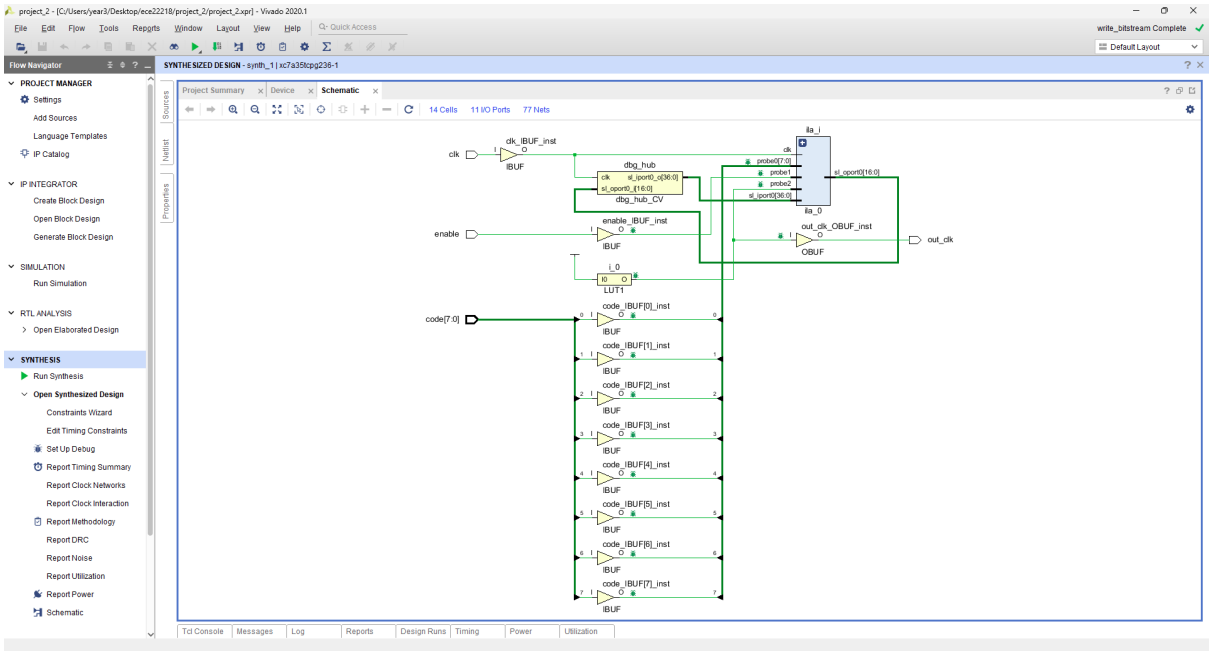
The proposed DCO architecture consists of:

- A ring oscillator formed by chaining multiple clocked delay cells.
- A Coarse Adjustment Module (CAM) that selects a delayed node using a 64-to-1 multiplexer.
- A Fine Adjustment Module (FAM) that uses a chain of buffer stages to introduce smaller incremental delays.
- A combined control word (code[7:0]) where the upper 6 bits select the CAM output and the lower 2 bits control the FAM path.

Most oscillator designs for DCOs rely on analog components or behavioural simulation models. This approach introduces novelty by:

- Implementing a purely digital, clock-based ring oscillator, which is rarely modelled at the gate/register level for FPGA use.
- Hierarchical delay control, combining coarse (multiplexer-based) and fine (buffer-chain based) tuning paths to simulate analog-level delay resolution in digital hardware.
- No reliance on analog primitives, making it portable across different FPGA platforms and usable in safety-critical or radiation-hardened applications where full-digital designs are preferred.

The design is especially suited for adaptive clocking, digital PLLs, and real-time tuneable frequency generators, all of which benefit from its flexible, digital-only nature.



SIMULATION

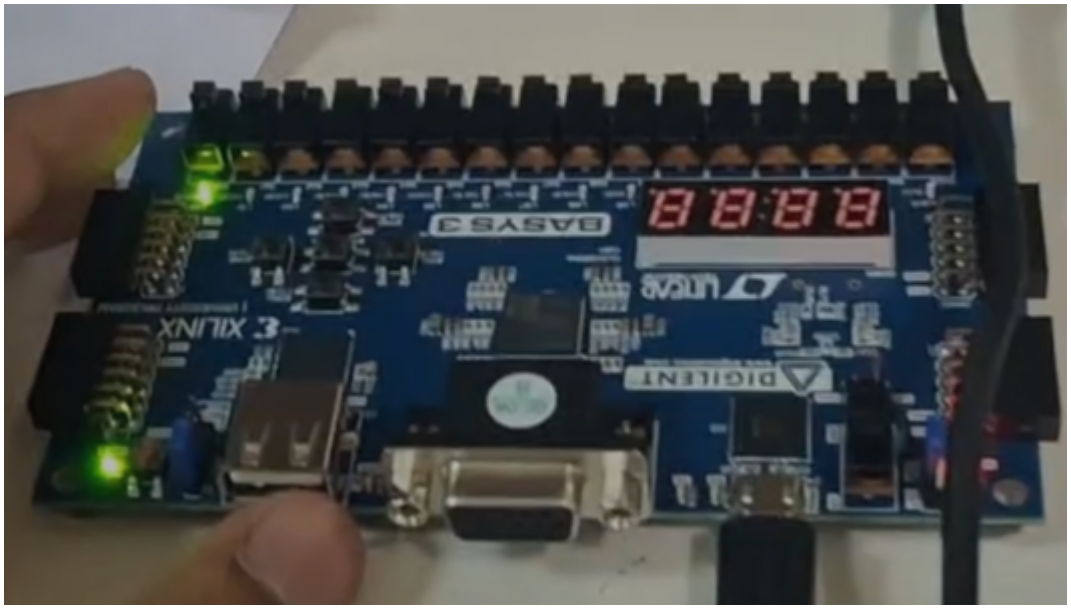
The Verilog design was simulated using Xilinx Vivado. Since the hardware delays (#) were replaced by clock-driven logic, the simulation focused on verifying timing correctness over multiple clock cycles and functional behaviour of the ring DCO and its control mechanisms.
Simulator:
Vivado Testbench Inputs:

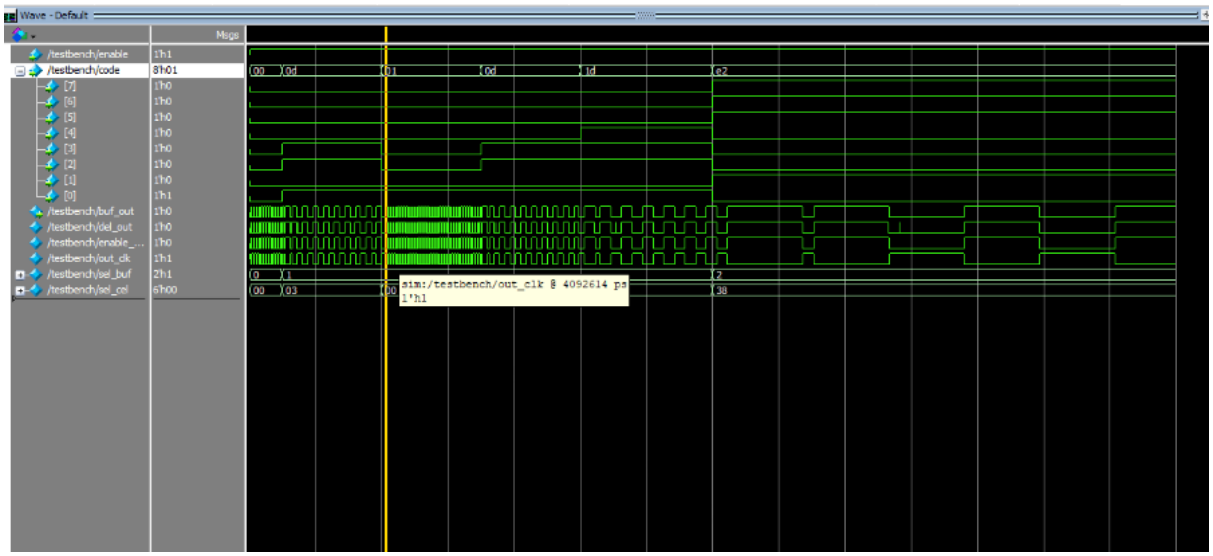
- clk: 100 MHz clock (10 ns period)
- code[7:0]: Digital control input split into:
    - code[7:2] → Coarse delay selection
    - code[1:0] → Fine tuning path selection
- enable: Enable signal to toggle oscillator activity

Parameter	Value
Clock frequency	100 MHz
Delay chain length (CAM)	64 stages
Buffer chain length (FAM)	4 stages
Simulation runtime	4000 ns
Control values simulated	Varying code[7:0] from low to high

HARDWARE SELECTION

Basys 3 board was chosen due to its higher number of input pins as we need 9 input pins to run our implementation and an LED from which we can observe that the implementation is working.





RESULTS

As we increase the select inputs through the 8-bit codeword, the frequency changes, and this is observed in the waveform as shown in the previous figure. The output is a signal that is of varying frequency that works by changing the delay and varying the time period.

CONCLUSION

This project successfully demonstrates the design and FPGA implementation of a synthesizable, digitally controlled ring oscillator (DCO) with tunable delay resolution using both coarse and fine adjustment mechanisms. The use of clocked logic in place of simulation-only delays ensures compatibility with FPGA synthesis flows, allowing real-time validation on a Xilinx ZCU104 board. By leveraging modular Verilog design, pipelined delay cells, and hierarchical selection logic, the DCO architecture maintains flexibility and scalability while conforming to hardware constraints.

From a practical standpoint, the project bridges the gap between theoretical delay-based oscillators and their digital hardware counterparts. It highlights the effectiveness of using FPGA resources like registers and LUTs to emulate delay control logic, which is particularly relevant for prototyping digital PLLs and timing-sensitive systems.

Future Scope

- Frequency Measurement Integration: Add frequency counter modules to measure output clock dynamically on the FPGA.
- PLL Integration: Combine the DCO with a digital phase comparator and loop filter to implement a full ADPLL.
- Dynamic Control via AXI or UART: Integrate the control input with a microcontroller or processor interface to enable runtime tuning.
- Delay Calibration: Use temperature or voltage sensors for PVT-aware tuning of delay chains.
- Post-Silicon Validation: Use the FPGA model as a pre-silicon validation platform before migrating to an ASIC implementation.